



Thomas J Walker/LS/GDYN

11/03/2010 04:34 PM

To support@ti.com

cc Dung Q Vuong/LS/GDYN@LS, Tara S Silvestri/LS/GDYN@LS, Sally M Sellers/LS/GDYN@LS, Sean M Winans/LS/GDYN@LS, John K Baker/LS/GDYN@LS

bcc Thomas J Walker/LS/GDYN

Subject 4 questions regarding TI DSP P/N TMS320C6701GJCA120

Support,

I have the following questions regarding the DSP p/n TMS320C6701GJCA120?

1. Regarding the below RSV signals that specify dedicated resistors, our legacy design uses 14 kilo-ohm pull up resistors for the past 8 years in production efforts. Can you please tell me if there is any impact to the DSP operation by using 14 kilo-ohm resistors instead of 20 kilo-ohm resistors?

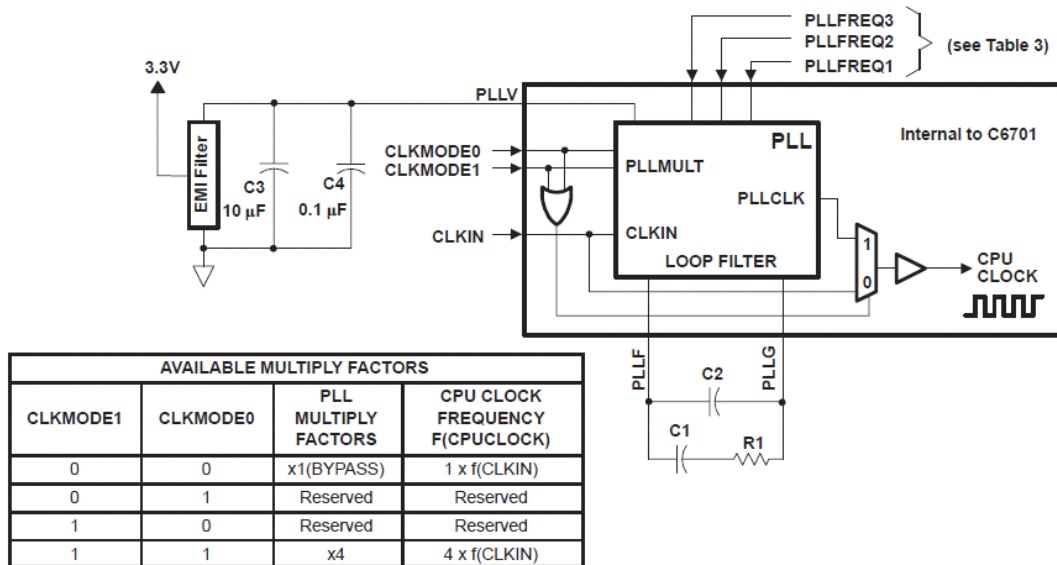
RESERVED FOR TEST			
RSV0	T2	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV1	G2	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV2	C11	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV3	B9	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV4	A6	I	Reserved for testing, pulldown with a dedicated 20-kΩ resistor
RSV5	C8	O	Reserved (leave unconnected, do not connect to power or ground)
RSV6	C21	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV7	B22	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV8	A23	I	Reserved for testing, pullup with a dedicated 20-kΩ resistor
RSV9	E4	O	Reserved (leave unconnected, do not connect to power or ground)
SUPPLY VOLTAGE PINS			
	A10		

2. Regarding the below EMU0/EMU1 signals, our legacy design has used 3.01 kilo-ohm pull up resistors for the past 8 years in production efforts. Can you please tell me if there is any impact to the DSP operation by using 3.01 kilo-ohm resistors instead of 20 kilo-ohm resistors?

JTAG EMULATION			
TMS	L3	I	JTAG test-port mode select (features an internal pullup)
TDO	W2	O/Z	JTAG test-port data out
TDI	R4	I	JTAG test-port data in (features an internal pullup)
TCK	R3	I	JTAG test-port clock
$\overline{\text{TRST}}$	T1	I	JTAG test-port reset (features an internal pulldown)
EMU1	Y1	I/O/Z	Emulation pin 1, pullup with a dedicated 20-k Ω resistor [¶]
EMU0	W3	I/O/Z	Emulation pin 0, pullup with a dedicated 20-k Ω resistor [¶]

3. Regarding the below PLLF/PLLG signals, our legacy design has uses R1 = 60.4 ohms, C2 = 560 pF, and C1 = 0.027 uF for the past 8 years in production efforts. Our configuration is the same as the below per DSP data sheet TMS320C6701GJCA120 except R1 and C1 are swapped. The R1 in our legacy design is common to PLLF instead of PLLG and C1 in our legacy design is common to PLLG instead of PLLF. Can you please let me know if this is a problem?

clock PLL (continued)



- NOTES:
- A. Keep the lead length and the number of vias between the PLLF pin, the PLLG pin, and R1, C1, and C2 to a minimum. In addition, place all PLL external components (R1, C1, C2, C3, C4, and the EMI Filter) as close to the C6000™ DSP device as possible. For the best performance, TI recommends that all the PLL external components be on a single side of the board without jumpers, switches, or components other than the ones shown.
 - B. For reduced PLL jitter, maximize the spacing between switching signals and the PLL external components (R1, C1, C2, C3, C4, and the EMI Filter).
 - C. The 3.3-V supply for the EMI filter must be from the same 3.3-V power plane supplying the I/O voltage, DV_{DD} .
 - D. EMI filter manufacturer: TDK part number ACF451832-333, 223, 153, 103. Panasonic part number EXCCET103U.

Figure 5. External PLL Circuitry for Either PLL x4 Mode or x1 (Bypass) Mode

4. Regarding decoupling capacitors DSP p/n TMS320C6701GJCA120, we have been using 4 of 0.1 uF capacitors decoupling between 1.8 Vdc core voltage and 3.3 Vdc I/O voltage in our legacy design for the past 8 years. Do you have any idea why this is necessary or what the purpose of this configuration is?

Thanks much,

Thomas (Tom) J. Walker, Senior Engineer Specialist

Proj. Lead - TLH ED&D Abrams/Bradley/Stryker Prod. Sup.

General Dynamics Land Systems, TLH Operations

2930 Commonwealth Boulevard, TLH, FL 32303

Desk = 850-574-4868; Cell = 850-528-2402; Fax = 850-574-4501; email = walkertj@gdls.com "One Team... One Goal"