Dual Link DVI Receiver Implementation

This application note describes some features of single link receivers that must be considered when using 2 devices for a dual link application. Specific characteristics of the TFP401 and TFP501 are mentioned, and signals measured from a pair of TFP401 devices operated in parallel are shown.

A single DVI link consists of 3 T.M.D.S. data signal pairs and a reference clock signal pair. In a single link DVI receiver, each signal is terminated with 50 ohms to supply voltage internal to the receiver device. With dual link DVI, there are 6 T.M.D.S. data signal pairs and a single reference clock signal pair. Possible block diagrams for single and dual link receivers are shown in figures 1 and 2.

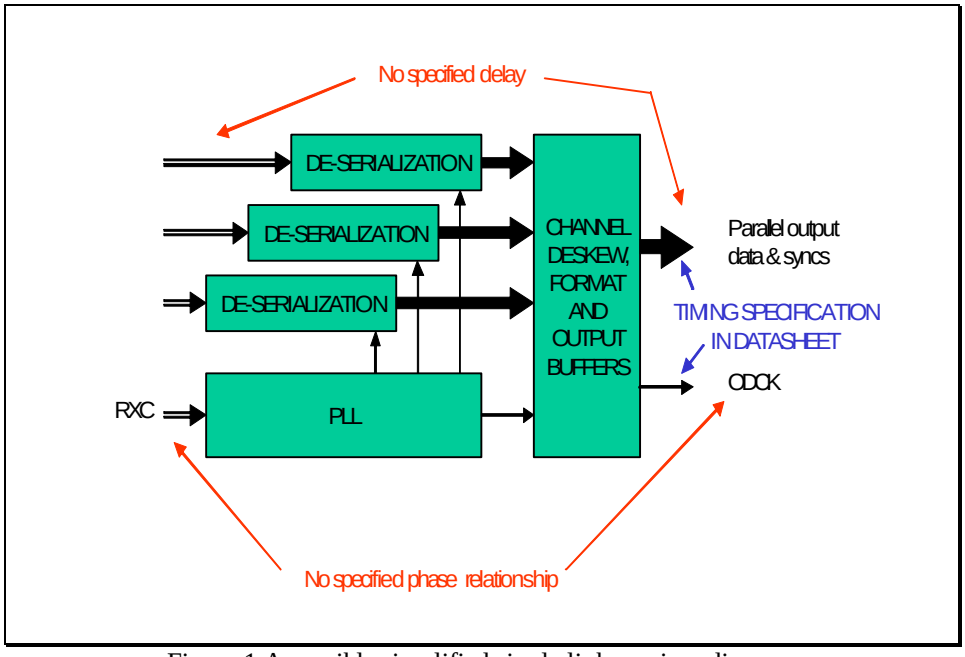

Figure 1 A possible simplified single link receiver diagram

In the receiver, the clock is used to run a PLL which will provide a clock for de-serializing the data streams. Each data channel is de-serialized and aligned with the others. The data is output from the device using a clock also derived from the PLL

In the dual link receiver the DVI clock is used to run the PLL and the de-skew circuit aligns all of the channels. The data is output with a clock derived from the PLL.

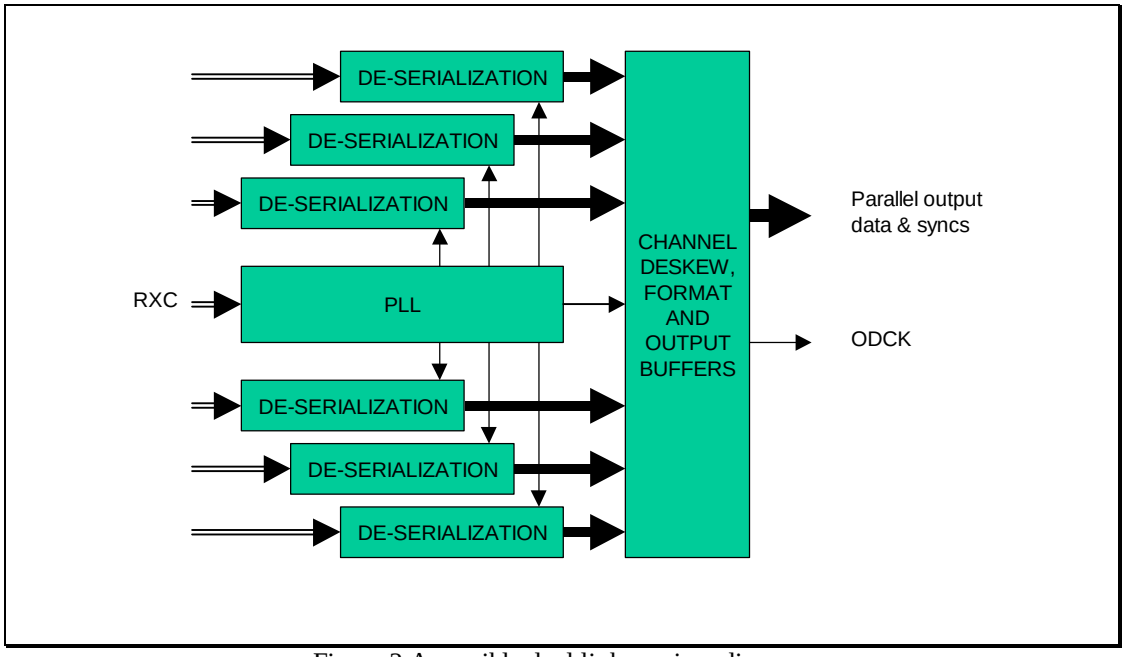

Figure 2 A possible dual link receiver diagram

When a dual link system is created using two single link receivers, both receivers expect to receive and terminate the clock. Each device has a separate PLL with its unique delay and phase alignment. Each device will deskew the channels it receives. Each device will receive and process three channels, but will not have information on the processing which takes place in the other receiver. The system design must handle at least the following considerations:

1. Attenuation and possible reflections due to dual termination of the DVI clock.
2. Conversion from the clock domains of the 2 receiver outputs to one clock domain.
3. De-skew of the two "links", or receiver outputs. The individual receivers have de-skewed their channels, but the parts may have skew as shown from tests above.
4. Format and signal detection
5. HDCP reception and processing

CLOCK DISTRIBUTION

The first consideration is the single DVI clock. Since each receiver terminates the clock, the signal level will be reduced. Instead of driving a 50 ohm load, the DVI transmitter current sink will be driving 25 ohms. Since DVI is a current sink device, the voltage level will be reduced by half. Another consideration is reflections on the clock network. With the rise times of DVI and the clock speed up to 165MHz, the transmission line effects can be significant. An impedance matching network or careful routing of the traces to avoid transmission line stubs may be needed.

CLOCK PHASE AND OUTPUT SKEW

The second and third considerations are affected by the delays in the single link receivers. The DVI 1.0 specification requires a receiver pipeline delay (t_R, figure 3-7 of the specification) to be a maximum of 64 pixels. There are no requirements on the input to output clock timing. Refer to figure 1. Pipeline delay is not typically a datasheet value for DVI receivers. The architecture of the TFP401 allows input to output clock phase differences on acquisition of the DVI signal. Also, the data pipeline delay through the part may vary from acquisition to acquisition. The following figures illustrate the effects of multiple acquisitions of a dual link signal by two TFP401 devices operated in parallel. Probe points were on test pads on the transmission lines near the devices. Reflections due to probing in the middle of the transmission lines are apparent.

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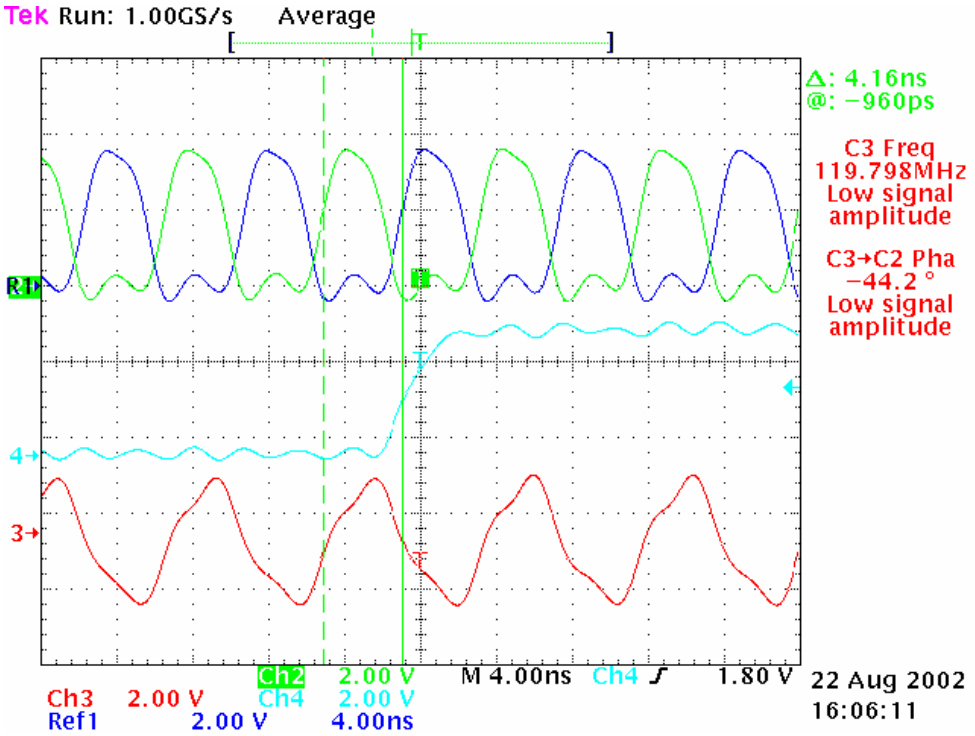

Figure 3 ODCK variation between devices on multiple acquisitions.

Figure 3 shows an example of phase variation possible between ODCK outputs of two devices. Channel 4 is DE of the first receiver, Channel 3 is ODCK of the first receiver, and channel 2 is the ODCK of the second receiver. The R1 channel showed the phase of a previous acquisition of the DVI signal.

Figures 4 and 5 show resulting data alignment of the two receiver outputs with respect to one ODCK. Channel 2 is a data bit from one receiver and Channel 4 is a data bit from the other (second) link receiver. When the clocks roughly align, as in Figure 4, the receiving device should be able to properly sample the data. When the clocks are not aligned as in Figure 5, the data sampled would be expected to be indeterminate.

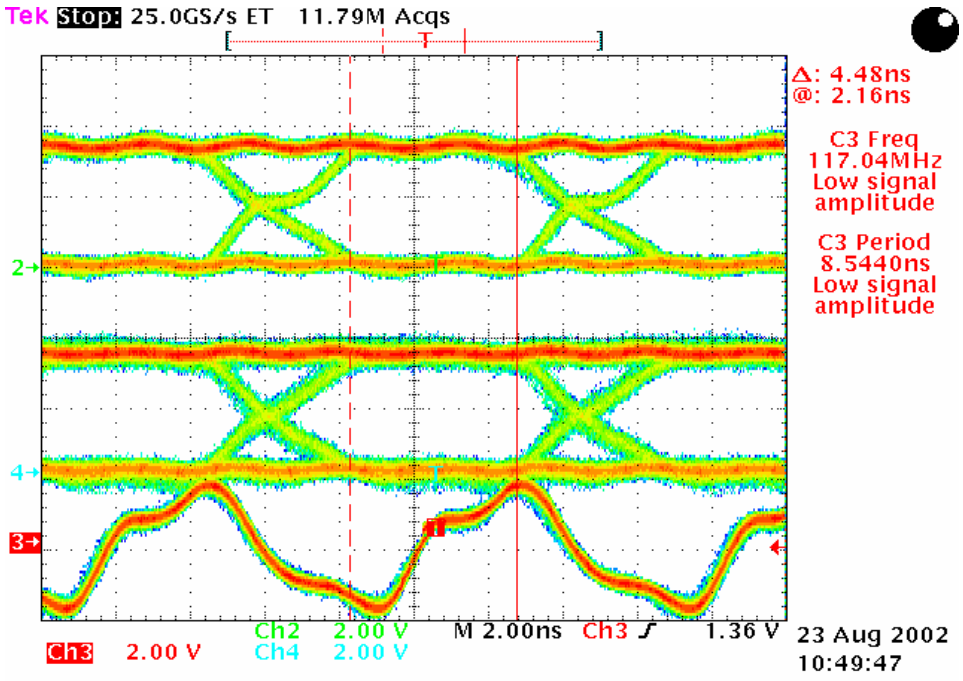

Figure 4 Output data aligns between receivers.

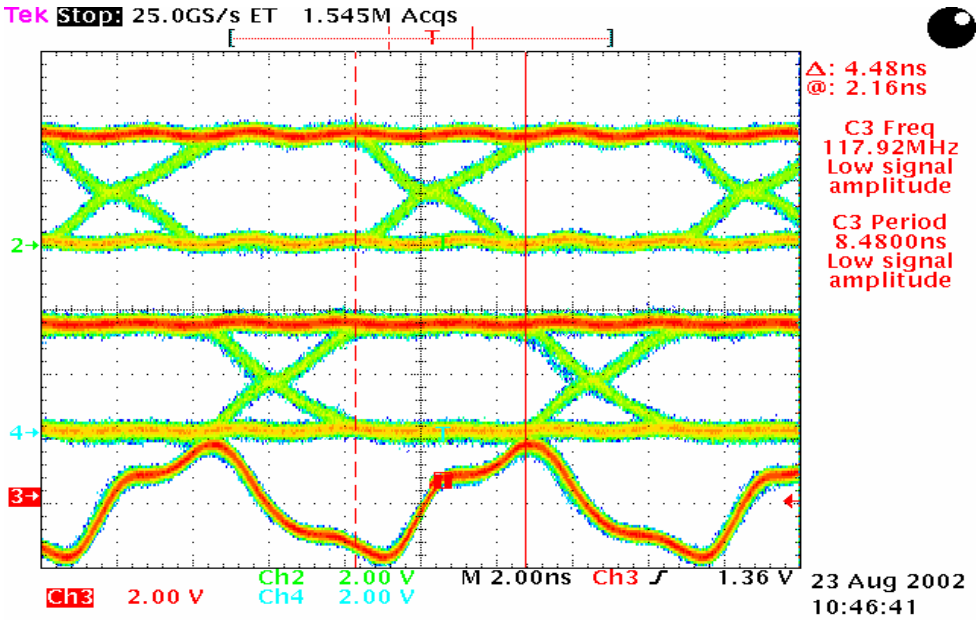

Figure 5 Output data from receivers is out of phase.

Additionally, single link DVI receivers do not specify pipeline delay values. The pipeline delay in the TFP401 is adjusted to compensate for skew of the signals as well as other internal operation. If when the two receivers acquire the signal they pick the same relative clock phase and pipeline delay, the delay between the output data may be small, and if the clock phase difference of the parts and DVI clock jitter is small, the monitor may display properly. This case is shown in Figure 6 below . The delay between one of the receiver DE and the other receiver DE is small. The sampling of both data sets by DCLK would produce the proper pixel sequence.

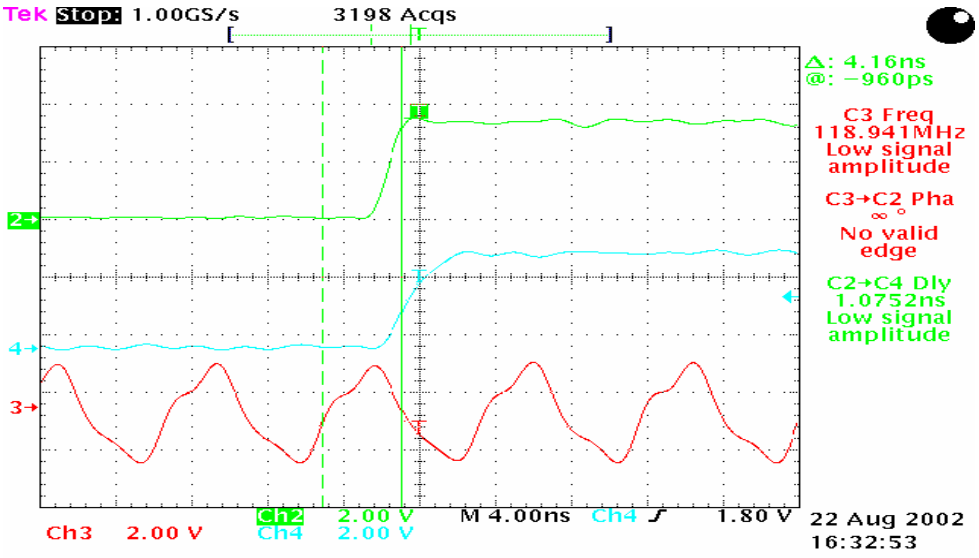

Figure 6 Delay between the 2 receivers DE is small

However, the pipeline delay of the TFP401 will vary from device to device and acquisition to acquisition. The delay through the TFP401 is less than the maximum allowed by the specification, exact values and variation are not currently available.

Figure 7 shows variation of the starting position of the data (horizontal line) of the two TFP401's. The Channel 2 trace and stored reference traces show a variety of DE signal locations of one receiver (A) obtained over a number of acquisitions. Channel 4 is the DE from the other receiver (B). Channel 3 is the ODCK from receiver A.

The captures are not all combinations that are possible from the parts. These captures were from relatively few acquisitions in a demonstration test. The variation pictured might be expected to produce any of the following Pixel sequences:
N, N-1, N+2, ...
N, N+1, N+2, ...
N, N+3, N+2, ...
N, N+5, N+2, ...
Other timing combinations could produce other pixel sequences.

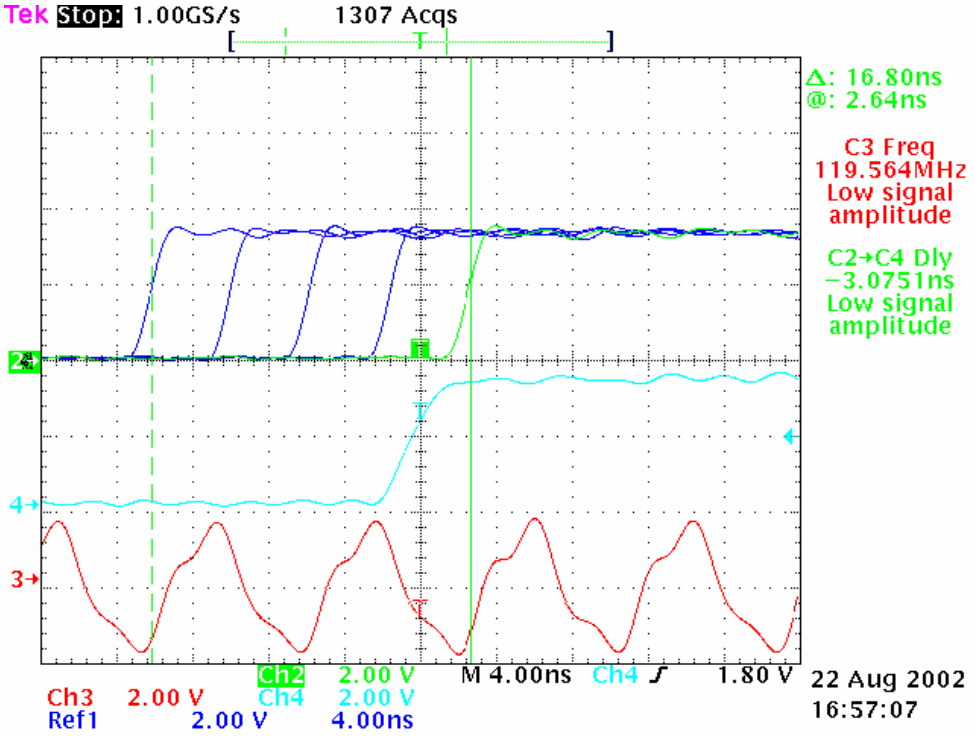

Figure 7 Delay variation between DE outputs of the 2 receivers

POSSIBLE CLOCK DOMAIN AND DESKEW SOLUTIONS

A single link receiver contains several system elements including the de-serialization and de-skew of the channels. A simplified diagram of a possible dual link system using single link receivers is shown in the figure 8. As mentioned, pipeline delay and input to output clock phase are not datasheet parameters. This is not a concern to the single link application since output clock to data timing is specified.

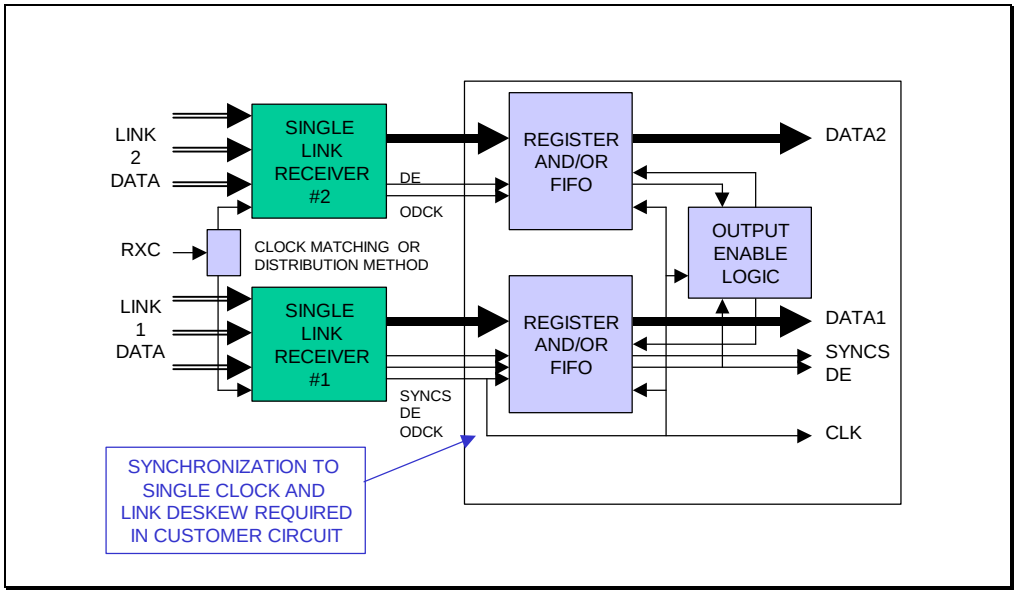

Figure 8 Possible synchronization diagram for 2 single link receivers.

For the data to be used by the downstream circuitry, a re-timing circuit (FIFO or other) must then be used to change from 2 clock domains back to 1 and allow for synchronization of the pixel streams. The max delay variation of the TFP401 is not presently known, sizing of the FIFO depth would depend on the risk and robustness desired by the designers. Line or frame buffers may be other possible solutions.

FORMAT AND SIGNAL DETECTION

A fourth issue which must be considered in a dual link implementation is detection of the valid format. When the system built with 2 single link receivers is operating in dual link mode, both receivers decode the information provided and SCDT should work normally. When the DVI frequency drops and the link transitions from dual link to single link operation, the transmitter should turn off the second link. The receiver used for this link is still active however, and is receiving a valid clock. The receiver device will output ODCK and the device will attempt to decode the input it receives. With the TFP401, if the device decodes sufficient edges on DE, it will set SCDT high. With noise present at the receiver input, this is statistically possible. When the noise looks much like a DVI signal, which could occur with crosstalk from the single link, detection of DE may be very likely

Table 1 below shows input noise levels collected from a board using 2 TFP401 devices in a dual link implementation. This board would frequently set SCDT high on the second link when operating in single link mode.

DVI cable	**Peak to peak noise coupled TMDS 3+/-**	**Peak to peak noise coupled TMDS 4+/-**	**Peak to peak noise coupled TMDS 5+/-**
2m dual link cable 1	36mV	37mV	34mV
2m dual link cable 2	47.8mV	28mV	33mV
5m dual link cable	23.8mV	22.1	19.7

Table 1: Second link input noise levels with different DVI cables

Table 1 shows that the input noise levels with 2m dual link cables varied significantly and the 2m cables measured greater than the 5m dual link cable. A 2m single link cable, showed the input noise level coupled was same if no cable is connected. Figures 9 to 11 show representative noise measured with the 3 dual link cables shown in table 1. Note that although closed, the distribution begins to show the shape of an eye. A very sensitive receiver, under the right crosstalk condition may begin to decode a signal from this noise.

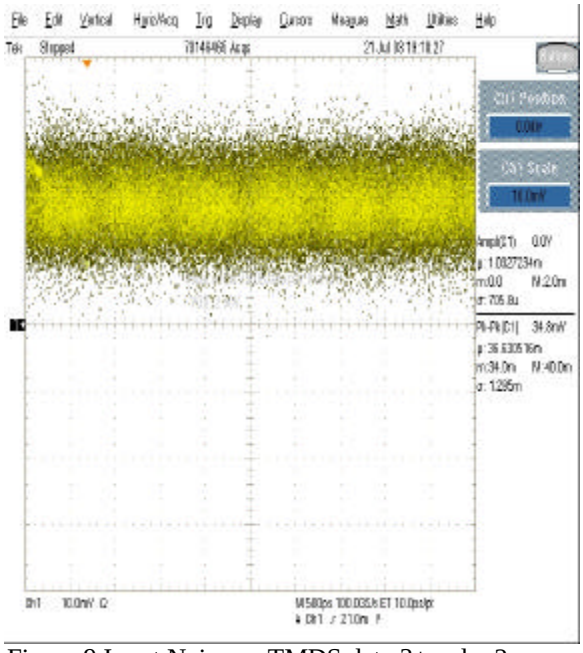

Figure 9 Input Noise on TMDS data 3+and – 2m Dual link cable 1

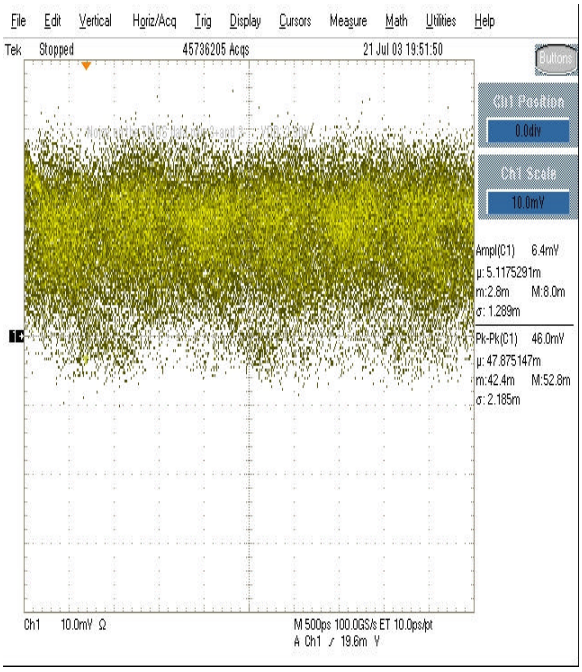

Figure 10Input Noise on TMDS data 3+and-2m Dual link cable 2

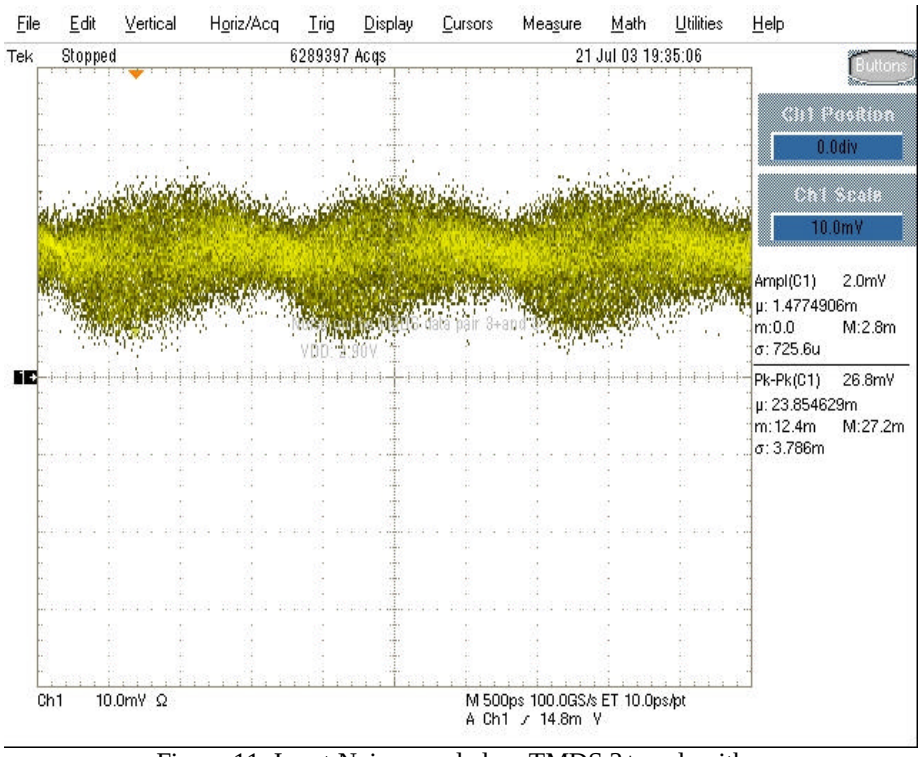

Figure 11: Input Noise coupled on TMDS 3+ and- with a 5m Dual link cable

Good design practices on the board should substantially reduce crosstalk on the board, however in many cases crosstalk in the cable may not be under control of the receiving system. In such applications it is recommended that the firmware on the application board should be used to determine link activity rather than relying on the SCDT. The system may have to evaluate timing and stability of sync signals from the 2 receivers to determine if the received format is dual link or single link and within the capability of the system. Since SCDT is only a very basic indication of activity, checking timing from the single link receiver to determine if it is within the supportable limits of the system is also recommended.

HDCP

A fifth consideration for a dual link monitor using 2 single link receivers is HDCP operation. If the monitor does not use HDCP devices, a transmitter will determine that the system is not HDCP capable and should never turn on HDCP. The receiving system should work fine if all system issues are considered. If HDCP is used on both receivers, the transmitter must be able to authenticate to each receiver and provide encryption signaling to both receivers.

The TFP501 does provide the possibility to set the DDC address to 0x76 for the secondary link. The keys must be exchanged uniquely for each receiver. The HDCP 1.0 spec indicates that both links use the same keys. See table 2-3 of the HDCP 1.0 specification. The address map does not change for the secondary link receiver. Thus it will have a Bcaps & Bstatus registers which are not shown in the HDCP 1.0 register map for this receiver (table 2-3). Although the keys must be the same for the receivers, the receivers can not share the key EEPROM. The keys must be programmed into separate EEPROMs. Each receiver will then uniquely encrypt the keys in its attached EEPROM.

Possibly the most significant issue is whether the secondary link device can be signaled for HDCP encryption. The HDCP spec indicates CTL3 is used for signaling of HDCP encryption. This goes to only the primary link receiver. Since the second link receiver is really a single link receiver, it requires encryption signaling on its CTL3 signal from its RX2. In the dual link application, these are CTL9 from

RX5. There is no mechanism for sending the decryption signal to the second receiver, so this signal must come through the CTL9 signal of the 2nd link. It is not known whether all or any dual link HDCP transmitters provide this signal.

If a HDCP receiver is implemented for only the primary link, the system designer would need to determine carefully whether the system design would meet all usage, performance, compliance and licensing requirements.

A designer must consider many issues in development of a dual link product. The items which were presented here are some of those to be considered for a successful dual link design using single link receivers.

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