XIO2000 PCI Express to PCI Bus Translation Bridge Production Silicon (PG 3.1/3.2) Errata List

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1. Receiver may fail to function during link training or when L1 is enabled (PG3.1)

Description	It has been observed that the XIO2000 will sometimes fail to recognize data being received on the receiver. At the time of failure the link will go into the RECOVERY state and the XIO2000 transmitter will transmit the TS1/TS2 ordered set while the receiver is receiving TS1/TS2 ordered sets. Since the XIO2000 fails to recognize the data on its receiver the link will get stuck in the RECOVERY state for a long period of time. Eventually a timeout will occur and the XIO2000 will go back to the DETECT state and the link will retrain and function normally. The link training failure is caused by the receiver elastic buffer locking up (shuttling between 2 states). The failure shows up only when the received data (affecting recovered clock) is stopped and restarted, as during: (a) repetitive resets (including first startup) or (b) L1 shutdown and restart.
Impact	This problem could result in loss of link
Workaround	Do not enable L1
Course of Action	Fix in next revision of silicon

2. When latency for a delayed transaction (IOR/W, MR, MRL, or MRM) is large enough for the discard timer to expire, the XIO2000 will terminate the originating master delay transaction if the discard timer expires in the middle of the transaction. (PG3.1)

Description	Within the XIO2000 there are two discard timers, one for the primary interface and other for the secondary interface. The default setting for these timers is 2^15 PCI clocks. Some BIOS's will program this timer to a smaller value (2^10 clocks for example). These timers can be changed by modifying bits 8 and 9 in the Bridge Control Register. With the smaller discard timer value, if a delayed transaction's latency is large enough the discard timer status bit will get set indicating that the discard timer expired. When the discard timer expires, the XIO2000 will flush the delayed transaction from its buffer. Now if the originating master of the delayed transaction is active on the bus at the same time the discard timer expires, the XIO2000 will flush the

	buffer and will thereby pull TRDY# away. This TRDY# wait state will last for an indefinite period of time.
Impact	A PCI master may fail to function if it does not retry a delayed transaction within the timeout period (or is prevented from doing so by another device that does not release the bus during this entire timeout period).
Workaround	Leaving the discard timer at the default value or increasing the discard timer will prevent the problem from happening.

3. A Receiver Overflow Error may occur if certain conditions are met (PG3.1, PG3.2)

Description	If a downstream PCIe memory write with data payload less than or equal to 3 dwords to a PCI device gets Master Aborted by the PCI device and the very next PCIe transaction is a non-posted transaction then the XIO2000 will return 1 extra posted header and extra data posted credits equivalent to the number of dwords in the payload. Eventually these extra returned credits will result in a receiver overflow error. Other PCIe transactions following a Master Aborted memory write will not result in this erratum occurring.
Impact	A PCI memory write that gets master aborted is in itself an error condition that should not occur under normal operating conditions so the likely hood of this problem ever occurring is almost non-existent.
Workaround	A) correct the error condition that is causing the Master Abort condition on the PCI bus. B) follow a Master Aborted PCI transaction by a posted write that will not get Master Aborted before sending a non-posted transaction.
Course of Action	A solution has been identified and verified.

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