SN65LVPE502A Application Note

Abstract

The SN65LVPE502A redriver is a dual channel, single lane USB 3.0 redriver and signal conditioner supporting data rates of 5.0Gbps. All errata for the previous part, SN65LVPE502CP, are fixed in this device. This application note provides information on implementation of the SN65LVPE502A device based on changes from the SN65LVPE502CP device.

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Introduction

The errata observed on the SN65LVPE502CP device are fixed on the SN65LVPE502A device. In addition to the errata fixes, connections are now defined as host side and device side. Connections between the host, redriver, and connector should be verified. The errata fixes include the false detect with VBUS powered devices and termination remaining enabled in certain situations.

Terminal Definition Changes

The host side and device side connections are now defined for the SN65LVPE502A device. Please reference Table 1 SN65LVPE502A Pin Functions, for a list of pin definition changes.

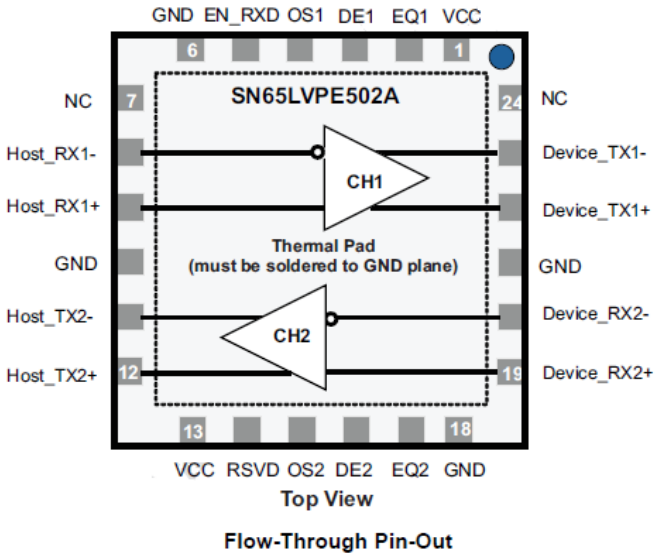

Figure 1 SN65LVPE502A Pin-Out

Table 1 SN65LVPE502A Pin Functions

PIN		I/O Type	Description
Number	Name		
HIGH SPEED DIFFERENTIAL I/O PINS			
8	Host_RX1–	I, CML	Non-inverting and inverting CML differential input for CH 1 and CH 2. These pins are tied to an internal voltage bias by dual termination resistor circuit. All pins labeled *Host* should be connected to the host. Pins labeled *Device* should be connected to the device or connector.
9	Host_RX1+	I, CML	
20	Device_RX2–	I, CML	
19	Device_RX2+	I, CML	
23	Device_TX1–	O, CML	Non-inverting and inverting CML differential output for CH 1 and CH 2. These pins are internally tied to voltage bias by termination resistors All pins labeled *Host* should be connected to the host. Pins labeled *Device* should be connected to the device or connector.
22	Device_TX1+	O, CML	
11	Host_TX2–	O, CML	
12	Host_TX2+	O, CML	

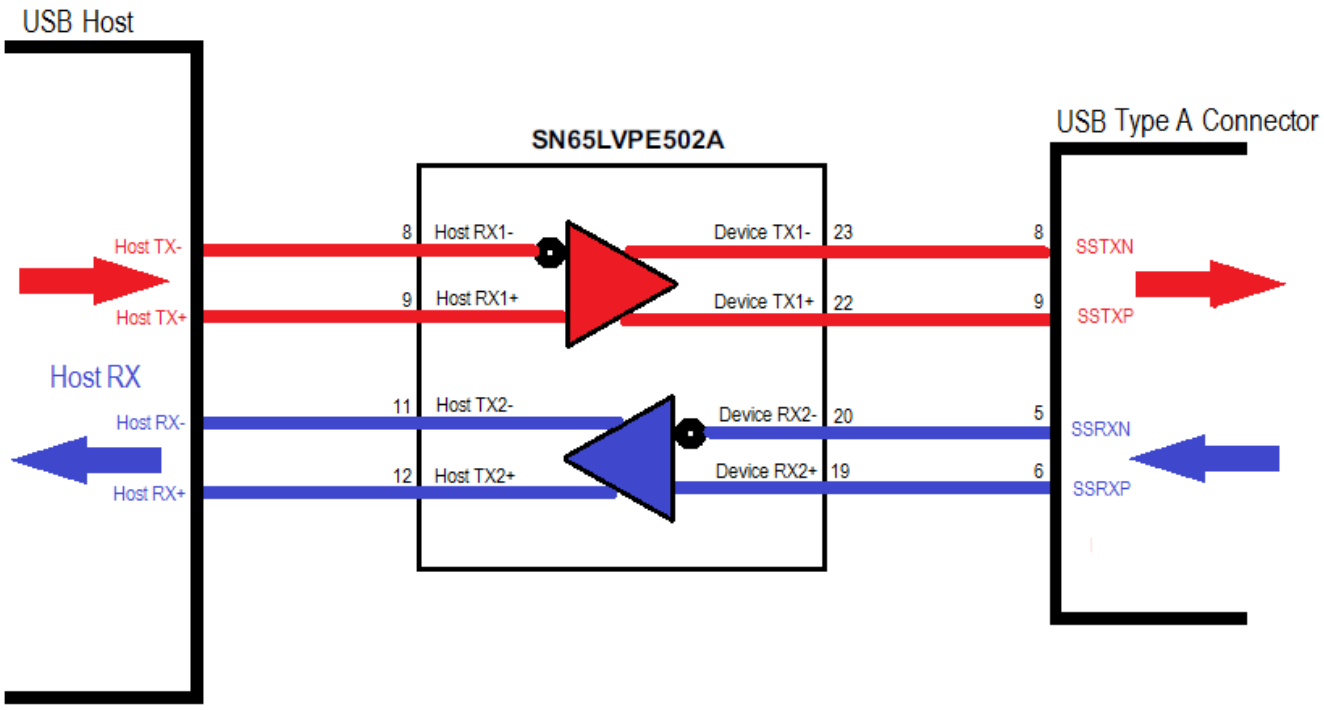

Figure 2 System Connection

Errata Fixes

False Detect

Some VBUS powered devices create noise on plug-in and cause the SN65LVPE502CP to falsely detect the device and enable termination early. After termination is enabled, the host begins polling before the device is ready. Polling will timeout and the host will enter compliance mode. This issue is fixed on the SN65LVPE502A device. Figure 2 Connection of VBUS Powered Device below shows a successful connection after a glitch is observed when the VBUS powered device is attached.

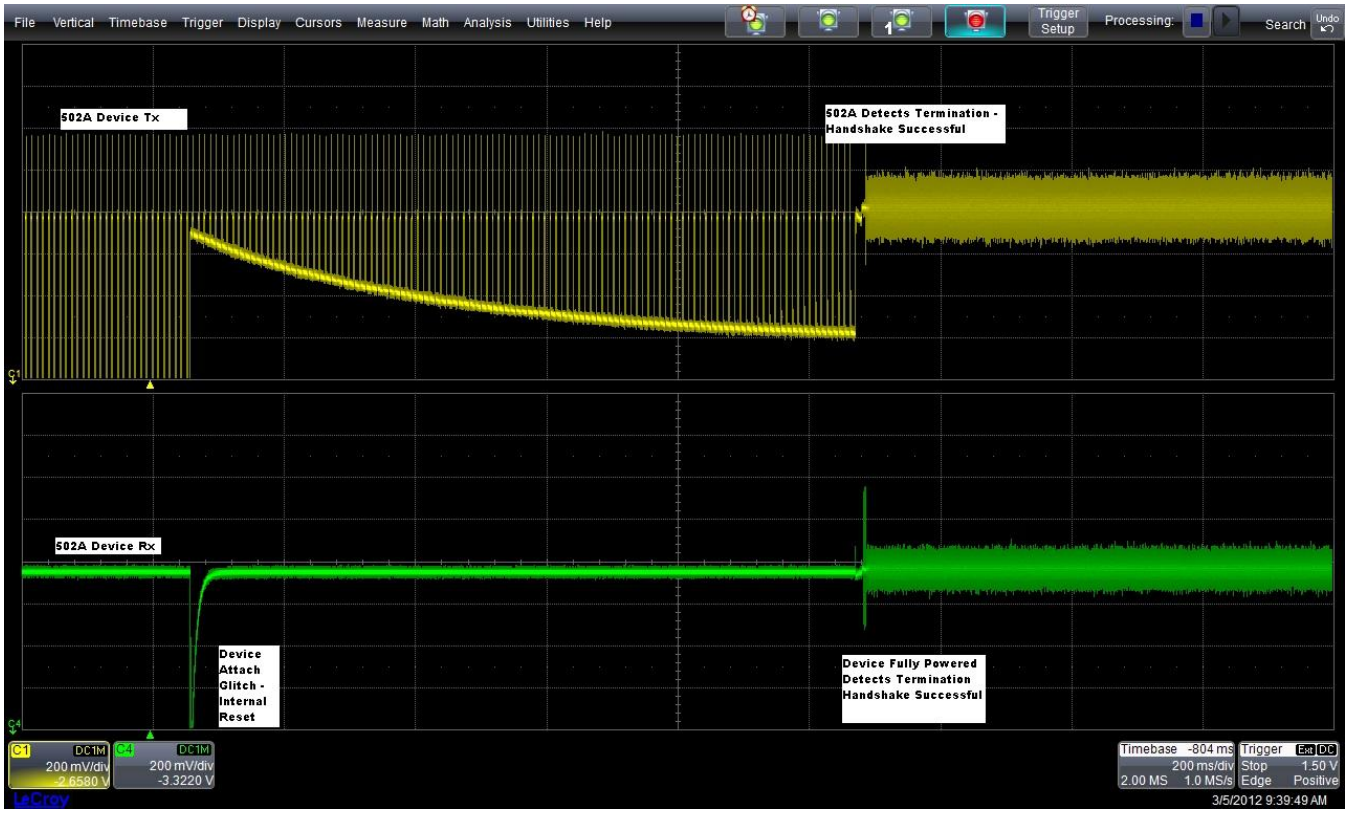

Figure 3 Connection of VBUS Powered Device

Termination Remains Enabled

In certain conditions the termination remains enabled after a device is disconnected from the SN65LVPE502CP. This issue is host software driver dependant. If host issues a warm reset within ~300ms of device disconnect the termination will remain enabled. No functional issues are observed, but the power consumption is increased while no devices are connected. This issue is no longer driver dependant and is fixed in the SN65LVPE502A. A successful disconnect may be observed in Figure 3 SN65LVPE502A Successful Disconnect below.

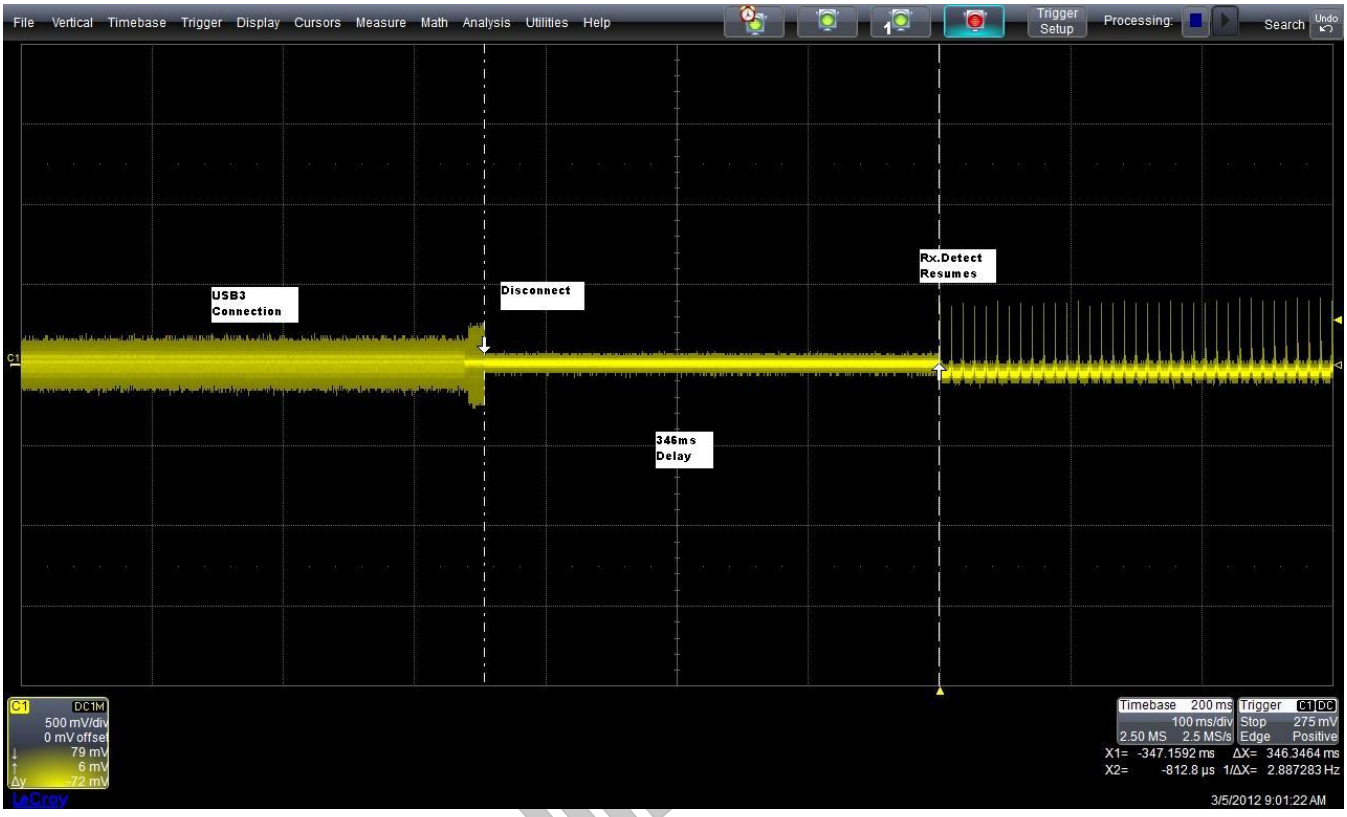

Figure 4 SN65LVPE502A Successful Disconnect