XIO2000 PCI Express to PCI Bus Translation Bridge PG1.0/2.0/2.1/3.0/3.1/3.2 Silicon Errata List

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How to Identify PG Version of Silicon

Printed on each device is a Trace Code. This code can be used to identify the PG release of the silicon.

PG1.0 trace codes are:
47AF5NW, 47AH58W, 48AH1LW, 48AH1NW, 48AH1RW, 48AH1XW, 48AH1YW

PG2.0 trace codes are:
4AA515W, 4AC234W

PG2.1 trace codes are:
53AH08W, 54A1XHW, 54A1XFW, 54A1XJW, 54A1XKW, 53AH08W, 53A45VW, 52A2E6W, 53AFF7W??

PG3.0 trace codes are:
55A09HW

PG3.1 are all units with symbolization XIO2000

PG3.2 all all units with symbolization XIO2000A

If your device does not match any of the trace codes above please write down all markings on device and contact your TI representative for identification.

Errata List

This document identifies the errata discovered in the XIO2000. These devices are engineering samples only and have not been fully tested or fully characterized. Affected devices are listed in parenthesis.

1. Upstream Memory Write Hang (PG1.0, PG2.0, PG2.1)

Description	The XIO2000 may stop processing upstream memory write transactions using 64-bit addressing if significant back-pressure is created. This back-pressure may be created by delayed flow control updates from the upstream device, delayed Ack responses from the upstream device, or by enabling the Active State Power Management function within the XIO2000.
Impact	The probability of this failure is low since an extended period of back-pressure is required to create this failure.
Workaround	None. When the XIO2000 hangs, a PERST is required to clear this failure.
Course of Action	A solution has been identified and verified. The errata has been fixed on the RTP version of the silicon.

2. Auxiliary Power Detected Status (PG1.0, PG2.0, PG2.1)

Description	In the Device Status Register at offset 9Ah, the Auxiliary Power Detected bit (APD) does not accurately report the state of the $V_{DD\_33\_AUX}$ terminal. This bit always returns a 0b value.
Impact	The system will never detect the presence of the auxiliary power supply. The system impact is low.
Workaround	None.
Course of Action	A solution has been identified and verified. The errata has been fixed on the RTP version of the silicon.

3. ASPM L0's Exit Hang (PG1.0, PG2.0)

Description	In the Link Control Register at offset A0h, the ASLPMC bits should remain in the 00b default state. If the Active State Power Management L0s or L1 entry function is enabled, the XIO2000 may stop processing transactions.
Impact	The system impact is low because the function can remain disabled.
Workaround	None. When the XIO2000 hangs, a PERST is required to clear this failure.
Course of Action	A solution has been identified and verified. The errata will be fixed on the RTP version of the silicon.

4. Common Clock Configuration Status (PG1.0, PG2.0, PG2.1)

Description	In the Link Status Register at offset A2h, the SCC configuration register status bit is inverted. If the REFCLK_SEL terminal is set to common clock mode, this register bit indicates asynchronous clock mode.
Impact	The system impact is low. Based on this status bit, the system may increase the number of FTS sequences during link training. The link training will still complete.
Workaround	None.
Course of Action	A solution has been identified and verified. The errata has been fixed on the RTP version of the silicon.

5. Upstream Memory Write and Invalidate Hang (PG1.0, PG2.0, PG2.1)

Description	The XIO2000 may stop processing upstream memory write and invalidate transactions if significant PCI bus traffic is created for an extended period of time.
Impact	The probability of this failure is low since a high amount of PCI bus traffic is required to create this failure. This failure only occurs with 66 MHz PCI bus master devices.
Workaround	In the Classic PCI Command Register Configuration Space at offset 04h, deassert bit 4 (MWI_ENB). This will prevent the system hang.
Course of Action	A solution has been identified and verified. The errata has been fixed on the RTP version of the silicon.

6. PCI Master Command Timeout (PG1.0, PG2.0, PG2.1)

Description	A PCI master has been identified that illegally issues a command that does not repeat according to PCI bus protocol. According to the PCI bus specification, a PCI command that gets retried must be repeated by the Master. The specific case is an upstream Memory Read command that gets retried by the XIO2000. After the XIO2000 retry, the PCI device responds with a Memory Read Line or a Memory Read Multiple command to the same memory address as the original Memory Read command. When this happens, the XIO2000 holds the completion data in the downstream data buffer until either the discard timer expires or the original Memory Read command is repeated. This retry scenario results in poor PCI bus performance.
Impact	The system impact is moderate. Prior to the expiration of the discard timer, PCI bus performance is poor, but all transactions eventually complete successfully.
Workaround	None.
Course of Action	A solution has been identified and verified. The errata has been fixed on the RTP version of the silicon.

7. Single-Ended PCI-Express Reference Clock (PG1.0)

Description	When the REF_CLK_SEL terminal is asserted high and the 125 MHz single-ended reference clock is selected, the XIO2000 does not link train.
Impact	The system impact is low because there is a work-around.
Workaround	Use a 100 MHz single-ended reference clock.
Course of Action	A solution has been identified and verified. The errata has been fixed on the RTP version of the silicon.

8. Single-Ended PCI-Express Reference Clock (PG2.0)

Description	When the REF_CLK_SEL terminal is asserted high and the 125 MHz single-ended reference clock is selected, the XIO2000 does not link train.
Impact	The system impact is low because there is a work-around.
Workaround	Use a 250 MHz single-ended reference clock.
Course of Action	A solution has been identified and verified. The errata has been fixed on the RTP version of the silicon.

9. REFCLK_DIV_SEL (PG2.0)

Description	PCI clock frequency will operate at incorrect frequency unless REFCLK_DIV_SEL (terminal D17) is pulled low.
Impact	Failure to pull REFCLK_DIV_SEL low will result in PCI clock running at 26.6MHz or 13.3MHz depending on state of M66EN
Workaround	None
Course of Action	A solution has been identified and verified. The errata has been fixed on the RTP version of the silicon.

10. PCI Express Compliance pattern incorrect (PG 3.0)

Description	The compliance pattern generated by the XIO2000 is Incorrect
Impact	In system applications this issue should not be noticeable. Any compliance software that checks compliance pattern may report an error
Workaround	None
Course of Action	A solution has been identified and verified. The errata has been fixed on the RTP version of the silicon.

11. ASPM L0s FTS sync failure (PG 3.0)

Description	When the link of the device upstream of the XIO2000 enters L0s (also L1), the XIO2000 goes into recovery, fails recovery, goes into detect, and eventually retrains the link. This process repeats each time the upstream device's transmitter enters L0s.
Impact	The XIO2000 and all devices downstream will be inaccessible while this continues. Additionally after failing recovery the XIO2000 will undergo a link reset, resetting all non-sticky registers
Workaround	1) Ensure the upstream device's transmitter does not enter L0s. 2) Some chipsets upon reading a minimum exit Latency (<64ns) will disable the upstream device's entry into L0s. By programming the XIO2000 with this minimum L0s exit latency via EEPROM or BIOS it may prevent BIOS from enabling the upstream port's ASPM. This is programmed via register 0xD4 bits 18-16 as all 0 (EEPROM offset 0x8 bits 3-0). Also if enabled, L1 exit latency must be minimized (<1us) via register 0xD4 bits 15-13 as all 0 (EEPROM offset (0x7 bits 7-4)
Course of Action	This issue is expected to be corrected in release silicon.

12. Slow ramp rate on 1.5V rail causes XIO2000 to fail link training (PG1.0, PG2.0, PG2.1, PG3.0)

Description	When the 1.5V power rail ramps too slowly the device fails to link train.
Impact	Devices will fail to link train
Workaround	If the 1.5V rail ramps at a rate of greater than 1.875 V/ms will allow the device to properly function. Also if the 1.5V rail ramps to full value before the 3.3V rail begins to ramp, the device will function properly. Either the 1.5V rail must be ramped in advance of the 3.3V ramp or a voltage regulator that can ensure an appropriate ramp rate for the 1.5V rail must be selected. A TPS72615DCQ is used on XIO2000 EVMs and is known to work for this application
Course of Action	A solution has been identified and verified. The errata has been fixed on the RTP version of the silicon.

13. Data Corruption may occurs when an upstream write burst occurs with data phases where all byte enables disabled followed by a phase where a partial dword is sent (PG1.0, PG2.0, PG2.1, PG3.0)

Description	If an upstream write burst is generated and data phases occur where no data is sent (all byte enables disabled) followed by a data phase with partial data (one or more but not all byte enables enabled), the XIO2000 sends each no-data as a single DWord transaction with all byte enables disabled and the data phase with partial data may then appear at the address 1 DWord prior to the correct address. Subsequent data phases will be sent to the correct address
Impact	The partial DWord of Data will be sent to the previous DWord address resulting in possible incorrect data in the DWord and the prior DWord
Workaround	Disallow data phases where no data is sent (all Byte Enables disabled)
Course of Action	A solution has been identified and verified. The errata has been fixed on the RTP version of the silicon.

14. Receiver may fail to function during link training or when L1 is enabled (PG3.1)

Description	It has been observed that the XIO2000 will sometimes fail to recognize data being received on the receiver. At the time of failure the link will go into the RECOVERY state and the XIO2000 transmitter will transmit the TS1/TS2 ordered set while the receiver is receiving TS1/TS2 ordered sets. Since the XIO2000 fails to recognize the data on its receiver the link will get stuck in the RECOVERY state for a long period of time. Eventually a timeout will occur and the XIO2000 will go back to the DETECT state and the link will retrain and function normally. The link training failure is caused by the receiver elastic buffer locking up (shuttling between 2 states). The failure shows up only when the received data (affecting recovered clock) is stopped and restarted, as during: (a) repetitive resets (including first startup) or (b) L1 shutdown and restart.
Impact	This problem could result in loss of link
Workaround	Do not enable L1
Course of Action	Fix in next revision of silicon

15. When latency for a delayed transaction (IOR/W, MR, MRL, or MRM) is large enough for the discard timer to expire, the XIO2000 will terminate the originating master delay transaction if the discard timer expires in the middle of the transaction. (PG1.0, PG2.0, PG2.1, PG3.0, PG3.1)

Description	Within the XIO2000 there are two discard timers, one for the primary interface and other for the secondary interface. The default setting for these timers is 2^15 PCI clocks. Some BIOS's will program this timer to a smaller value (2^10 clocks for example). These timers can be changed by modifying bits 8 and 9 in the Bridge Control Register. With the smaller discard timer value, if a delayed transaction's latency is large enough the discard timer status bit will get set indicating that the discard timer expired. When the discard timer expires, the XIO2000 will flush the delayed transaction from its buffer. Now if the originating master of the delayed transaction is active on the bus at the same time the discard timer expires, the XIO2000 will flush the buffer and will thereby pull TRDY# away. This TRDY# wait state will last for an indefinite period of time.
Impact	A PCI master may fail to function if it does not retry a

	delayed transaction within the timeout period (or is prevented from doing so by another device that does not release the bus during this entire timeout period).
Workaround	Leaving the discard timer at the default value or increasing the discard timer will prevent the problem from happening.
Course of Action	Fix in next revision of silicon

16. Link Number field is only a 5 bit field instead of 8 bits (PG1.0)

Description	If a root port sends a link number in a training sequence ordered set that is greater than 31, the XIO2000 will send back the wrong sequence number. The bit field for Link Number is only 5 bits instead of 8 bits.
Impact	Most root ports do not use a Link Number greater than 31 so the likely hood of this problem occurring is very low.
Workaround	None
Course of Action	A solution has been identified and verified. The errata has been fixed on all PG versions after PG1.0.

17. A Receiver Overflow Error may occur if certain conditions are met (PG1.0, PG2.0, PG2.1, PG3.0, PG3.1, PG3.2)

Description	If a downstream PCIe memory write with data payload less than or equal to 3 dwords to a PCI device gets Master Aborted by the PCI device and the very next PCIe transaction is a non-posted transaction then the XIO2000 will return 1 extra posted header and extra data posted credits equivalent to the number of dwords in the payload. Eventually these extra returned credits will result in a receiver overflow error. Other PCIe transactions following a Master Aborted memory write will not result in this erratum occurring.
Impact	A PCI memory write that gets master aborted is in itself an error condition that should not occur under normal operating conditions so the likely hood of this problem ever occurring is almost non-existent.
Workaround	A) correct the error condition that is causing the Master Abort condition on the PCI bus. B) follow a Master Aborted PCI transaction by a posted write that will not get Master Aborted before sending a non-posted transaction.
Course of Action	A solution has been identified and verified.

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Mailing Address: Texas Instruments
Post Office Box 655303
Dallas, Texas 75265