DS80PCI800EVK User Guide
4 Channels SMA Evaluation Kit

General Description:
The DS80PCI800EVK is a 4 channel SMA evaluation kit. It provides a complete high bandwidth platform to evaluate the signal integrity and signal conditioning features of the Texas Instruments DS80PCI800SQ – 2.5 Gbps / 5.0 Gbps / 8.0 Gbps 8 Channel PCI Express Repeater with Equalization and De-Emphasis.

Features:
- 8 channel PCIe repeater up to 8 Gbps (GEN 3)
- Low power consumption, with option to power down unused channels
- Adjustable receive equalization
- Adjustable transmit VOD and De-emphasis
- IDLE detection — squelch function auto mutes the output
- Programmable via pin selection or SMBus interface
- Single supply operation: VIN = 3.3V±10% or VDD = 2.5V ±5%
- -40°C to +85°C Operation
- >6 kV HBM ESD Rating
- High speed signal flow–thru pin-out package - SQA54A: 54-pin LLP (10 mm x 5.5 mm, 0.5 mm pitch)

Applications:
- FR-4 Backplane Traces and High Speed Cable for PCIe GEN 3

DS80PCI800EVK Demo Kit Contents:
- End User License Agreement
- DS80PCI800EVK User Guide Rev 1.2
- DS80PCI800EVK Board

Ordering Information:
DEVICE: DS80PCI800SQE: QTY = 250, DS80PCI800SQ: QTY = 2,000
SMA Evaluation Kit: DS80PCI800EVK

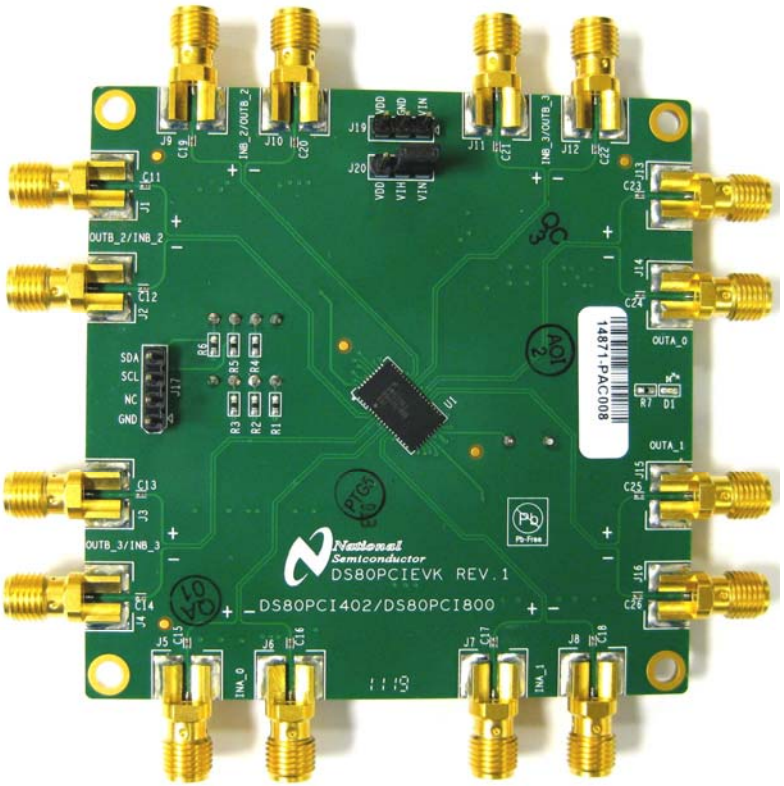

Figure 1. DS80PCI800EVK (TOP VIEW)

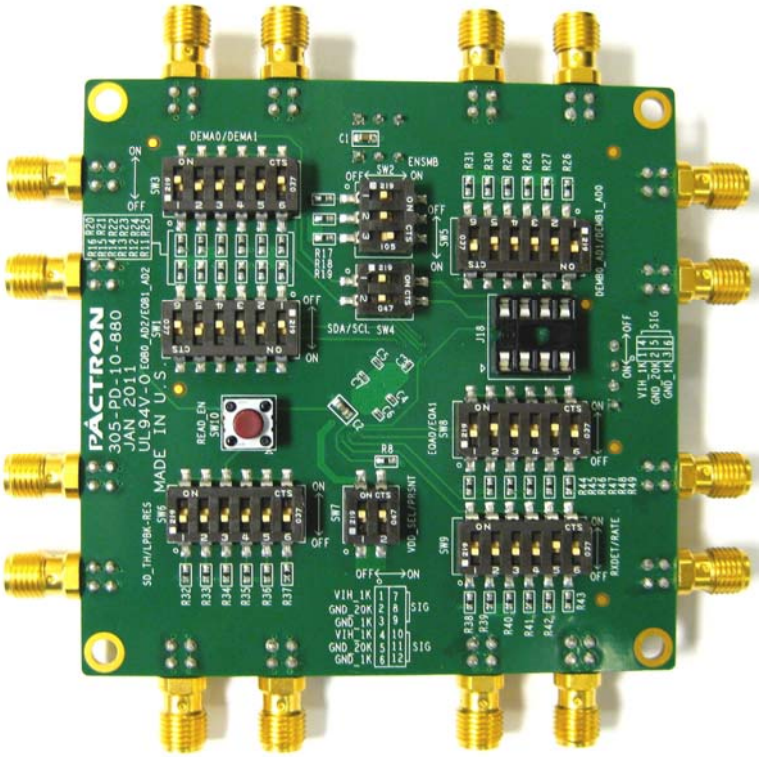

Figure 2. DS80PCI800EVK (BOTTOM VIEW)

Table 1. Switches to set the 4-level input control pins

4 – level Input Settings	Setting for 3 pin switches (3-2-1)
0 – Tie 1k ohm to GND	**ON** – OFF – OFF
R – Tie 20k ohm to GND	OFF – **ON** – OFF
F – FLOAT (open)	OFF – OFF – OFF
1 – Tie 1k ohm to VIH	OFF – OFF – **ON**

The following switches are used to set the input condition for the 4-level inputs:
SW1, SW2, SW3, SW5, SW6, SW8, SW9.
There are 3 switches connected to an input signal pin. Each switch when set to the ON position sets the pin to one of the 4-level setting. The 6 pin switches are assigned similar to the 3 pin switches. The only difference is 2 signal pins are connected and thus 6-5-4 is for the one signal pin and 3-2-1 is for another signal pin. Please note only 1 switch at the ON position is allowed.

Table 2. Connection and Control Description

Component	Name	Function
J1 to J8	IN_B2+, IN_B2-, IN_B3+, IN_B3-, IN_A0+, IN_A0-, IN_A1+, IN_A1-	High speed differential inputs.
J9 to J16	OUT_B2+, OUT_B2-, OUT _B3+, OUT_B3-, OUT _A0+, OUT_A0-, OUT _A1+, OUT_A1-	High speed differential outputs.
J19	VIN or VDD	DC Power – VIN or VDD to DS80PCI800SQ
J20	VIN or VDD	Jumper – VIN or VDD to VIH power
J17	SDA, SCL	Optional SMBUS access pins. See the datasheet for additional information on SMBUS.
J18	EEPROM	Optional socket for EEPROM
SW1	EQB[1:0] or AD[3:2]	PIN MODE – EQ control for channel B inputs SMBUS MODE – AD[3:2] device address bits
SW2	ENSMB	ENSMB = LOW – PIN MODE ENSMB = HIGH – SMBUS (slave mode) ENSMB = FLOAT – SMBUS (master mode – load configuration from EEPROM)
SW3	DEMA[1:0]	PIN MODE – DE control for channel A outputs
SW4	SDA/SCL	“ON” position connects SDA and SCL lines to the device pin.
SW5	DEMB[1:0] or AD[1:0]	PIN MODE – DE control for channel B outputs SMBUS MODE – AD[1:0] device address bits
SW6	SD_TH and LPBK - RES	SD_TH – Signal detect threshold level (FLOAT = Default level) LPBK function for PCI402 and RESERVED for PCI800 (FLOAT = Normal operation)
SW7	VDD_SEL and PRSNT	VDD_SEL – Enable or disable the internal 3.3V to 2.5V regulator. PRSNT – Enable or disable the device (LOW – Enables the device)
SW8	EQA[1:0]	PIN MODE – EQ control for channel A inputs
SW9	RXDET and RATE	RXDET – Input internal 50 ohm to VDD terminations RXDET = F (AUTO RX Detect), RXDET = 1 (50 ohm input termination). RATE = 0 (GEN1,2) = 2.5G / 5.0G. RATE = R (GEN3) = 8.0G. RATE = F (AUTO Detect). The RATE auto detect circuit requires the idle and active signal which occurs during the link training negotiation.
SW10	READ_EN	ENSMB = FLOAT – SMBUS (master mode – load configuration from EEPROM) SW6: SD_TH becomes the READ_EN pin. To start the loading at power up, set SW6 pin 3 to “ON” position (pull to GND). To manually control the start, set SW6 pin 1 to “ON” position (pull to VDD) and push the SW10 button for the high to low transition to start the loading. When the loading is complete the LED – D1 light should turn OFF.

Quick Start User Guide:

1. Connect J19: VIN = 3.3V or VDD = 2.5V and GND.

For VIN = 3.3V:
Set SW7 pin1 (VDD_SEL) to the ON position (enable internal LDO regulator) and float VDD at J19.
For VDD = 2.5V:
Set SW7 pin1 (VDD_SEL) to the OFF positions (disable internal LDO regulator) and float VIN at J19.

2. Set jumper – J20 for VIH connection to VIN or VDD.

3. Connect 50 Ohm SMA cables to the board.

The input signals J1 to J8 can be connected from a pattern generator.
The output signals J9 to J16 can be connected to a scope.
Top 2 – B channel: J1 – IN_B2+, J2 – IN_B2- → J9 – OUT_B2+, J10 – OUT_B2-
J3 – IN_B3+, J4 – IN_B3- → J11 – OUT_B3+, J12 – OUT_B3-
Bottom 2 – A channel: J5 – IN_A0+, J6 – IN_A0- → J13 – OUT_A0+, J14 – OUT_A0-
J7 – IN_A1+, J8 – IN_A1- → J15 – OUT_A1+, J16 – OUT_A1-

4. Set the control pins for normal operation

SW7 – PRSNT = 0 (enables the device): set switch pin2 to the ON position.
SW9 – RXDET = F (continuous receiver detection): set switches (3-2-1) = (OFF-OFF-OFF).
RXDET = 1 (50 ohm input termination): set switches (3-2-1) = (OFF-OFF-**ON**).
SW9 – RATE = F (enable rate detection): set switches (6-5-4) to (OFF-OFF-OFF).
RATE = R (GEN3 mode): set switches (6-5-4) = (OFF-**ON**-OFF).
RATE = 0 (GEN1,2 mode): set switches (6-5-4) = (**ON**-OFF-OFF).
SW6 – SD_TH = F (default signal detect threshold level): set switches (3-2-1) = (OFF-OFF-OFF).
SW6 – LPBK - RES = F (normal operation): set switches (6-5-4) = (OFF-OFF-OFF).

5. Set the input equalization level.

For external pin mode control of the equalization level:
Set ENSMB = 0 (1kohm to GND) by using the SW2 (3-2-1) = (**ON**-OFF-OFF).
SW4 pin1,2 must be set to the OFF positions, so the SMBUS signals are disconnected.
Refer to Table 1 for information on the 3 switch settings for the 4 level input.

Example:
Set EQB[1:0] with SW1 for the B bank of inputs (top 4 inputs of DS80PCI800).
SW1 (6-5-4), (3-2-1) = (OFF-**ON**-OFF), (OFF-**ON**-OFF) = EQB[1:0] = R,R = 14.6 dB at 4 GHz (level 6).
Set EQA[1:0] with SW8 for the A bank of inputs (bottom 4 inputs of DS80PCI800).
SW8 (6-5-4), (3-2-1) = (OFF-**ON**-OFF), (OFF-**ON**-OFF) = EQA[1:0] = R,R = 14.6 dB at 4 GHz (level 6).
The table below is the 16 possible EQ settings when in pin mode.

Level	EQA/B[1:0]	SW1 - EQB[1:0] SW8 - EQA[1:0]						EQ (dB) at 4 GHz
		6	5	4	3	2	1	
1	0, 0	**ON**	OFF	OFF	**ON**	OFF	OFF	4.9
2	0, R	**ON**	OFF	OFF	OFF	**ON**	OFF	7.9
3	0, F	**ON**	OFF	OFF	OFF	OFF	OFF	9.9
4	0, 1	**ON**	OFF	OFF	OFF	OFF	**ON**	11.0
5	R, 0	OFF	**ON**	OFF	**ON**	OFF	OFF	14.3
6	R, R	OFF	**ON**	OFF	OFF	**ON**	OFF	14.6
7	R, F	OFF	**ON**	OFF	OFF	OFF	OFF	17.0
8	R ,1	OFF	**ON**	OFF	OFF	OFF	**ON**	18.5
9	F ,0	OFF	OFF	OFF	**ON**	OFF	OFF	18.0
10	F, R	OFF	OFF	OFF	OFF	**ON**	OFF	22.0
11	F, F	OFF	OFF	OFF	OFF	OFF	OFF	24.4
12	F, 1	OFF	OFF	OFF	OFF	OFF	**ON**	25.8
13	1, 0	OFF	OFF	**ON**	**ON**	OFF	OFF	27.4
14	1, R	OFF	OFF	**ON**	OFF	**ON**	OFF	29.0
15	1, F	OFF	OFF	**ON**	OFF	OFF	OFF	31.4
16	1, 1	OFF	OFF	**ON**	OFF	OFF	**ON**	32.7

6. Set the output VOD and De-emphasis level.

For external pin mode control for the VOD and De-emphasis level (Gen1&2 only):

Set ENSMB = 0 (1kohm to GND) by using the SW2 (3-2-1) = (**ON**-OFF-OFF).
SW4 pin1,2 must be set to the OFF positions, so the SMBUS signals are disconnected.
Refer to Table 1 for information on the 3 switch settings for the 4 level input.

Example:
Set DEMB[1:0] with SW5 for the B bank of outputs (top 4 outputs of DS80PCI800).
SW5 (6-5-4), (3-2-1) = (**ON**-OFF-OFF), (OFF-OFF-**ON**) = DEMB[1:0] = 0,1 (VOD=1.0V, DE=0 dB).
Set DEMA[1:0] with SW3 for the A bank of outputs (bottom 4 outputs of DS80PCI800).
SW3 (6-5-4), (3-2-1) = (**ON**-OFF-OFF), (OFF-OFF-**ON**) = DEMA1:0] = 0,1 (VOD=1.0V, DE=0 dB).

The table below is the 16 possible settings of VOD and DE when in pin mode.
In Gen 1/2, the de-emphasis level can be set with the DEMx[1:0] pins, but is not available in Gen 3.

Level	DEMA/B[1:0]	SW5 - DEMB[1:0] SW3 - DEMA[1:0]						GEN1,2 and 3	
		6	5	4	3	2	1	VOD (Vp-p)	DE (dB)
1	0, 0	**ON**	OFF	OFF	**ON**	OFF	OFF	0.8	0
2	0, R	**ON**	OFF	OFF	OFF	**ON**	OFF	0.9	0
3	0, F	**ON**	OFF	OFF	OFF	OFF	OFF	0.9	-3.5
4	0, 1	**ON**	OFF	OFF	OFF	OFF	**ON**	1.0	0
5	R, 0	OFF	**ON**	OFF	**ON**	OFF	OFF	1.0	-3.5
6	R, R	OFF	**ON**	OFF	OFF	**ON**	OFF	1.0	-6
7	R, F	OFF	**ON**	OFF	OFF	OFF	OFF	1.1	0
8	R ,1	OFF	**ON**	OFF	OFF	OFF	**ON**	1.1	-3.5
9	F ,0	OFF	OFF	OFF	**ON**	OFF	OFF	1.1	-6
10	F, R	OFF	OFF	OFF	OFF	**ON**	OFF	1.2	0
11	F, F	OFF	OFF	OFF	OFF	OFF	OFF	1.2	-3.5
12	F, 1	OFF	OFF	OFF	OFF	OFF	**ON**	1.2	-6
13	1, 0	OFF	OFF	**ON**	**ON**	OFF	OFF	1.3	0
14	1, R	OFF	OFF	**ON**	OFF	**ON**	OFF	1.3	-3.5
15	1, F	OFF	OFF	**ON**	OFF	OFF	OFF	1.3	-6
16	1, 1	OFF	OFF	**ON**	OFF	OFF	**ON**	1.3	-9

For SMBUS mode control of the EQ, VOD and De-emphasis level:

Set ENSMB = 1 (1kohm to VIH) by using the SW2 (3-2-1) = (OFF-OFF-**ON)**.
Set SW4 pin1,2 to the ON position so the SMBUS signals are connected.
Set SW3 pin1 thru pin6 switches to the OFF position so they do not connect to the SDA and SCL line.
Set the SW1 and SW5 for the AD[3:0] pins. AD[3:0]=0000 sets device slave address = B0'hex.
Connect SDA, SCL and GND to J17. Please refer to datasheet for register map for EQ, VOD and DEM.

Bill of Materials for DS80PCI800EVK:

Item	Qty	Reference	Digikey PN	Manufacture PN	Descriptions
1	1	C1	445-3448-1-ND	C1608Y5V0J106Z	CAP CER 10UF 6.3V Y5V 0603
2	1	C2	445-1322-1-ND	C1608X5R0J105K	CAP CER 1.0UF 6.3V X5R 10% 0603
3	1	C3,C4,C5,C6,C7	445-4711-1-ND	C0603X5R0J104M	CAP CER .10UF 6.3V X5R 0201
4	16	C11,C12,C13,C14,C15,C16	587-2483-1-ND	LMK063BJ224MP-F	CAP CER .22UF 10V X5R 20% 0201
		C17,C18,C19,C20,C21,C22,			
		C23,C24,C25,C26			
5	1	D1	511-1592-1-ND	SML-P12PTT86	LED GREEN 0.2MM 13MCD 0402 SMD
6	16	J1,J2,J3,J4,J5,J6,J7,J8,	J801-ND	142-0761-881	CONN JACK SMA 50 OHMS PC MOUNT
		J9,J10,J11,J12,J13,J14,			
		J15,J16			
7	1	J17	WM6504-ND	22-28-4043	CONN HEADER 4POS .100 VERT GOLD
8	2	J19,J20	WM6503-ND	22-28-4033	CONN HEADER 3POS .100 VERT GOLD
9	1	J18	3M5473-ND	4808-3004-CP	SOCKET IC OPEN FRAME 8POS .3"
10	31	R1,R2,R3,R4,R8,R11,R13,	P1.00KLCT-ND	ERJ-2RKF1001X	RES 1.00K OHM 1/10W 1% 0402 SMD
		R14,R16,R17,R19,R20,R22,			
		R23,R25,R26,R28,R29,R31,			
		R32,R34,R35,R37,R38,R40,			
		R41,R43,R44,R46,R47,R49			
11	1	R7	P220LCT-ND	ERJ-2RKF2200X	RES 220 OHM 1/10W 1% 0402 SMD
12	13	R12,R15,R18,R21,R24,R27,	P20.0KLCT-ND	ERJ-2RKF2002X	RES 20.0K OHM 1/10W 1% 0402 SMD
		R30,R33,R36,R39,R42,R45,			
		R48			
13	2	R5,R6	P4.70KLCT-ND	ERJ-2RKF4701X	RES 4.70K OHM 1/10W 1% 0402 SMD
14	6	SW1,SW3,SW5,SW6,SW8, SW9	CT2196MST-ND	219-6MST	SWITCH TAPE SEAL 6 POS SMD
15	1	SW2	CT2193MST-ND	219-3MST	SWITCH TAPE SEAL 3 POS SMD
16	2	SW4,SW7	CT2192MST-ND	219-2MST	SWITCH TAPE SEAL 2 POS SMD
17	1	SW10	P12225SCT-ND	EVQ-21505R	SWITCH LT 6MM 160GF 5MM HEIGHT
18	1	U1	NA	DS80PCI800SQ	PCIE REPEATER

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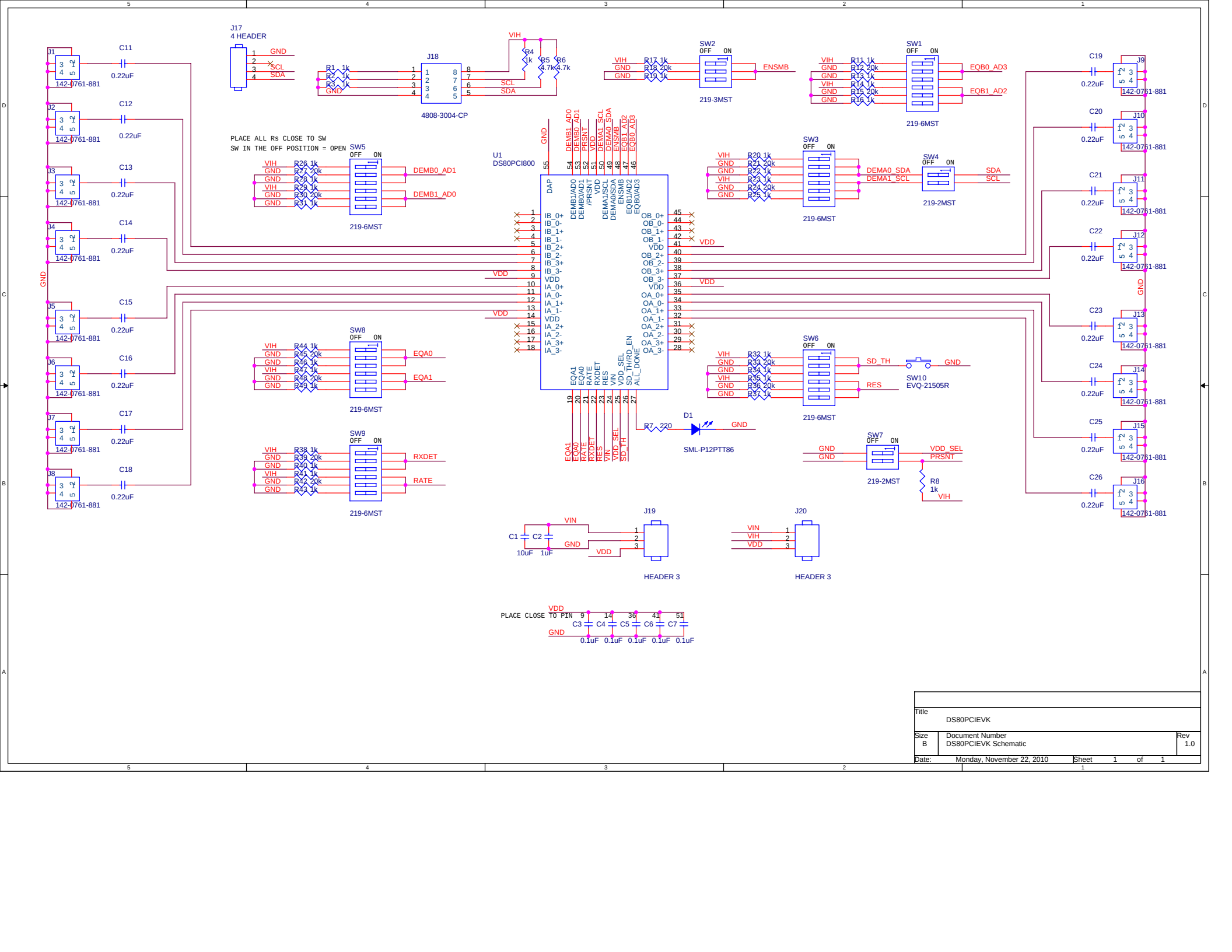
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4 HEADER
GND
SCL
SDA
J18
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R1 1k
R2 1k
R3 1k
R4 1k
R5 4.7k
R6 4.7k
VIH
SCL
SDA
SW2
OFF ON
219-3MST
ENSMB
SW1
219-6MST
EQB0_AD3
EQB1_AD2
PLACE ALL Rs CLOSE TO SW
SW IN THE OFF POSITION = OPEN
SW5
219-6MST
DEMB0_AD1
DEMB1_AD0
U1
DS80PCI800
SW3
219-6MST
SW4
219-2MST
DEMA0_SDA
DEMA1_SCL
SDA
SCL
SW8
219-6MST
EQA0
EQA1
SW9
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RXDET
RATE
SW6
219-6MST
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RES
SW10
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D1
SML-P12PTT86
R7 220
SW7
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VDD_SEL
PRSNT
R8 1k
J1
J2
J3
J4
J5
J6
J7
J8
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C12
C13
C14
C15
C16
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C21
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C24
C25
C26
J9
J10
J11
J12
J13
J14
J15
J16
J19
HEADER 3
J20
HEADER 3
C1 10uF
C2 1uF
PLACE CLOSE TO PIN
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C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
Title
DS80PCIEVK
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DS80PCIEVK Schematic
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