When selecting the external components, it is important have in mind the current drawn from the ADC input. The input impedance of the ADC has been simulated to 197kΩ.

**Decoupling capacitor**

Assuming the input from the resistive ladder is a perfect open circuit and is not supplying any current, the average voltage across the capacitor C151 should not drop more than 0.5VLSB during the maximum number of conversions, which is when a decimation rate 512 is used (12ENOB).

The voltage that is input to the ADC can be calculated by looking at the charge transfer during each of the samples:

Assuming the external capacitor Cext is fully charged to the voltage Vi,0, the initial charge on this capacitor can be written as. The simulated input impedance of 197kΩ is at a sampling frequency of 4 Mhz equivalent to an internal switched capacitance Cint with the value:



Assuming that the internal capacitor Cint is fully discharged between each sequential sample, the voltage Vi,1 on the ADC input after one single sample (of N samples) is found as:



Continuing this series we see that the ADC input voltage after n samples is found as:



The average input voltage Vin,avg calculated by the decimation filter after N samples will then be:



This geometric series has a result given as:



Table ‎6‑3 summarizes a simulation of the capacitor value needed to avoid an average voltage error >0.5VLSB when using a decimation rate of N=512 for given accuracies.

The results comes from simulation in MATLAB with Vref=1.15V and the initial voltage Vi on the ADC input as 1.1V. The simulation assumes that no current is delivered from the resistive ladder.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Accuracy(Bits) | 12 | 11 | 10 | 9 | 8 | 7 |
| Vaverage(N=512) | 1.09986 | 1.09972 | 1.09944 | 1.09888 | 1.09775 | 1.09547 |
| Capacitance(F) | 2.56u | 1.28u | 640n | 320n | 160n | 80n |

Table ‑. Accuracy vs. decoupling capacitor value

As seen above, quite large decoupling capacitors are needed to maintain the accuracy that the ADC is capable of delivering.

**Resistive ladder**

The resistive ladder is mainly used to divide down the battery voltage below the internal reference. It is desirable to maximize the resistance values in order to minimize the power consumption, but it is important to keep in mind that the decoupling capacitor must be fully recharged between each conversion to yield correct ADC results.

The components C151, R152 and R153 in Figure ‎6‑1 will act as a RC filter when C151 is recharged after an ADC conversion is complete. The differential equation for the ADC input voltage Vi is found with Kirchoff’s Current Law as (ignoring parasitic effects):



Naming the initial value Vi(t=0) as Vi0, the solution of the equation is found as:



As an example, consider the case when C151=160nF, R152=2MΩ, R153=1MΩ and VDD=3.3V, which will give Vi =1.1V. The quiescent current of the ladder will then be 1.1µA. Using the assumptions and values from Table ‎6‑3, the initial value on the ADC input after a conversion is done will be Vi0 =1.09775V. If you want to wait until the voltage Vi is within the 12 bit accuracy value again, this will take 296ms!

For many applications, this time limit is not a concern. However if it is, one should consider implementing a solution where resistive voltage division is not needed.

Another alternative is utilizing a switch to eliminate current being drawn outside the conversion periods together with a low resistance ladder which will supply the ADC inputs and charge the decoupling capacitor faster.

C

151

1

NC

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NC

3

NC

4

NC

5

P

1

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5

**CC**

**2530**

DIE ATTACH PAD

:

10

DVDD

2

9

P

1

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1

8

P

1

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2

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1

\_

3

6

P

1

\_

4

RBIAS

30

AVDD

4 29

AVDD

1 28

AVDD

2 27

RF

\_

N

26

AVDD

5 21

XOSC

\_

Q

1 22

XOSC

\_

Q

2 23

AVDD

3 24

RF

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P

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P

1

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0

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**LDO**

VBATT

R

152

R

153

Figure ‑. CC2530 powered by LDO with example ADC connection