1.1 RSSI

The AGC module returns an estimate on the signal strength received at the antenna called RSSI (Received Signal Strength Indicator). The RSSI is a 12 bits two's complement number with 0.0625 dB resolution hence ranging from –128 to 127 dBm. A value of –128 dBm indicates that the RSSI is invalid. The RSSI can be found by reading `RSSI1.RSSI_11_4` and `RSSI0.RSSI_3_0`. It should be noted that for most applications using the 8 MSB bits of the RSSI, with 1 dB resolution, is good enough.

To get a correct RSSI value a calibrated RSSI offset value should be subtracted from the value given by `RSSI[11:0]`. The RSSI offset value can be found by input a signal of known strength to the radio when `AGC_GAIN_ADJUST.GAIN_ADJUSTMENT` is 0x00.

Example:

Assume a -70 dBm signal into the antenna and `RSSI[11:0] = 0x200` (32) when `AGC_GAIN_ADJUST.GAIN_ADJUSTMENT = 0x00`.

This means that the offset is 102 dB as 32 dBm – 102 dB = –70 dBm.

When the offset is known it can be written to the `AGC_GAIN_ADJUST.GAIN_ADJUSTMENT` register field (`GAIN_ADJUSTMENT = 0x9A` (102)). When the same signal is input to the antenna, the `RSSI[11:0]` register will be 0xBA0 (-70).

The RSSI value is output from a configurable moving average filter in order to reduce uncertainty in the RSSI estimates. It is as such possible to trade RSSI computation speed/update rate against RSSI accuracy. This trade-off is determined by configuring the `AGC_CFG0.RSSI_VALID_CNT` register. This register field gives the number of new input samples to the moving average filter (internal RSSI estimates) that are required before the next update of the RSSI value[1]. The `RSSI_VALID` signal will be asserted from the first RSSI update. `RSSI_VALID` is available on a GPIO by setting `IOCFGx.GPIOx_CFG = RSSI_VALID` (13) or can be read from the `RSSI0` register.

Carrier Sense (CS) indication will also be affected by the setting of `AGC_CFG0.RSSI_VALID_CNT`. After the RSSI is valid it will be continuously compared to the CS threshold set in the `AGC_CS_THR` register, but since the RSSI update rate is given by the `RSSI_VALID_CNT` register field, this will in practice limit the CS update rate as well. The exception is when the CS threshold is changed while in RX mode. The `CARRIER_SENSE` signal will then be updated immediately (if needed). Figure 1 shows when CS is updated with respect to the RSSI.

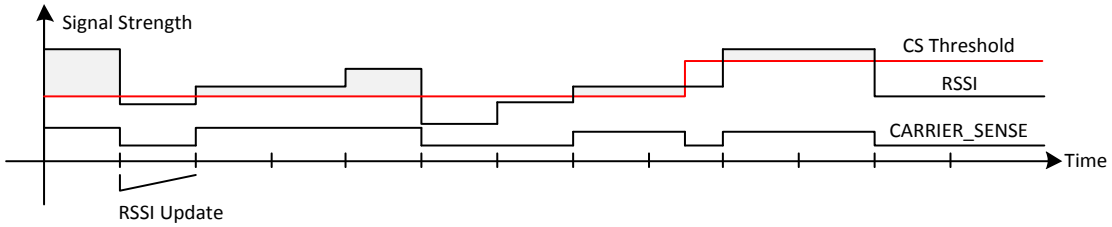

Figure 1: CS vs. RSSI_UPDATE

Figure 2 shows an example of the behavior of RSSI specific signals given two different values for the `AGC_CFG0.RSSI_VALID_CNT` register value (00b and 10b).

[1] By setting the `IOCFG3.GPIO3_CFG` or `IOCFG2.GPIO2_CFG = RSSI_UPDATE` (14), a pulse will occur on GPIO3 or GPIO2 each time the RSSI value is updated

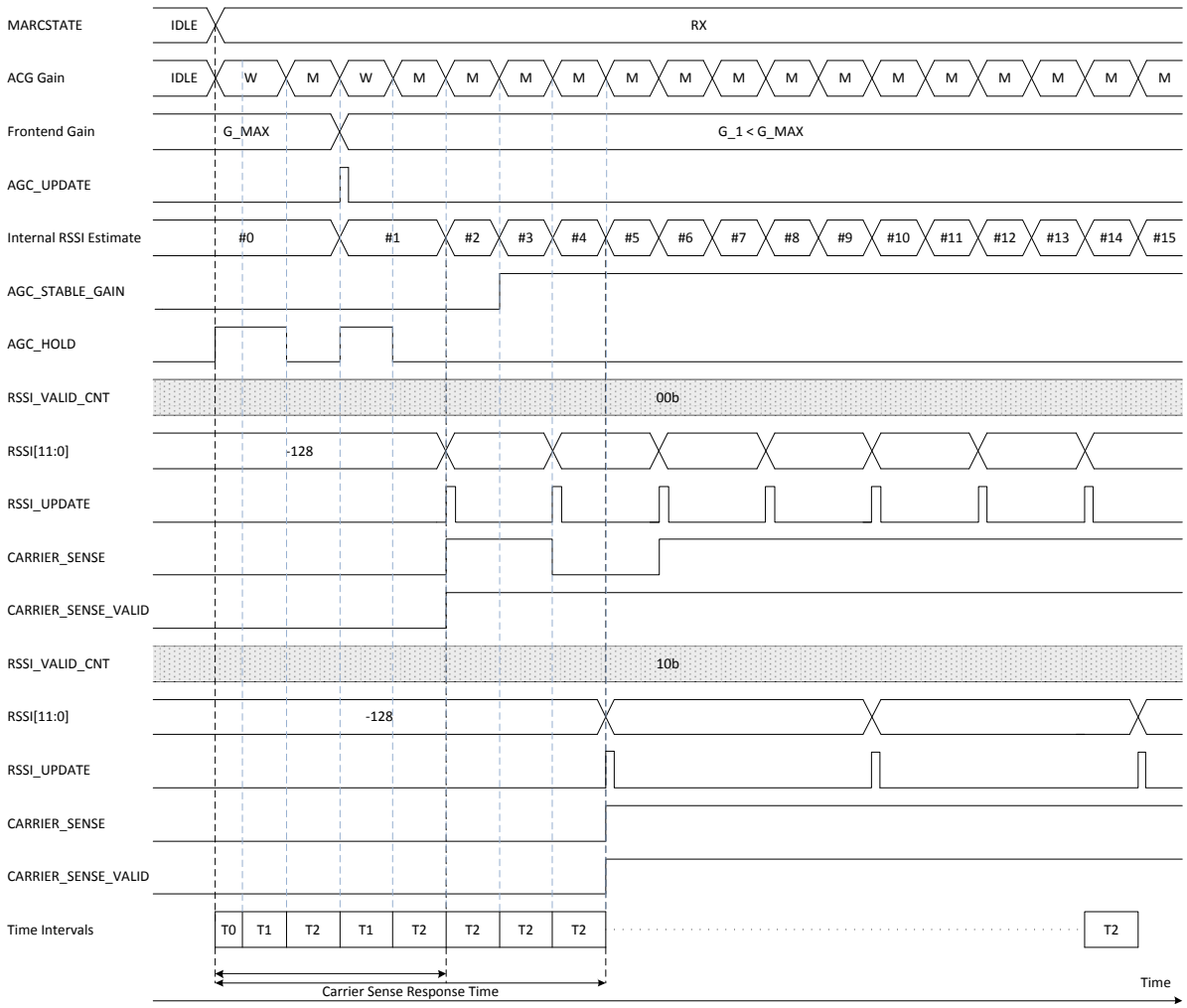

Figure 2: RSSI/CS Timing Diagram

T0: Start-up delay before RSSI measurements can begin. This delay is dependent on demodulator settings and can be found using Table 1, Table 2, and Equation 3.

T1: The time the AGC waits after adjusting the front end gain to allow signal transients to decay before the next signal strength measurement can take place. T1 can be calculated using Equation 1.

T2: The time the AGC uses to measure the signal strength and potentially adjust the gain. T2 can be calculated using Equation 2.

The CS response time is the time it takes before `CARRIER_SENSE_VALID` is asserted. This is the maximum time the radio will be in RX state when RX termination based on CS is enabled. The CS response time is given by Equation 4.

Figure 2 shows an example of how RSSI computation speed/update rate can be traded against RSSI accuracy. In the case where `AGC_CFG0.RSSI_VALID_CNT = 00b` the number of new input samples to the moving average filter is 2, making the CS response time short but might lead to a less robust CS indication on the second RSSI update. In the case where `AGC_CFG0.RSSI_VALID_CNT = 10b` (5 samples) there are no failing CS, but the response time is longer.

`BB_CIC_DECFACT`[2] is found in register `CHAN_BW` while `AGC_SETTLE_WAIT` and `AGC_WIN_SIZE` register fields are found in the `AGC_CFG1` register. `CARRIER_SENSE_GATE` is found in `MDMCFG1` and

[2] If `BB_CIC_DECFACT` = 0, use a value of 1

DCFILT_FREEZE_COEFF is found in DCFILT_CFG. The decimation factor is 20 or 32, given by the CHAN_BW.ADC_CIC_DECFACT register field.

$$T1 = \frac{(16 \cdot \text{AGC\_SETTLE\_WAIT} + 48) \cdot \text{BB\_CIC\_DECFACT} \cdot \text{Decimation Factor}}{f_{XOSC}}$$

Equation 1: T1

$$T2 \leq \frac{2^{\text{AGC\_WIN\_SIZE}+4} \cdot \text{BB\_CIC\_DECFACT} \cdot \text{Decimation Factor} + 46}{f_{XOSC}}$$

Equation 2: T2

Configuration Register Fields/Conditions		T0
CHAN_BW.CHFILT_BYPASS	CHAN_BW.BB_CIC_DECFACT > 0x01	
0	0	$D_0 + D_2 + D_4 + D_5$
0	1	$D_0 + D_1 + D_3 + D_5$
1	0	D_0
1	1	$D_0 + D_1 + D_6$

Table 1: T0 Matrix

Delay	Equation
D_0	$\frac{16 \cdot \text{Decimation Factor} + 74}{f_{XOSC}}$
D_1[3]	$\frac{(1 - DCFILT\_FREEZE\_COEFF) \cdot (62 + CARRIER\_SENSE\_GATE \cdot (2^{(5+x)} - 1)) \cdot \text{Decimation Factor} \cdot 2}{f_{XOSC}}$
D_2[3]	$\frac{(62 + CARRIER\_SENSE\_GATE \cdot (2^{(5+x)} - 1)) \cdot \text{Decimation Factor} \cdot 2}{f_{XOSC}}$
D_3	$\frac{(16 \cdot BB\_CIC\_DECFACT - 2) \cdot \text{Decimation Factor} \cdot 2}{f_{XOSC}}$
D_4	$\frac{(35 - DCFILT\_FREEZE\_COEFF) \cdot \text{Decimation Factor} \cdot 2}{f_{XOSC}}$
D_5	$\frac{68 \cdot BB\_CIC\_DECFACT \cdot \text{Decimation Factor}}{f_{XOSC}}$
D_6	$\frac{(BB\_CIC\_DECFACT - 2) \cdot \text{Decimation Factor} \cdot 2}{f_{XOSC}}$

Table 2: D_0 - D_6

$$T0 \leq \sum Applicable\ Delays\ |_{\text{Current Configuration}}$$

Equation 3: T0

[3] x = DCFILT_CFG.DCFILT_BW when DCFILT_CFG.DCFILT_BW < 5, else it is 4

The maximum carrier sense response time is given by Equation 4.

$$\text{CS Response Time} \le T0 + (T1 + T2) \cdot (2^{RSSI\_VALID\_CNT} + 1)$$

Equation 4: Max CS Response Time

If number of `AGC_UPDATE` pulses before the first RSSI update is known, the CS response time is given by Equation 5, where x = # of `AGC_UPDATE` pulses before first `RSSI_UPDATE`.

$$\text{CS Response Time} \le T0 + T1 \cdot (x + 1) + T2 \cdot (2^{RSSI\_VALID\_CNT} + 1)$$

Equation 5: CS Response Time (# of gain reductions is known)

In cases where `AGC_CFG1.AGC_SYNC_BEHAVIOR` is set to freeze the RSSI value after a sync word is detected, it is important that preamble and sync word is long enough so that the RSSI represent the RSSI of the packet and not of noise received prior to the preamble.

Assume a data rate of 1.2 ksps and the following register configurations:

`CHAN_BW.ADC_CIC_DECFACT` = 0

`CHAN_BW.BB_CIC_DECFACT` = 8

`AGC_CFG1.AGC_WIN_SIZE` = 2

`AGC_CFG0.RSSI_VALID_CNT` = 3

`AGC_CFG1.SETTLE_WAIT` = 1

Equation 4 can be used to find the max RSSI update rate. For this example it is assumed that the radio has been in RX for some time before a packet is received so T0 can be ignored.

$$\text{RSSI Update Rate} \le (T1 + T2) \cdot (2^{RSSI\_VALID\_CNT} + 1)$$

$$\text{T1} = \frac{(16 \cdot \text{AGC\_SETTLE\_WAIT} + 48) \cdot \text{BB\_CIC\_DECFACT} \cdot \text{Decimation Factor}}{f_{XOSC}} = \frac{(16 \cdot 1 + 48) \cdot 8 \cdot 20}{32 \cdot 10^6} = 320\ \mu s$$

$$\text{T2} \le \frac{2^{\text{AGC\_WIN\_SIZE}+4} \cdot \text{BB\_CIC\_DECFACT} \cdot \text{Decimation Factor} + 46}{f_{XOSC}} = \frac{2^{2+4} \cdot 8 \cdot 20 + 46}{32 \cdot 10^6} = 321.44\ \mu s$$

$$\text{RSSI Update Rate} \le (320 + 321.44) \cdot (2^3 + 1) = 5.77\ ms$$

To guarantee that the RSSI measurement is done during the packet and not on noise, preamble + sync word should be greater than twice the RSSI update rate.

With a data rate of 1.2 ksps this means that a minimum of 28 bits preamble/sync must be received for the RSSI readout to be correct. For this example it is assumed that the radio has been in RX for a time longer than the max CS response time (see Equation 4) when the preamble and sync word is received.