

// Init Timer-Base Control Register for EPWM1-EPWM3

EPwm1Regs.TBCTL.bit.FREE\_SOFT = SOFT\_STOP\_FLAG;

EPwm1Regs.TBCTL.bit.PHSDIR = PHSDIR\_CNT\_UP;

EPwm1Regs.TBCTL.bit.CLKDIV = CLKDIV\_PRESCALE\_X\_1;

EPwm1Regs.TBCTL.bit.HSPCLKDIV = HSPCLKDIV\_PRESCALE\_X\_1;

EPwm1Regs.TBCTL.bit.SYNCOSEL = 1; //send synch down stream

EPwm1Regs.TBCTL.bit.PRDLD = 1; //0-shadow mode, 1-immidiate mode

EPwm1Regs.TBCTL.bit.PHSEN = 0; //no sync, make this pwm master

EPwm1Regs.TBCTL.bit.CTRMODE = TIMER\_CNT\_UP;

EPwm2Regs.TBCTL.bit.FREE\_SOFT = SOFT\_STOP\_FLAG;

EPwm2Regs.TBCTL.bit.PHSDIR = PHSDIR\_CNT\_UP;

EPwm2Regs.TBCTL.bit.CLKDIV = CLKDIV\_PRESCALE\_X\_1;

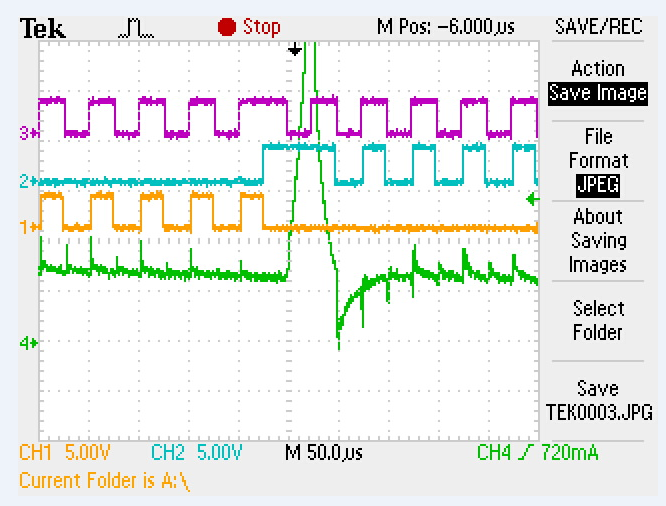
EPwm2Regs.TBCTL.bit.HSPCLKDIV = HSPCLKDIV\_PRESCALE\_X\_1;

EPwm2Regs.TBCTL.bit.SYNCOSEL = 0; //sync to master

EPwm2Regs.TBCTL.bit.PRDLD = 1; //0-shadow mode, 1-immidiate mode

EPwm2Regs.TBCTL.bit.PHSEN = 1; //sync enable

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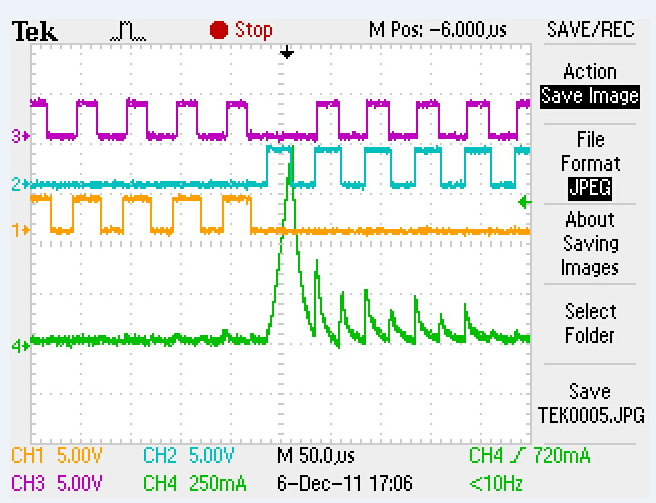
EPwm2Regs.TBCTL.bit.CTRMODE = TIMER\_CNT\_UP;

//And resetting counter in ISR, in every commutation state

EPwm1Regs.TBCTR = 0;

EPwm2Regs.TBCTR = 0;

EPwm3Regs.TBCTR = 0;



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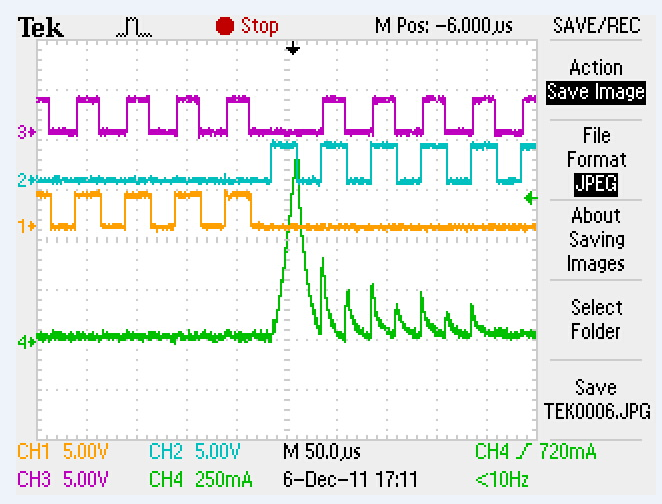
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