bq20z80

Application Book

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TEXAS INSTRUMENTS

Contents

Chapter 1

Impedance Track™ Gas Gauge for Novices

PMP Portable Power

ABSTRACT

This application report introduces the bq20z80 Impedance Track™ and bq29312A chipset gas gauge solution.

1.1 Introduction

This application report provides an introductory overview of the following bq20z80 Impedance Track™ gas gauge topics:

- The Basics
  - The bq20z80 Impedance Track™ Gas Gauge Overview
  - Impedance Track™ Technology Operation Principle
  - Gas Gauge Hardware
    - bq29312A Analog Front-End Protector
    - How the bq20z80 and bq29312A Operate Together
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1.2 The Basics

bq20z80 Impedance Track™ Gas Gauge Overview

1.2.1.1 Key Features:

- Patented Impedance Track™ technology accurately measures available charge in Li-ion and Li-polymer batteries.
- Better than 1% capacity estimate error over the lifetime of the battery
- Instant capacity estimate accuracy – no learning cycle required
- Supports the Smart Battery Specification SBS V1.1
- Works with the TI bq29312A analog front-end (AFE) protection IC to provide a complete pack electronics solution
- Full array of programmable voltage, current, and temperature protection features
- Integrated time base removes need for external crystal with optional crystal input
- Supporting 2-, 3-, and 4-cell battery packs with few external components
- Based on a powerful low-power RISC CPU core with high-performance peripherals
- Integrated, field-programmable FLASH memory eliminates the need for external configuration memory
- Measures charge flow using a high-resolution, 16-bit integrating delta-sigma converter
- Uses 16-bit delta-sigma converter for accurate voltage and temperature measurements
- Extensive data reporting options for improved system interaction
- Optional pulse charging feature for improved charge times
- Drives 3-, 4-, or 5-segment LED display for remaining capacity indication
- Optional cell-balancing feature for increased battery life

The bq20z80 is an advanced, SBS v1.1-compliant, feature-rich battery gas gauge IC, designed for accurate reporting of available charge of Li-ion or Li-polymer batteries. The bq20z80 incorporates the patented Impedance Track™ technology, whose unique algorithm allows for real-time tracking of battery capacity change, battery impedance, voltage, current, temperature, and other critical information of the battery pack. Unlike the *current integration*- or *voltage correlation*-based gas gauge algorithms, the Impedance Track™ algorithm takes full advantage of battery response to electronic and thermal stimuli and therefore maintains the best capacity estimate accuracy over the lifetime of the battery. The bq20z80 automatically accounts for charge and discharge rate, self-discharge, and cell aging, resulting in excellent gas-gauging accuracy even when the battery ages. The IC also provides a variety of battery performance parameters to a system host over a standard serial communication bus (SMBus).

The heart of the bq20z80 programmable battery management IC is a high-performance, low-power, reduced instruction-set (RISC) CPU, which offers powerful information processing capability that is crucial to battery management functional calculation and decision-making. The IC also integrates plenty of program and data flash memory and an array of peripheral and communication ports, facilitating rapid development of custom implementations and eliminating the need for external configuration memory.

The bq20z80 is equipped with two high-resolution, analog-to-digital converters (ADC) dedicated for accurate coulomb counting and voltage/temperature measurements. These low-power analog peripherals improve accuracy beyond discrete implementations. The bq20z80 is designed to work with the bq29312A analog front-end (AFE) protection IC to provide a complete pack electronics solution. Figure 1 shows a simplified system diagram of a typical multicell gas-gauging solution consisting of the bq20z80 and the bq29312A. The main task of the AFE bq29312A is to provide safety protection of overcharge, overload, and short-circuit of the battery. The AFE can be configured to autonomously shut off the FET drives at overload or short-circuit conditions. In addition, the AFE serves as a voltage translator for the bq20z80 gas gauge IC, providing individual cell or battery voltages to the gas gauge IC. In case of overvoltage and undervoltage conditions as detected by the gas gauge IC, the AFE performs actions such as turning on/off charge/discharge FETs as instructed or programmed by the gas gauge IC.

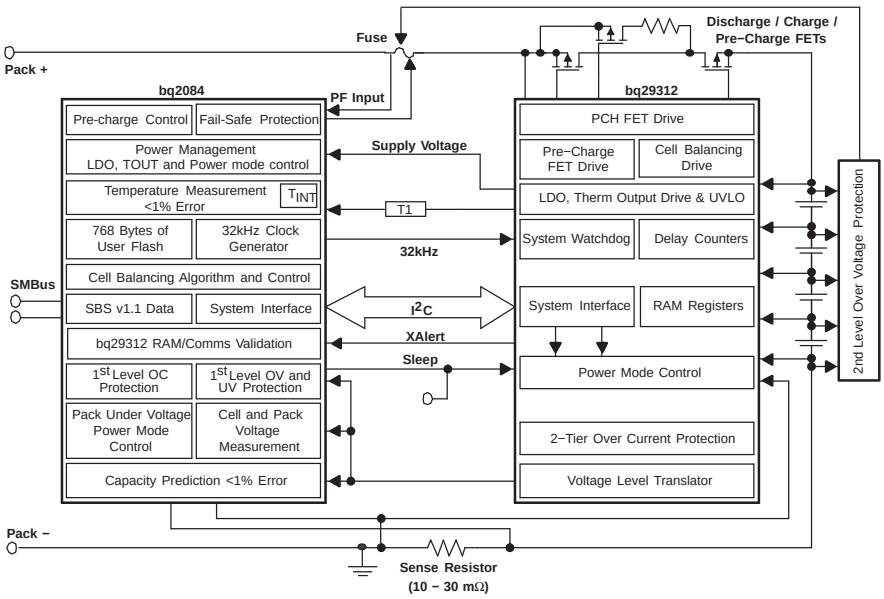


Figure 1. Battery Management Unit Block Diagram

The bq20z80 measures individual cell and pack voltages, temperature, current, and integrated passed charge using the analog interface of the bq29312A AFE and the two delta-sigma ADCs of the bq20z80.

Impedance Track™ Technology Operation Principle

What makes the Impedance Track™ technology unique and much more accurate than existing solutions is a self-learning mechanism that accounts for the change of (1) battery impedance and (2) the no-load chemical full capacity (Qmax) due to battery aging. A fact that is often ignored is that battery impedance increases when the battery ages. As an example, typical Li-ion batteries double the impedance after approximately 100 cycles of discharge. Furthermore, battery impedance also varies significantly between cells and at different usage conditions, such as temperature and state-of-charge. Therefore, to achieve sufficient accuracy, a large, multidimension impedance matrix must be maintained in the IC flash memory, making the implementation difficult. Acquiring such a database is also time-consuming. The Impedance Track™ technology significantly simplifies gas-gauging implementation by continuously updating the battery impedance during the usage lifetime of the battery, and thus only needs a simple, initial impedance database. Temperature and load effects are automatically accounted for when calculating the full-charge capacity (FCC) and the remaining capacity (RM). On the other hand, the Qmax is also calculated and updated during the usage of the battery — only in more strict conditions as mentioned later in this section.

The full-fledged monitoring mechanisms of the bq20z80 allow for accurate measurement of the following key properties:

- OCV: Open-circuit voltage of a battery, usually assuming the battery is already in relaxation mode
- Battery impedance: $\frac{OCV - BatteryVoltageUnder\ Load}{AverageLoad\ Current}$
- PassedCharge: Coulomb counter integrated charge during battery charge or discharge
- SOC: State-of-charge at any moment, defined as SOC=Q/Qmax, where Q is the PassedCharge from the full-charge state
- DOD: Depth of discharge; DOD= 1-SOC
- DOD_0: Last DOD reading before charge or discharge
- DODcharge: DOD for a fully charged pack
- Qstart: Charge that would have passed to make DOD = DOD_0
- Qmax: Maximum battery chemical capacity
- RM: Remaining capacity

- FCC: Full-charge capacity, the amount of charge passed from the fully charged state to the Terminate Voltage

Figure 2 illustrates charge, discharge, and relaxation modes of the battery.

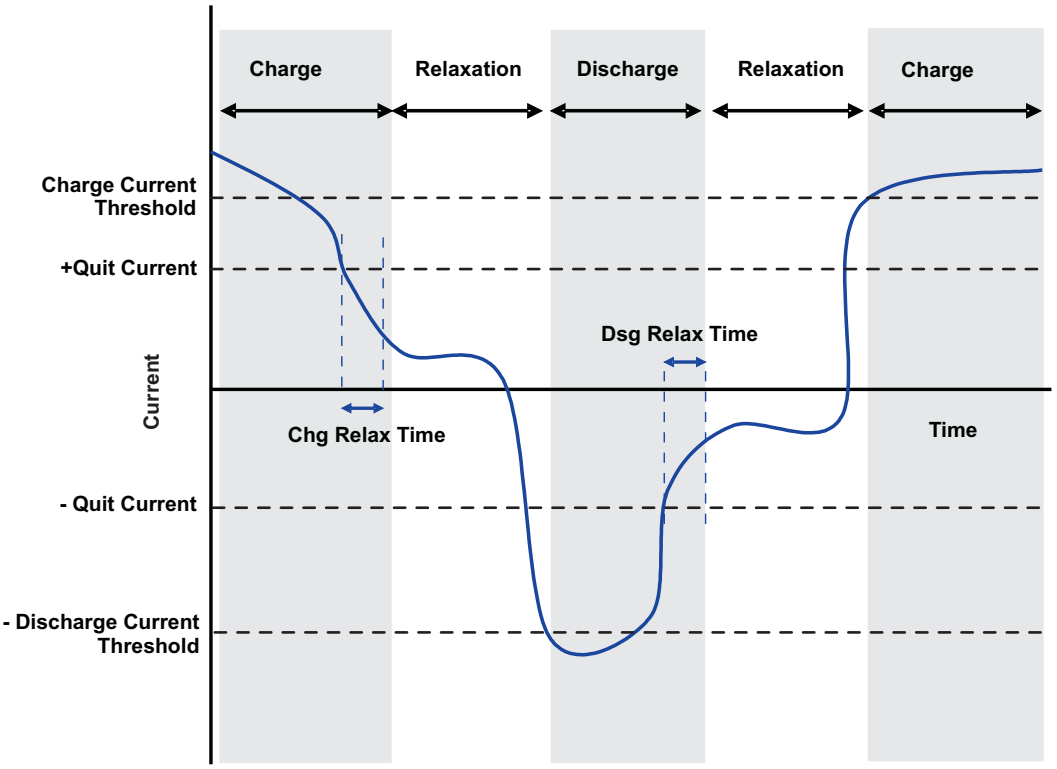


Figure 2. Algorithm Operation Mode Changes With Varying Battery Current

The SOC is estimated based on the OCV of the battery because of a strong correlation of SOC to OCV for a particular battery chemistry, shown in Figure 3 as an example. In the relaxation mode, where no load current is present and the current is below a user-chosen *quit current* level, the SOC is determined using the measured cell voltage (must meet certain voltage settling criteria; see the *Gas Gauging* section in the bq20z80 data sheet, SLUS681, for details) and the predefined OCV versus SOC relationship.

During charging and discharging, the SOC is continuously calculated using the relationship of present Qmax to the integrated passed charge measured by the coulomb counter ADC:

$$Q_{max} = \frac{Passedcharge}{|SOC1 - SOC2|} \quad (1)$$

The derivation of this equation is discussed in the following paragraphs. Figure 4 illustrates graphically illustrates some of the Impedance Track™ terminology.

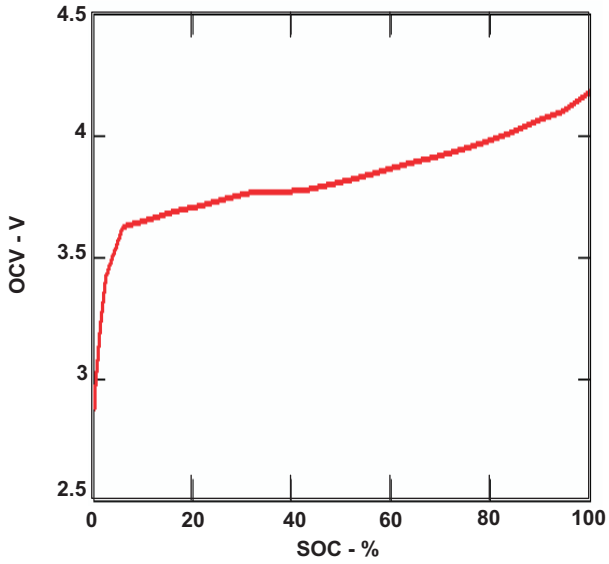


Figure 3. SOC Dependency on OCV

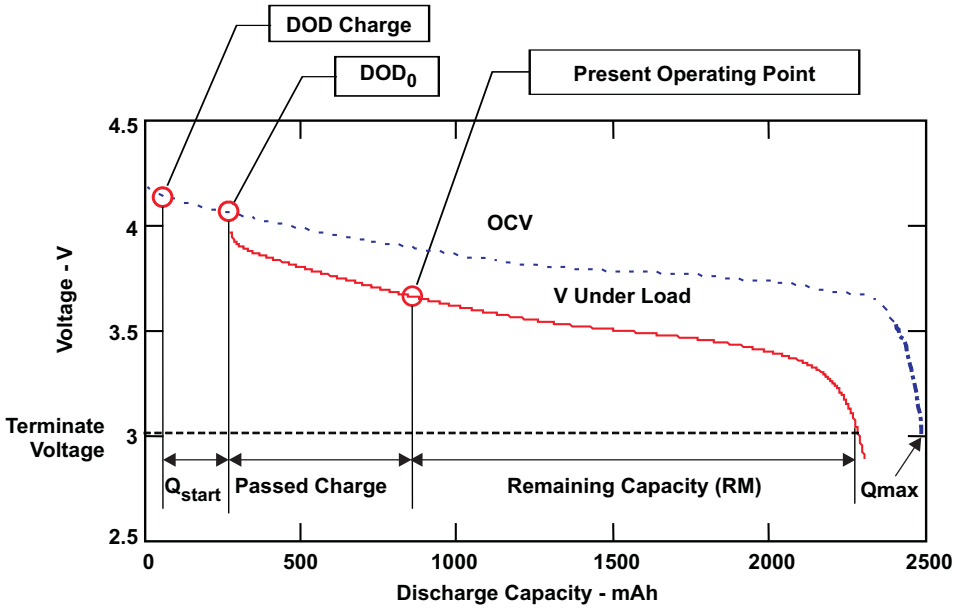


Figure 4. OCV Characteristics (Dotted Curve) and Battery Discharge Curve Under Load (Solid Curve)

Qmax is calculated with two OCV readings (leading to calculation of two SOC values, SOC1 and SOC2) taken at fully relaxed state (dV/dt < 4 µV/sec) before and after charge or discharge activity and when the passed charge is more than 37% of battery design capacity, using Equation 2:

$$SOC1 = \frac{Q1}{Qmax},\ SOC2 = \frac{Q2}{Qmax} \tag{2}$$

subtracting these two equations yields

$$Q_{max} = \frac{Passedcharge}{|SOC1 - SOC2|},\ \text{where Passedcharge} = |Q1 - Q2|. \tag{3}$$

This equation demonstrates that it is unnecessary to have a complete discharge cycle to learn the battery chemical capacity.

When an external load is applied, the impedance of each cell is measured by finding the difference between the measured voltage under load and the open-circuit voltage (OCV) specific to the cell chemistry at the present state-of-charge (SOC). This difference, divided by the applied load current, yields the impedance. In addition, the impedance is correlated with the temperature at time of measurement to fit in a model that accounts for temperature effects.

With the impedance information, the remaining capacity (RM) can be calculated using a voltage simulation method implemented in the firmware. The simulation starts from the present DOD, i.e., DOD_{start} and calculates a future voltage profile under the same load with a 4% DOD increment consecutively:

$$V(DOD_i,T) = OCV(DOD_i,T) + I \times R(DOD_i,T),$$

where $DOD_i = DOD_{start} + I \times 4\%$ and i represents the number of increments, and $R(DOD_I,T)$ is the battery impedance under DOD_i and temperature T. Once the future voltage profile is calculated, the Impedance Track algorithm predicts the value of DOD that corresponds to the system termination voltage and captures this as DOD_{final}. The remaining capacity then is calculated using:

$$RM = (DOD_{final} - DOD_{start}) \times Q_{max}$$

FCC (Full-charge capacity) is the amount of charge passed from the fully charged state to the Termination Voltage, and can be calculated using:

$$FCC = Qstart + PassedCharge + RM$$

The following section presents a more detailed description of the gas gauge hardware.

Gas Gauge Hardware

1.2.3.2 bq29312A Analog Front-End Protector The bq29312A AFE serves an important role for the bq20z80 2-, 3-, or 4-cell lithium-ion battery pack gas gauge chipset solution. The bq29312A powers the bq20z80 directly from its 3.3-V, 25-mA low-dropout regulator (LDO), which is powered by either the battery voltage or the pack+ voltage. The AFE also provides all the high-voltage interface needs (the battery cell voltage levels need to be down-converted to meet the input range requirement of bq20z80 ADC) and current protection features. The AFE offers an I^2C-compatible interface to allow the bq20z80 to have access to the battery information and to configure the AFE's protection features. Other features of the AFE include cell balance control, thermistors drive circuit, precharge function, etc. Figure 5 presents a functional block diagram of the bq29312A AFE.

The AFE can be configured to translate each of the series cell voltages or the pack voltage into ground-referenced voltage, which can be measured by the bq20z80 gas gauge IC. The allowable AFE input range for an individual cell is 0 V to 4.5 V. Because voltage measurement accuracy is crucial for minimizing battery capacity estimate errors, the bq29312A AFE provides means for the bq20z80 to measure its voltage monitor amplifier offset and gain errors, leading to accurate gas gauge calibration.

In many situations, the state-of-charge (SOC) of the individual cells may differ from each other in a multicell battery pack, causing cell imbalance and voltage difference between cells. The bq29312A AFE incorporates a bypass path for each of the series element. These bypass paths can be used to reduce the charging current into any cell and thus allow for an opportunity to balance the SOC of the cells during charging. The bq20z80 enables and disables these paths as needed through the I^2C bus.

The bq29312A is also responsible for overload and short-circuit detection and protection of the pass FETs (i.e., charge and discharge FETs), cells, and any other inline components from excessive current conditions. The overload detection is used to detect excessive currents in the discharge direction, whereas the short-circuit detection is used to detect excessive current in either the charge or discharge direction. Threshold and delay time of overload and short-circuit can be programmed by bq20z80. When an overload or short-circuit is detected and a programmed delay time has expired, the FETs are turned off and the details of the condition are reported in the STATUS (b0:b2) register of bq29312A. Next, the XALERT output is triggered, signaling the bq20z80 to investigate the failure.

Another feature of the AFE is the precharging function. In some cases, the battery that needs to be charged is deeply depleted. When the CHG-FET is turned on, the voltage at the pack pin of bq29312A is as low as the battery voltage, which can be too low for the AFE to operate. The bq29312A provides three precharging/0-V charging options to remedy this problem.

1.2.3.3 How the bq20z80 and bq29312A Operate Together The bq20z80 is the master of this chipset because it implements the entire Impedance Track™ algorithm. The bq29312A is configured by the bq20z80 for how it should respond to handle gas-gauging situations. These include when and which cell voltage information it needs to provide to the gas gauge IC, and what overload and short-circuit threshold and delay value should be used.

On the other hand, the bq20z80 requires the bq29312A to create a full solution for 2-, 3- or 4-series-cell Li-Ion battery packs. The bq20z80 cannot operate without the AFE. As shown in Figure 1, the bq20z80 relies on the AFE to provide scaled cell/pack voltage information to perform gas gauging and voltage/current protection functions. The bq20z80 can only access the charge and discharge FETs by sending control commands to the AFE. The bq20z80 has two tiers of charge/discharge overcurrent protection settings, and the AFE provides a third level of discharge overcurrent protection. In case of short-circuit condition, which does not need more than a brief amount of time to damage the circuit, the gas gauge chipset entirely depends on the AFE to autonomously shut off the FETs before such damage occurs.

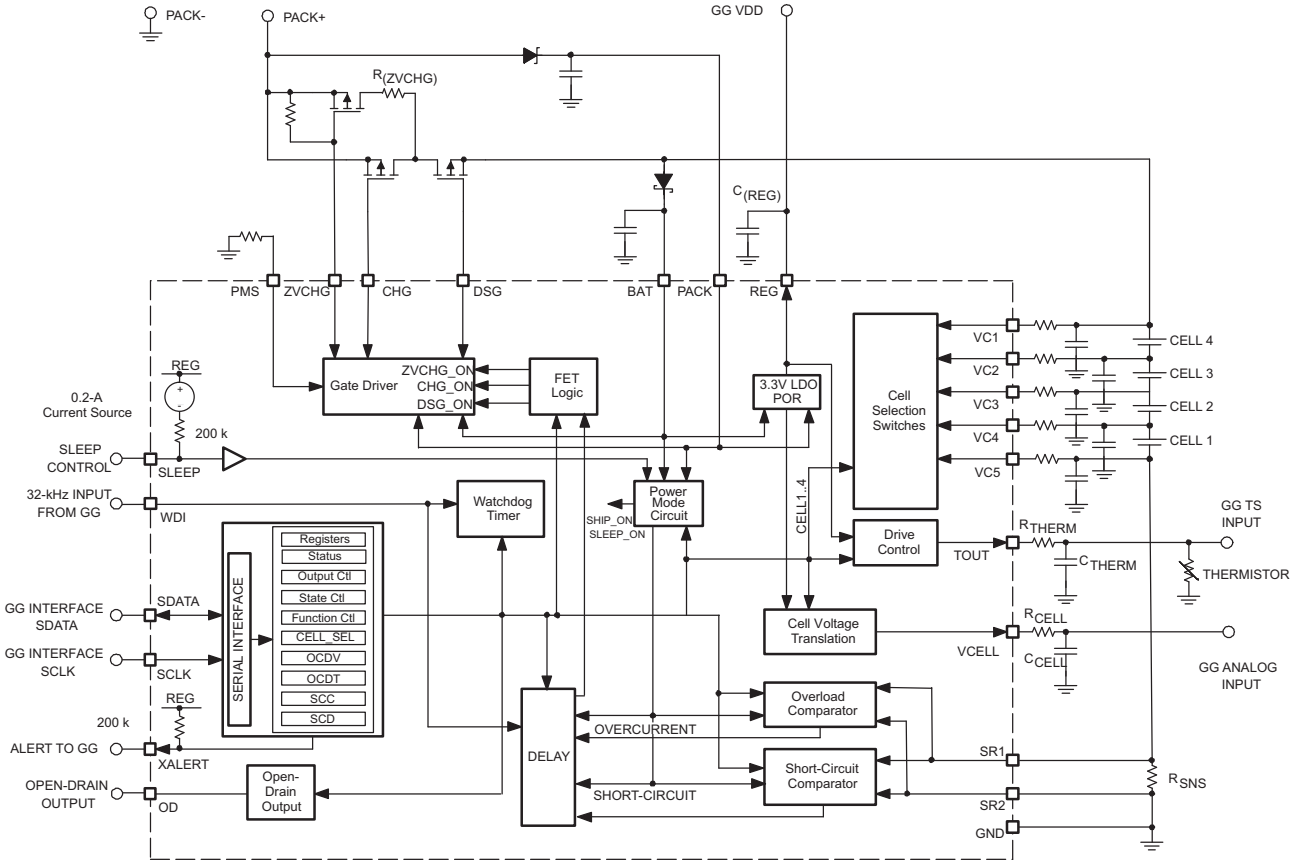


Figure 5. bq29312A Functional Block Diagram

1.2.3.4 The bq2941x 2nd-Level Overvoltage Protector Although the bq20z80 and its associated AFE provide overvoltage protection, the sampled nature of the voltage monitoring limits the response time of this protection system. Most applications require a fast-response, real-time, independent overvoltage monitor operating with the bq20z80 and the AFE. Texas Instruments offers the bq2941x 2nd-level protector IC for this purpose. The bq2941x monitors individual cell voltages independently of the gas gauge and AFE and provides a logic level output which toggles if any of the cells reaches a hard-coded overvoltage limit. The response time of the IC is determined by the value of an external delay capacitor. In a typical application, the output of the bq2941x would be tied to a heater fuse or other fail-safe protection device.

bq20z80EVM-001 Evaluation Module

The bq20z80EVM-001 evaluation module (EVM) is a complete evaluation system for the bq20z80/bq29312A/bq29412 battery pack electronics system. The EVM includes:

1. One bq20z80/bq29312A/bq29412 circuit module
2. A current sense resistor
3. Two thermistors
4. An EV2300 PC interface board for gas gauge interface
5. A PC USB cable
6. Windows™-based PC software

The circuit module includes one bq20z80 IC, one bq29312A IC, one bq29412 IC, and all other onboard components necessary to monitor and predict capacity, perform cell balancing, monitor critical parameters, protect the cells from overcharge, overdischarge, short-circuit, and overload in 2-, 3-, or 4-series-cell Li-ion or Li-polymer battery packs. The circuit module connects directly across the cells in a battery. With the EV2300 interface board and software, the user can read the bq20z80 data registers, program the chipset for different pack configurations, log cycling data for further evaluation, and evaluate the overall functionality of the bq20z80/bq29312A/bq29412 solution under different charge and discharge conditions.

bqEVSW Software for Use With the bq20z80

The bqEVSW is a Windows™-based evaluation software program provided by TI for functional evaluation of the bq20z80/bq29312A/bq2941x chipset. The bqEVSW provides the standard Smart Battery System (SBS) data commands as well as extended SBS commands. On opening the software, it automatically detects the presence of EV2300 USB module and the chipset. Once the device type and version of firmware are identified, the software displays the SBS interface. The users may also toggle between SBS, Data flash, Calibration, and Pro screens for a variety of information about the battery pack and the chipset settings. The bqEVSW can also be used to program or update the firmware of the bq20z80 and for battery cycle data logging. See the bq20z80EVM user's guide and application reports for more information.

1.3 Next Steps

Developing a PCB for the bq20z80 and bq29312A Chipset

Using the 3-cell reference design schematic in the Appendix as a guide, a battery pack schematic should be designed to meet the individual requirements. Start with the number of cells. Note that in this schematic, pins VC1 and VC2 are connected on both the bq29312A and the bq29412. For packs with 2-series cells, connect VC1, VC2, and VC3 of each device together and remove the filter components R8, C7, R28, and C23. For a 4-cell design, follow the pattern of the 3-cell schematic but add an additional RC network at the VC1 input of both ICs.

Next, the current-sense resistor should be selected. As a general guideline, 20 mΩ is appropriate for a single (1P) string of 18650 cells, whereas 10 mΩ is recommended for a 2P pack. See the bq29312A data-sheet tables to ensure that the desired short-circuit and over-current protection levels fall within the available range for the selected sense resistor.

The use of a chemical fuse is recommended. Using information from the fuse data sheet, ensure that the FET used to ignite the fuse has a low enough on-resistance to succeed in opening the fault. Also, note that the gate of Q3 (see the reference design schematic in the Appendix) is driven by a 3.3-V output port from the bq20z80 in series with a Schottky diode. Ensure that the selected FET turns on adequately to provide the required ignition current. The output voltage of the bq29412 is around 6 V, providing an adequate 3 V to the gate of Q3.

The bq29312A is flexible with regard to the precharge function. The schematic in the Appendix uses the *Common FET* mode for precharge, where the Charge FET is turned on at initialization allowing for precharge current to flow. Two other precharge modes are also supported, but require the use of a dedicated precharge FET. The bq29312A data sheet (SLUS629) contains detailed theory of operation for each mode

Printed-circuit board layout requires careful consideration when developing a smart battery application. The high currents developed during a battery short-circuit event can be incompatible with the micropower design of the semiconductor devices. It is important to realize that battery transients can be capacitively or magnetically coupled into low-level circuits resulting in unwanted behavior. Success with a first-pass design can depend on realizing that parallel circuit board traces are indeed small capacitors and current transformers. The ideal board layout would have the entire high-current path physically located away from the low-current electronics. Because this is not often possible, the coupling principle must be taken into account. Short-circuit, ESD, and EMI testing should be part of the initial checkout of a new design.

With regard to component placement, several components surrounding the bq20z80 need special attention. Most important are the two, power-supply decoupling capacitors C10 and C11 and the oscillator resistor R13. Each of these must be close to the gas gauge device and have low-resistance / low-inductance connections that do not form large loops. C10 should be placed between pins 8 and 11. C11 should be located between pins 31 and 29. The trace from R13 to U2-34 must not include return currents from other components. Also, C29 should be close to U2. Components of lesser priority but still a concern are the PLL filter components R14, C14, and C15 and the master reset network C4, R9. These should all be placed in the general vicinity of the IC. Over on the bq29312A, C8, C18, and C24 should be placed as close to U3 as practically possible, with the loop area minimized.

Proper sensing of voltage and current requires the use of Kelvin connections at the sense resistor and at the top and bottom battery terminals. If top and bottom connections to the cells allow too much voltage drop, then the resulting error in cell voltage measurement has an effect on the measurement accuracy of battery capacity and therefore the remaining run time.

It Is important to have correct grounding. On the reference design schematic in the Appendix, two separate symbols are used for low-level analog and low-level digital grounds. These should be kept separate, only joining together at the sense resistor as shown. The Pack– terminal (also known as ESD ground) is the suggested return point for C19, SW1, and the D3 network. For additional information, see the TI application report *Avoiding ESD and EMI Problems in bq20zxx Battery Pack Electronics* (SLUA368).

Solution Development Process

Browsing the data flash screens of the bq20z80 evaluation software can be a challenging experience. Approximately 300 individual settings are possible. However, the default value for most of them can be easily used. The first step is to set up the data flash values for the number of cells and the coulomb capacity for a specific application. This simple process is described in detail in the application report *bq20z80 EVM Data Flash Settings for Number of Serial Cells and Pack Capacity* (SLVA208).

With different numbers of cells, several voltage settings must change. Application report SLVA208 presents the suggested default settings for Pack Over Voltage, Pack Under Voltage, Safety Over Voltage, Charging Voltage, Design Voltage, Cell Configuration, Flash Update OK Voltage, Shutdown Voltage, Charger Present Voltage, and Charge Terminate Voltage.

With different types of cells and number of parallel cells, capacity settings are different. Suggested values are presented for Qmax Cells, Qmax Pack, Design Capacity, and Design Energy in the same application report (SLVA208).

With the preceding changes in place, the evaluation module should function normally with the target cell configuration. The next step is to review all of the selectable features in the configuration registers A and B. Use the data sheet to review each configuration bit in these registers and configure them for a specific application. Note that if you use the default of 0 for the NR bit in Configuration Register B, then a System_Present signal needs to be implemented on the pack connector. See the EVM user's guide (SLUU205) schematic for implementation details.

Mass Production Setup

One of the main benefits of Impedance Track™ technology is the significant reduction in the complexity of battery pack mass production. Because many data flash values are adaptively derived with use, it is possible to simply transfer the knowledge gained from a single *golden* pack to each individual pack as it leaves the assembly line. Charging and discharging each pack in order to force it to learn its capacity is unnecessary. Although the individual packs will contain cells with varying impedances, that is quickly corrected during normal use as impedance is constantly measured and updated by the bq20z80 gas gauge.

A good strategy for production is a 7-step process flow:

1. Write the data flash image to each device. This image was read from a *golden* pack
2. Calibrate the device.
3. Update any individual flash locations, such as serial number, lot code, and date.
4. Perform any desired protection tests.
5. Connect the cells.
6. Initiate the Impedance Track™ algorithm.
7. Seal the pack.

The TI application report *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* (SLUA355) discusses the first three steps in detail. TI application report *Pack Assembly and the bq20z80* (SLUA335) discusses step 5 in detail. Description of steps 6 and 7 can be found in the bq20z80 data sheet (SLUS681). Calibration is presented as sample VB6 code for those who wish to develop their own calibrator. However, Texas Instruments has higher-level support for high-speed programming and calibration steps. A single channel test and calibration program is available, with open-source code. Also, a multistation test system is available.

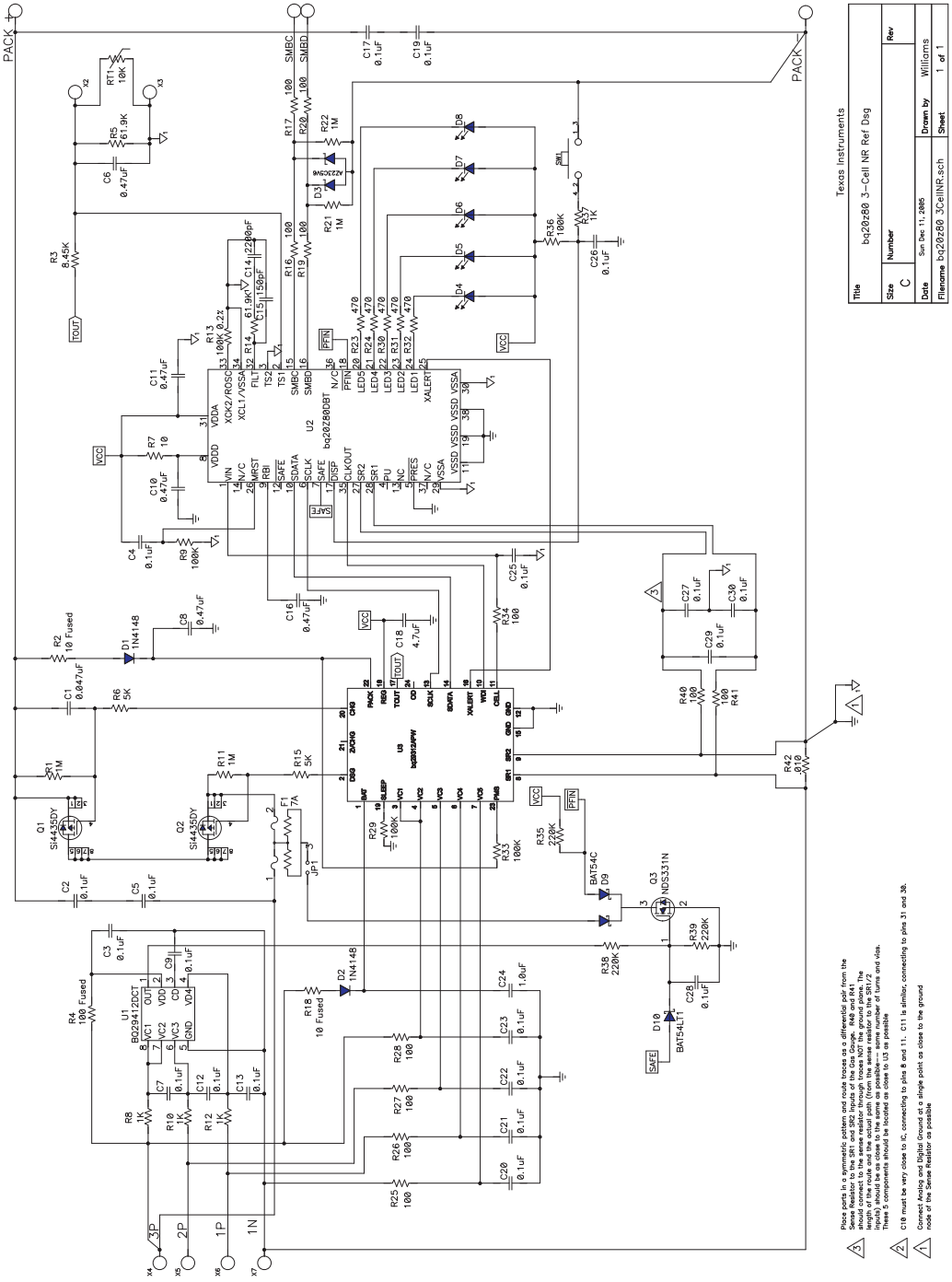
For additional application reports covering various aspect of bq20z80 Impedance Track solution, see the Texas Instruments bq20z80 online product folder.

1.4 Glossary

- OCV: Open-circuit voltage of a battery
- Passed Charge: Coulomb counter integrated charge during battery discharge or battery charge
- Qmax: Maximum battery chemical capacity
- Design Capacity: Cell chemical capacity specified by cell manufacturer times number of paralleled cells
- SOC: State-of-charge at any moment, defined as SOC=Q/Qmax (usually in %), where Q is the Passed Charge from full charge state
- DOD: Depth of discharge; DOD= 1-SOC (usually in %)
- DOD_0: Last DOD reading before charge or discharge
- DODcharge: DOD for a fully charged pack
- Qstart: Charge that would have passed from fully charged state to make DOD = DOD_0
- RM: Remaining capacity, in mAh or mWh
- FCC: Full-charge capacity, the amount of charge passed from the fully charged state to the terminate voltage, in mAh or mWh
- Quit current: user-defined current levels for both charge and discharge, usually about ~10 mA
- Relaxation mode: the state of the battery when the current is below user-defined *quit current* levels and after a user-defined minimum charge relax time (see Figure 2)
- AFE: Analog front-end, in this document, this refers to the bq29312A

Reference Design Schematic

The reference design schematic is affixed to this page.



Chapter 2

Configuring the bq20z80 Data Flash

Battery Management

ABSTRACT

The bq20z80 has numerous data flash constants that can be used to configure the device with a variety of different options for most features. The data flash of the bq20z80 is split into sections which are described in detail within this document.

2.1 Glossary

ASOC: **Absolute State of Charge**

Bit: **This word has a different meaning than Flag. This word is used to refer to a configuration setting bit. It is primarily used in data flash settings.**

Blink, Flash and Delay: **There are 3 different display modes for the LEDs in this document that need clarification.**

- **Blinking: When the display is said to be blinking, then the word "blinking" is used to refer to the LED located closest to the LED used to indicate 100% that is illuminated and "blinking" when the LED display is activated and displaying SOC (state of charge). Only this "topmost" activated LED in the display blinks. All other LEDs that are activated is steady state when activated. (see *LED Blink Rate*)**
- **Flashing: When the display is said to be flashing, then the word "flashing" means all LEDs that are activated to indicate the SOC will flash with a period of (2 ×*LED Flash Rate*).**
- **Delay: When the display is activate, all LEDs that are required to indicate the SOC may not illuminate at the same time. Starting from the LED that represents the lowest SOC, there can be a delay (*LED Delay*) between each LED illuminating from the LED that represents the lowest possible SOC up to the LED that represents the present SOC.**

***Cell Voltage(Max)*:** **This represents the maximum value among all the SBS cell voltage registers.(*Cell Voltage 1* through *Cell Voltage 4*)**

***Cell Voltage(Min)*:** **This represents the minimum value among all the SBS cell voltage registers.(*Cell Voltage 1* through *Cell Voltage 4*)**

***Cell Voltage(Any)*:** **This represents any of the possible SBS cell voltage registers.(*Cell Voltage 1* through *Cell Voltage 4*)**

[DSG] in *Battery Status*: **SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. This can be confused in many descriptions in this document because different functions require different methods for determining charging or discharging. The SBS description sometimes does not give enough resolution for correct part function so these functions require other data flash registers as described in their respective definitions. SBS states that if the battery is charging then [DSG] is 0, and any other time (Current less than or equal to 0), the [DSG] flag is set. The actual formula that the bq20z80 uses for setting or clearing the [DSG] flag are as follows:**

[DSG] clear: **[DSG]=0 if *Current* >= Chg Current Threshold**

[DSG] set: **[DSG]=1 if**

1. **Current <= Dsg Current Threshold or**
2. **Relaxation Mode which is defined by one of the following statements:**
   - **A) *Current* transitioning from below (–)*Quit Current* to (above (–)*Quit Current* and below *Quit Current*) for *Dsg Relax Time***
   - **B) *Current* transitioning from above *Quit Current* to (below *Quit Current* and above (–)*Quit Current*) for *Chg Relax Time***

FCC: Full Charge Capacity

FET opened/Closed: It is common to say FET opened or FET closed. This is used throughout this document to mean the FET is turned off or the FET is turned on respectively.

Flag: This word is usually used to represent a read only status bit that indicates some action has occurred or is occurring. This bit usually cannot be modified by the user.

Precharge/ZVCHG: The words Precharge and ZVCHG are interchangeable throughout the document

RCA: Remaining Capacity Alarm

RM: Remaining Capacity

RSOC: Relative state of Charge

RTA: Remaining Time Alarm

SAFE and $\overline{\text{SAFE}}$: These words are used throughout this document to represent 2 output pins on the bq20z80. SAFE is pin 7 on the bq20z80 and $\overline{\text{SAFE}}$ is pin 12. When this document discusses permanent failures, it normally includes a discussion of these two pins. When a permanent failure happens and its control bit is enabled, then these 2 pins are activated to either blow a fuse or to activate some hardware protection. The reason there are 2 outputs is for backwards compatibility with bq20z8X parts and to give options for an application. Both outputs are activated at the same time when enabled, but the $\overline{\text{SAFE}}$ pin is active low so it is driven low when activated while the SAFE pin is active high and is driven high when activated.

SOC: This is used as a generic meaning of State-of-Charge. It can mean RSOC, ASOC, or percentage of actual chemical capacity.

System: The word system is sometimes used in this document. It always means a host system that is consuming current from the battery pack that includes the bq20z80.

***Italics*:** All words in this document that are in italics represent names of data flash locations exactly as they are shown in the EV software.

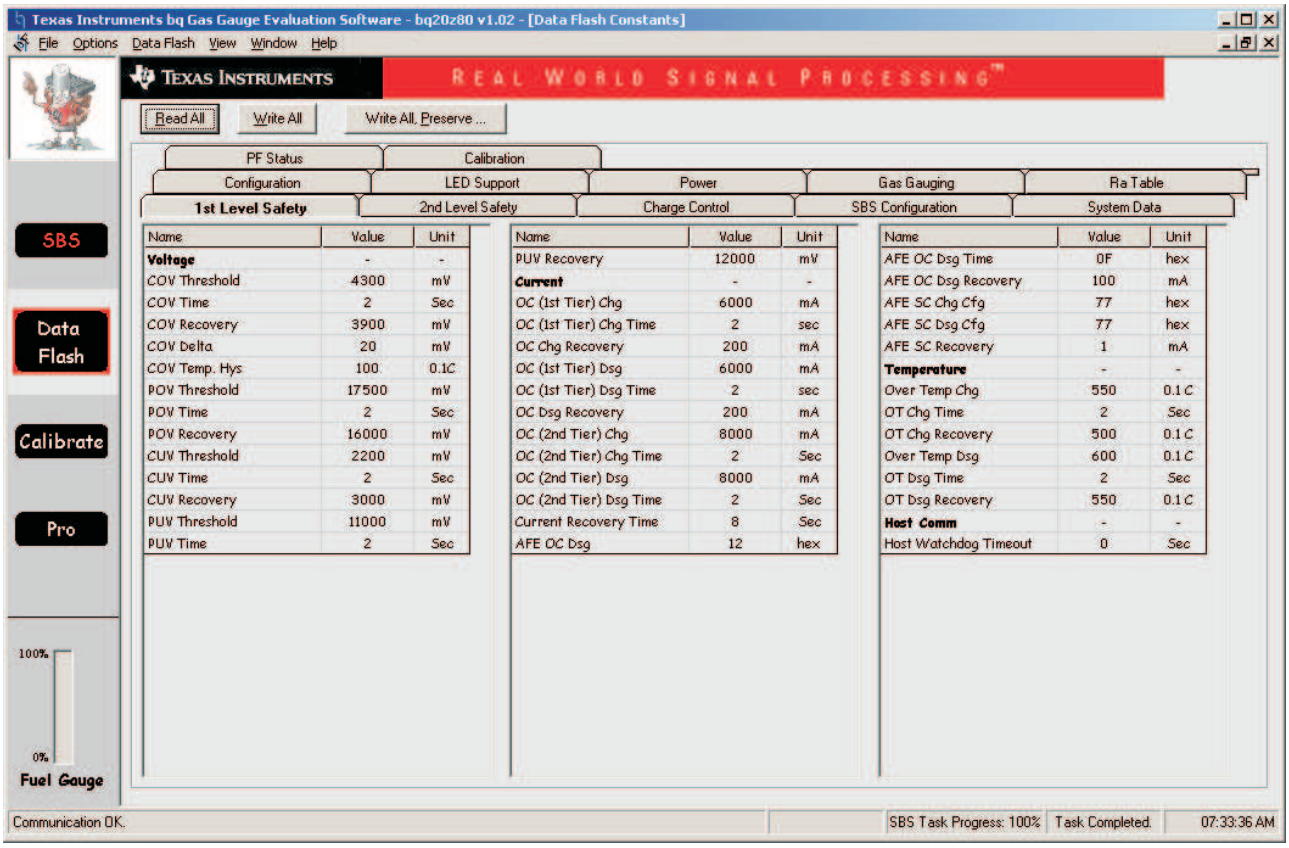
***Bold Italics*:** All words that are bold italic represent SBS compliant registers exactly as they are shown in the EV software.

[brackets]: All words or letters in brackets represent bit/flag names exactly as they are shown in the SBS and Data Flash in the EV software.

(–): This is commonly used in this document to represent a minus sign. It is written this way to ensure that the sign is not lost in the translation of formulas in the text of this document.

2.2 1st Level Safety

All 1st Level Safety functions are temporary. There should be no permanent failures or damage to the battery if any of the 1st Level Safety functions are triggered.



Name	Value	Unit
Voltage	-	-
COV Threshold	4300	mV
COV Time	2	Sec
COV Recovery	3900	mV
COV Delta	20	mV
COV Temp. Hys	100	0.1C
POV Threshold	17500	mV
POV Time	2	Sec
POV Recovery	16000	mV
CUV Threshold	2200	mV
CUV Time	2	Sec
CUV Recovery	3000	mV
PUV Threshold	11000	mV
PUV Time	2	Sec

Name	Value	Unit
PUV Recovery	12000	mV
Current	-	-
OC (1st Tier) Chg	6000	mA
OC (1st Tier) Chg Time	2	sec
OC Chg Recovery	200	mA
OC (1st Tier) Dsg	6000	mA
OC (1st Tier) Dsg Time	2	sec
OC Dsg Recovery	200	mA
OC (2nd Tier) Chg	8000	mA
OC (2nd Tier) Chg Time	2	Sec
OC (2nd Tier) Dsg	8000	mA
OC (2nd Tier) Dsg Time	2	Sec
Current Recovery Time	8	Sec
AFE OC Dsg	12	hex

Name	Value	Unit
AFE OC Dsg Time	0F	hex
AFE OC Dsg Recovery	100	mA
AFE SC Chg Cfg	77	hex
AFE SC Dsg Cfg	77	hex
AFE SC Recovery	1	mA
Temperature	-	-
Over Temp Chg	550	0.1 C
OT Chg Time	2	Sec
OT Chg Recovery	500	0.1 C
Over Temp Dsg	600	0.1 C
OT Dsg Time	2	Sec
OT Dsg Recovery	550	0.1 C
Host Comm	-	-
Host Watchdog Timeout	0	Sec

Voltage

COV Threshold

When any cell voltage measured by ***Cell Voltage (Any)*** rises to this threshold, then the Cell Over Voltage (COV) protection process is triggered, initiating a [COV] in ***Safety Alert*** for *COV Time*. If the COV condition clears prior to the expiration of the *COV Time* timer, then [COV] in *Safety Alert* is cleared and no [COV] flag is set in ***Safety Status***. If the COV condition does not clear, then [COV] is set in ***Safety Status*** and the Charge FET is opened. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. Setting *COV Time* to 0 completely disables this function.

Normal Setting: Default is 4300 mV. This cell is chemistry dependent, but 4200-4300 is the most common settings.

COV Time

See *COV Threshold*. This is a buffer time allotted for a COV condition. The timer starts after [COV] is set in ***Safety Alert***. When it expires, then the bq20z80 forces [COV] set in ***Safety Status*** and opens the Charge FET. If the condition clears prior to the expiration of the *COV Time* timer, then the [COV] is cleared in ***Safety Alert*** and the COV Time timer resets without setting [COV] in ***Safety Status***. Setting *COV Time* to 0 completely disables *COV Threshold*.

Normal Setting: This is normally set to 2 seconds, but depends on the application.

COV Recovery

When a [COV] is set in ***Safety Status***, it is only cleared when **ALL** cell voltages as measured by ***Cell Voltage(All)*** fall below this threshold.

Normal Setting: This defaults to 3900 mV. It must be set low enough that the hysteresis between *COV Threshold* fault and this recovery prevents oscillation of the Charge FET.

COV Delta

The actual trigger value for *the COV Threshold* is adjusted down by this amount if ***Temperature*** rises above (*Over Temperature Threshold – COV Temp Hys*). The actual Data Flash location for *COV Threshold* is not modified, just the trigger value. It returns to normal if the temperature falls below (*Over Temperature Threshold – COV Temp Hys*). If this time is set to 0, then the *COV Threshold* trigger value is not modified based on the temperature.

Normal Setting: This value is normally set to 20 mV. This is application and cell chemistry dependent.

COV Temp Hys

See *COV Delta*. This is the delta temperature below the *Over Temperature Threshold* where the *COV Threshold* is modified by *COV Delta*.

Normal Setting: This value is normally set to 100 in 0.1°C. This is application and cell chemistry dependent.

POV Threshold

When the pack voltage measured by ***Voltage*** rises to this threshold, then the Pack Over Voltage (POV) protection process is triggered. This process starts by setting [POV] in ***Safety Alert*** for POV Time. If the POV condition clears prior to the expiration of the *POV Time* timer, then the [POV] is cleared in ***Safety Alert*** with no [POV] being set in ***Safety Status***. If the POV condition does not clear, then [POV] is set in ***Safety Status*** and the Charge FET is opened. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. Setting *POV Time* to 0 completely disables this function.

Normal Setting: This register defaults to 17500 which is for a 4-cell pack. This is high, but it depends on the cell chemistry and the number of cells in series for an application. It is normally set to the (number of cells × 4300 mV). (i.e., 8600 mV for 2-cell applications, 12900 mV for 3-cell, and 17200 mV for 4-cell applications)

POV Time

See *POV Threshold*. This is a buffer time allotted for a POV condition. The timer starts after the [POV] is set in ***Safety Alert***. When it expires, then the bq20z80 forces [POV] set in ***Safety Status*** and opens the Charge FET. If the condition clears prior to the expiration of the *POV Time* timer, then [POV] is cleared in ***Safety Alert*** and the *POV Time* timer resets. Setting *POV Time* to 0 completely disables *POV Threshold*.

Normal Setting: This is normally set to 2 seconds, but depends on the application.

POV Recovery

When [POV] is set in ***Safety Status***, it is only cleared when the pack voltage measured by ***Voltage*** falls below this threshold.

Normal Setting: This defaults to 16000 mV. It must be set low enough that the hysteresis between *POV Threshold* fault and this recovery prevents oscillation of the Charge FET.

CUV Threshold

When any cell voltage measured by ***Cell Voltage(Any)*** falls below this threshold, then the Cell Under Voltage (CUV) protection process is triggered, initiating a [CUV] flag getting set in ***Safety Alert*** for *CUV Time*. If the CUV condition clears prior to the expiration of the *CUV Time* timer, then [CUV] is cleared in ***Safety Alert*** and no [CUV] is set in ***Safety Status***. If the CUV condition does not clear, then a [CUV] is set in ***Safety Status*** and the Discharge FET is opened. This fault condition causes [TDA] and [FD] in ***Battery Status*** to be set. It also causes [XDSG] in ***Operation Status***. Setting *CUV Time* to 0 completely disables this function.

Normal Setting: Default is 2200 mV. This is cell chemistry dependent but 2200 mV–2300 mV is the most common setting.

CUV Time

See *CUV Threshold*. This is a buffer time allotted for a CUV condition. The timer starts after [CUV] is set in ***Safety Alert***. When it expires, then the bq20z80 forces [CUV] set in ***Safety Status*** and opens the Charge FET. If the condition clears prior to the expiration of the *CUV Time* timer, then [CUV] is cleared in ***Safety Alert*** and the *CUV Time* timer resets. Setting *CUV Time* to 0 completely disables *CUV Threshold*.

Normal Setting: This is normally set to 2 seconds but depends on the application.

CUV Recovery

When [CUV] is set in ***Safety Status***, it is only cleared when **ALL** cell voltages as measured by ***Cell Voltage(All)*** rise above this threshold.

Normal Setting: The default for this register is 3000 mV. It must be set high enough that the hysteresis between *CUV Threshold* fault and this recovery prevents oscillation of the Discharge FET.

PUV Threshold

When the pack voltage measured by ***Voltage*** falls below this threshold, then the Pack Under Voltage (PUV) protection process is triggered, initiating a [PUVt] in ***Safety Alert*** for *PUV Time*. If the PUV condition clears prior to the expiration of the *PUV Time* timer, then [PUV] is cleared in ***Safety Alert*** and [PUV] are not set in ***Safety Status***. If the PUV condition does not clear, then a [PUV] is set in ***Safety Status*** and the Discharge FET is opened. This fault condition causes [TDA] and [FD] in ***Battery Status*** to be set. It also causes [XDSG] in ***Operation Status***. Setting *PUV Time* to 0 completely disables this function.

Normal Setting: This register defaults to 11000 which is for a 4-cell pack. This is very application and cell chemistry dependent. It also depends on the number of cells in series for an application. A very common setting is the (number of cells $\times$ 2750 mV). i.e., 5500 mV for 2-cell applications, 8250 mV for 3-cell, and 11000 mV for 4-cell applications)

PUV Time

See *PUV Threshold*. This is a buffer time allotted for a PUV condition. The timer starts after [PUV] is set in ***Safety Alert***. When it expires, then the bq20z80 forces [PUV] set in ***Safety Status*** and opens the Discharge FET. If the condition clears prior to the expiration of the *PUV Time* timer, then [PUV] is cleared in ***Safety Alert*** and the *PUV Time* timer resets. Setting *PUV Time* to 0 completely disables *PUV Threshold*.

Normal Setting: This is normally set to 2 seconds but depends on the application.

PUV Recovery

When [POV] is set in ***Safety Status***, it is only cleared when the pack voltage measured by ***Voltage*** falls below this threshold.

Normal Setting: The default for this register is 12000 mV. Set high enough that the hysteresis between *PUV Threshold* fault and this recovery prevents oscillation of the Discharge FET.

Current

There are 3 levels or tiers of current protection in the bq20z80. The first 2 levels, 1st Tier and 2nd Tier are slow responding (>1 second). The third level is a very quick responding current protection controlled directly by the bq29312A.

IT is important that the bq29312A makes the triggering decision for any of the AFE fault conditions. This is to ensure quick response to dangerous faults. It is also designed in such a way that the AFE can act completely autonomously in the event of damage to the bq20z80 in the triggering of any AFE fault. The bq29312A cannot, however, clear the fault condition. It is cleared only by the bq20z80. The AFE data is transferred to the bq29312A on reset and (if enabled in the **AFE Verification** subclass) is continually monitored by the bq20z80 to ensure no corruption has occurred at any time. If corruption has occurred, the bq20z80 attempts to make corrections. If after repeated attempts (as set in the **AFE Verification** subclass), it cannot correct the condition, then it sets a permanent failure. If enabled in *Permanent Fail Cfg*, then the SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. (See *Permanent Fail Cfg*)

OC (1st Tier) Chg

When current measured by ***Current*** reaches up to or above this threshold during charging, then the 1st Tier Over Current in the Charge [OCC] protection process is triggered, initiating an [OCC] in ***Safety Alert*** for *OC (1st Tier) Chg Time* in seconds. If the 1st Tier OCC condition clears prior to the expiration of the *OC (1st Tier) Chg Time* timer, then [OCC] in ***Safety Alert*** is cleared and no [OCC] is set in *Safety Status*. If the 1st Tier OCC condition does not clear, then a [OCC] is set in ***Safety Status*** and the Charge FET is opened. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. Setting the *OC (1st Tier) Chg Time* to 0 completely disables this function.

Normal Setting: This register is application dependent. It should be set above the absolute maximum expected discharge current. It should be set high enough that unexpected mild charge spikes or inaccuracies do not create a false over current trigger, but low enough to force the Charge FET to open before damage occurs to the pack.

OC (1st Tier) Chg Time

See *OC(1st Tier) Chg*. This is a buffer time allotted for a 1st tier Over Current condition. The timer starts every time the [OCC] in ***Safety Alert*** is initially set. When the timer expires, then the bq20z80 forces an [OCC] in ***Safety Status*** and opens the Charge FET. If [OCC] in ***Safety Alert*** clears prior to the expiration of the *OC (1st Tier) Chg Time* timer, then [OCC] in ***Safety Alert*** is cleared and the *OC (1st Tier) Chg Time* timer resets. Setting the *OC (1st Tier) Chg Time* to 0 disables OC (1st Tier) Chg .

Normal Setting: This is normally set to 2 seconds, but depends on the application. It must be set long enough to prevent false triggering of the [OCC] in ***Safety Status***, but short enough to prevent damage to the battery pack.

OC Chg Recovery

OC Chg Recovery is one of several recovery methods used for both 1st and 2nd level Over Current in the charge direction faults. This value is used for either nonremovable packs ([NR] in *Operation Cfg B =1)* or for removable packs configured ([OCC] in *Non-Removable Cfg)*. With either of these settings, ***Average Current*** must fall below this value for *Current Recovery Timer* in seconds to clear the [OCC] or the [OCC2] in ***Safety Status*** if either is set.

Normal Setting: This register is application dependent, but is normally set low enough that it prevents quick oscillation in the Charge FET. ***Average Current*** is used for this recovery function and falls every second that it is recomputed with ***Current*** at or near 0. If this recovery is set too high, then the Charge FET can oscillate with a frequency that is fast enough to cause damage to the battery pack because the ***Average Current*** falls below this value quickly.

OC (1st Tier) Dsg

When current measured by ***Current*** falls down to or below this threshold during discharging then the 1st Tier Over Current in discharge (OCD) protection process is triggered, initiating an [OCD] in ***Safety Alert*** for *OC (1st Tier) Dsg Time* in seconds. If the 1st Tier OCD condition clears prior to the expiration of the *OC (1st Tier) Dsg Time* timer, then the [OCD] is cleared and no [OCD] is set. If the 1st Tier OCD condition does not clear, then a [OCD] is set in ***Safety Status*** and the Discharge FET is opened. This fault condition causes [XDSG] and [XDSGI] in ***Operation Status*** to be set. It also causes ***Charging Current*** to be set to 0.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent. It should be set **below** the absolute maximum expected discharge current. It must be set low enough that unexpected mild discharge spikes or inaccuracies do not create a false over current trigger, but high enough to force the Discharge FET open before damage occurs to the pack.

OC (1st Tier) Time Dsg

See *OC(1st Tier) Dsg*. This is a buffer time allotted for a 1st tier Over Current in the discharge direction condition. The timer starts every time [OCD] in ***Safety Alert*** is initially set. When the timer expires, the bq20z80 forces an [OCD] Alarm in ***Safety Status*** and opens the Discharge FET. If [OCD] in Safety Alert clears prior to the expiration of the *OC (1st Tier) Time Dsg* timer, then the [OCD] in ***Safety Alert*** is cleared and the *OC (1st Tier) Time Dsg* timer resets. Setting the *OC (1st Tier) Time Dsg* to 0 disables *OC (1st Tier) Dsg*.

Normal Setting: This is normally set to 2 seconds, but depends on the application. It should be set long enough to prevent false triggering of the [OCD] in *Safety Status*, but short enough to prevent damage to the battery pack.

OC Dsg Recovery

OC Dsg Recovery is one of several recovery methods used for both 1st and 2nd level Over Current in the discharge direction Faults. This value is used for either nonremovable packs ([NR] in *Operation Cfg B = 1*) or for removable packs configured ([OCD] in *Non-Removable Cfg*). With either of these settings, ***Average Current*** must rise **above** this value for *Current Recovery Timer* in seconds to clear the [OCD] or the [OCD2] in ***Safety Status*** if either is set.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent but is normally set **high** enough that it prevents quick oscillation in the Discharge FET. ***Average Current*** is used for this recovery function and moves closer to 0 every second that it is recomputed with *Current* at or near 0. If this recovery is set too *low*, then the Discharge FET can oscillate with a frequency that is fast enough to cause damage to the battery pack because the ***Average Current*** moves **above** this value quickly.

OC (2nd Tier) Chg

When current measured by ***Current*** reaches up to or above this threshold during charging then the 2nd Tier Over Current in Charge [OCC2] protection process is triggered, initiating an [OCC2] in ***Safety Alert*** for *OC (2nd Tier) Chg Time* in seconds. If the 2nd Tier Over Current condition clears prior to the expiration of the *OC (2nd Tier) Chg Time* timer, then [OCC2] in ***Safety Alert*** is cleared and no [OCC2] is set in ***Safety Status***. If the 2nd Tier Over Current condition does not clear, then a [OCC2] is set in ***Safety Status*** and the Charge FET is opened. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0.**Normal Setting:** This register is application dependent. It should be set above the *OC (1st Tier) Chg* threshold and should be set high enough that unexpected mild charge spikes or inaccuracies do not create a false over current trigger, but low enough to force the Charge FET to open before damage occurs to the pack.

Normal Setting: This register is application dependent. It should be set above the *OC (1st Tier) Chg* threshold and should be set high enough that unexpected mild charge spikes or inaccuracies do not create a false over current trigger, but low enough to force the Charge FET to open before damage occurs to the pack.

OC (2nd Tier) Time Chg

See *OC(2nd Tier) Chg*. This is a buffer time allotted for a 2nd Tier Over Current condition. The timer starts every time the [OCC2] is ***Safety Alert*** is initially set. When the timer expires then, the bq20z80 forces an [OCC2] in ***Safety Status*** and opens the Charge FET. If [OCC2] in ***Safety Alert*** clears prior to the expiration of the *OC (2nd Tier) Chg Time* timer, then [OCC2] in ***Safety Alert*** is cleared and the *OC (2nd Tier) Chg Time* timer resets. Setting the *OC (2nd Tier) Chg Time* to 0 disables *OC (2nd Tier) Chg*.

Normal Setting: This is normally set to 2 seconds, but depends on the application. It must be set long enough to prevent false triggering of the [OCC2] in ***Safety Status***, but short enough to prevent damage to the battery pack. It is common for the second level over current threshold to be disabled.

OC (2nd Tier) Dsg

When current measured by ***Current*** falls down to or below this threshold during discharging, then the 2nd Tier Over Current in discharge (OCD2) protection process is triggered, initiating an [OCD2] in ***Safety Alert*** for *OC (2nd Tier) Dsg Time* in seconds. If the 2nd Tier OCD2 condition clears prior to the expiration of the *OC (2ndTier) Dsg Time* timer, then the [OCD2] is cleared in ***Safety Alert*** and no [OCD2] alarm is set in ***Safety Status***. If the 2nd Tier OCD condition does not clear, then a [OCD2] is set in ***Safety Status*** and the Discharge FET is opened. This fault condition causes [XDSG] and [XDSGI] in ***Operation Status*** to be set. It also causes ***Charging Current*** to be set to 0.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent. It should be set **below** the *OC (1st Tier) Dsg* threshold and must be set **below** the absolute maximum expected discharge current. It must be set **low** enough that unexpected mild discharge spikes or inaccuracies do not create a false over current trigger, but **high** enough to force the Discharge FET open before damage occurs to the pack.

OC (2nd Tier) Time Dsg

See *OC (2nd Tier) Dsg*. This is a buffer time allotted for a 2nd Tier Over Current in the discharge direction condition. The timer starts every time [OCD2] in ***Safety Alert*** is initially set. When the timer expires, then the bq20z80 forces an [OCD2] alarm in *Safety Status* and opens the Discharge FET. If [OCD2] in ***Safety Alert*** clears prior to the expiration of the *OC (2nd Tier) Time Dsg* timer, then the [OCD] in ***Safety Alert*** is cleared and the *OC (2nd Tier) Time Dsg* timer resets. Setting the *OC (2nd Tier) Time Dsg* to 0 disables *OC (2nd Tier) Dsg*.

Normal Setting: This is normally set to 2 seconds but depends on the application. It must be set long enough to prevent false triggering of the [OCD2] in ***Safety Status*** but short enough to prevent damage to the battery pack.

Current Recovery Timer

The *Current Recovery Timer* is used in the recovery process of any of the over current fault conditions. After a fault condition exists, depending on if enabled, the fault condition is cleared only after *Current Recovery Timer* time in seconds with ***AverageCurrent*** falling below the corresponding recovery threshold in the charge direction or rising above the corresponding recovery threshold in the discharge direction. The corresponding recovery does not happen immediately after the recovery condition exits. As soon as the recovery condition exists then the *Current Recovery Timer* starts and the condition clears and the corresponding FET is enabled after the *Current Recovery Timer* expires. This timer is associated with the following Fault Conditions as described in this section:

1. *OC (1st Tier) Dsg*
2. *OC (1st Tier) Chg*
3. *OC (2nd Tier) Dsg*
4. *OC (2nd Tier) Chg*
5. *AFE OC Dsg*
6. *AFE SC Dsg*
7. *AFE SC Chg*

This Recovery method is enabled if [NR] is set in *Operation Cfg B*, or if ([NR] is cleared and the corresponding bits are set in the *Non-Removable Cfg* register:

1. *OC (1st Tier) Dsg* [OCD]
2. *OC (1st Tier) Chg* [OCC]
3. *OC (2nd Tier) Dsg* [OCD2]
4. *OC (2nd Tier) Chg* [OCC2]
5. *AFE OC Dsg* [AOCD]
6. *AFE SC Dsg* [SCD]
7. *AFE SC Chg* [SCC]

Normal Setting: The default for this register is 8 seconds. This is a recommended number to prevent heating up in the corresponding FET.

AFE OC Dsg

See the important note about all AFE fault conditions at the beginning of the **Current** section.

This is the third level Over Current protection in the discharge direction. This is a last effort protection function before using the Permanent Fail Functions in the Second Level Safety Class. This register displays in HEX using the EV Software. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If the *AFE OC DSG* condition exists for *AFE OC Dsg Time* in milliseconds, then the discharge FET opens as controlled by the bq29312A. This fault condition causes [AOCD] to be set in ***Safety Status*** and [XDSG], [XDSGI] is set in *Operation Status*, and [TDA] is set in ***Battery Status***. It also causes ***Charging Current*** to be set to 0. See Table 1 for settings for this register.

Table 1. AFE OC Dsg Configuration

0X00	**0.050 V**	**0x08**	**0.090 V**	**0x10**	**0.130 V**	**0x18**	**0.170 V**
0x01	**0.055 V**	**0x09**	**0.095 V**	**0x11**	**0.135 V**	**0x19**	**0.175 V**
0x02	**0.060 V**	**0x0a**	**0.100 V**	**0x12**	**0.140 V**	**0x1a**	**0.180 V**
0x03	**0.065 V**	**0x0b**	**0.105 V**	**0x13**	**0.145 V**	**0x1b**	**0.185 V**
0x04	**0.070 V**	**0x0c**	**0.110 V**	**0x14**	**0.150 V**	**0x1c**	**0.190 V**
0x05	**0.075 V**	**0x0d**	**0.115 V**	**0x15**	**0.155 V**	**0x1d**	**0.195 V**
0x06	**0.080 V**	**0x0e**	**0.120 V**	**0x16**	**0.160 V**	**0x1e**	**0.200 V**
0x07	**0.085 V**	**0x0f**	**0.125 V**	**0x17**	**0.165 V**	**0x1f**	**0.205 V**

Normal Setting: Note that the maximum value for this register is 0x1F. Values above 0x1F cause unpredictable results. This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required in determining the proper setting for this register. Be sure that this value is **below** the *OC (2nd Tier) Dsg*.

AFE OC Dsg Time

This is the time after detection of an *AFE OC Dsg* fault before the Discharge FET attempts to open. This trigger function is completely controlled by the bq29312A. The setting of this register is in HEX, and it is in milliseconds (See *AFE OC Dsg*). See Table 2 for setting for this register.

Table 2. AFE OC Dsg Time Configuration

0x00	**1 ms**	**0x04**	**9 ms**	**0x08**	**17 ms**	**0x0c**	**25 ms**
0x01	**3 ms**	**0x05**	**11 ms**	**0x09**	**19 ms**	**0x0d**	**27 ms**
0x02	**5 ms**	**0x06**	**13 ms**	**0x0a**	**21 ms**	**0x0e**	**29 ms**
0x03	**7 ms**	**0x07**	**15 ms**	**0x0b**	**23 ms**	**0x0f**	**31 ms**

Normal Setting: Note that the maximum value for this register is 0x0F. Values above 0x0F cause unpredictable results. This register is completely application specific. It should be set long enough to prevent false triggering of the [AOCD] in ***Safety Status***, but short enough to prevent damage to the battery pack.

AFE OC Dsg Recovery

See the important note about all AFE fault conditions at the beginning of the **Current** section.

AFE OC Dsg Recovery is one of several recovery methods used for *AFE OC Dsg Fault*. This value is used for either nonremovable packs ([NR] in *Operation Cfg B =1*) or for removable packs configured ([AOCD] in *Non-Removable Cfg*). With either of these settings, ***AverageCurrent*** must rise **above** this value for *Current Recovery Timer* in seconds to clear the [AOCD] in ***Safety Status*** if it is set.

Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent, but is normally set **high** enough that it prevents quick oscillation in the Discharge FET. If set to **low**, then the Discharge FET can oscillate with a frequency that is fast enough to still cause damage to the battery pack because the ***AverageCurrent*** moves **above** this value quickly.

AFE SC Chg Cfg

See the **NOTE** at the beginning of the Current section for an important note about all AFE fault conditions.

This register includes 2 settings. We will refer to these as *AFE SC Chg* and *AFE SC Chg Time*. This register displays in HEX using the EV Software. The most significant nibble (bits 4-7) sets the time for the AFE short circuit in the Charge direction fault detection time (*AFE SC Chg Time*). The least significant nibble (bits 0-3) set the threshold at which the bq29312A detects a AFE short circuit fault (*AFE SC Chg*). This is an extreme condition with settings for very large voltages and very short setting times for violent faults far above any of the other fault conditions because its intended purpose is to detect a short circuit condition before damage to the battery pack can occur. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If an AFE short circuit in the Charge direction fault exists for AFE short circuit in the Charge direction fault detection time in microseconds, then the Charge FET opens as controlled by the bq29312A. This fault condition causes [SCC] to be set in ***Safety Status***, and [TCA] to be set in ***Battery Status***. It also causes ***Charging Current*** and ***Charging*** Voltage to be set to 0. See Table 4 for settings for this register.

Table 3. AFE SC Chg Cfg Bit Description

7	6	5	4	3	2	1	0
SCCT3	SCCT2	SCCT1	SCCT0	SCCV3	SCCV2	SCCV1	SCCV0
AFE SC Chg Time				*AFE SC Chg*			

Table 4. AFE SC Chg Cfg Least Significant Nibble (SCCV3-SCCV0)

0x00	**0.100 V**	**0x04**	**0.200 V**	**0x08**	**0.300 V**	**0x0c**	**0.400 V**
0x01	**0.125 V**	**0x05**	**0.225 V**	**0x09**	**0.325 V**	**0x0d**	**0.425 V**
0x02	**0.150 V**	**0x06**	**0.250 V**	**0x0a**	**0.350 V**	**0x0e**	**0.450 V**
0x03	**0.175 V**	**0x07**	**0.275 V**	**0x0b**	**0.375 V**	**0x0f**	**0.475 V**

Table 5. AFE SC Chg Cfg Most Significant Nibble (SCCT3-SCCT0)

0x00	**0 µs**	**0x04**	**244 µs**	**0x08**	**488 µs**	**0x0c**	**732 µs**
0x01	**61 µs**	**0x05**	**305 µs**	**0x09**	**549 µs**	**0x0d**	**793 µs**
0x02	**122 µs**	**0x06**	**366 µs**	**0x0a**	**610 µs**	**0x0e**	**854 µs**
0x03	**183 µs**	**0x07**	**427 µs**	**0x0b**	**671 µs**	**0x0f**	**915 µs**

Normal Setting: This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required in determining the proper setting for this register. Be sure that this value is sufficiently above *OC (2nd Tier) Chg*.

AFE SC Dsg Config

See the important note about all AFE fault conditions at the beginning of the Current section.

This register includes 2 settings. Refer to these as *AFE SC Dsg* and *AFE SC Dsg Time*. This register displays in HEX using the EV Software. The most significant nibble (bits 4–7) sets the time for the AFE short circuit in the discharge direction fault detection time (*AFE SC Dsg Time*). The least significant nibble (bits 0–3) sets the threshold at which the bq29312A detects an AFE short circuit fault in the discharge direction (*AFE SC Dsg*). This is an extreme condition with settings for large voltages and short setting times for violent faults far above any of the other fault conditions because its intended purpose is to detect a short circuit condition before damage to the battery pack can occur. Also note that this setting is in units of volts. It does not take into account the Sense resistor value. If an AFE short circuit in the Charge direction fault exists for AFE short circuit in the Charge direction fault detection time in microseconds, then the Discharge FET opens as controlled by the bq29312A. This fault condition causes [SCD] to be set in ***Safety Status***, [XDSG] and [XDSGI] to be set in ***Operation Status***, and [TDA] to be set in ***Battery Status***. See Table 7 and Table 8 for settings for this register.

Table 6. AFE SC Dsg Cfg Bit Description

7	6	5	4	3	2	1	0
SCDT3	SCDT2	SCDT1	SCDT0	SCDV3	SCDV2	SCDV1	SCDV0
AFE SC Dsg Time				*AFE SC Dsg*			

Table 7. AFE SC Dsg Cfg Least Significant Nibble (SCDV3-SCDV0)

0x00	**0.10 V**	**0x04**	**0.20 V**	**0x08**	**0.30 V**	**0x0c**	**0.40 V**
0x01	**0.125 V**	**0x05**	**0.225 V**	**0x09**	**0.325 V**	**0x0d**	**0.425 V**
0x02	**0.150 V**	**0x06**	**0.250 V**	**0x0a**	**0.350 V**	**0x0e**	**0.450 V**
0x03	**0.175 V**	**0x07**	**0.275 V**	**0x0b**	**0.375 V**	**0x0f**	**0.475 V**

Table 8. AFE SC Dsg Cfg Most Significant Nibble (SCDT3-SCDT0)

0x00	**0 µs**	**0x04**	**244 µs**	**0x08**	**488 µs**	**0x0c**	**732 µs**
0x01	**61 µs**	**0x05**	**305 µs**	**0x09**	**549 µs**	**0x0d**	**793 µs**
0x02	**122 µs**	**0x06**	**366 µs**	**0x0a**	**610 µs**	**0x0e**	**854 µs**
0x03	**183 µs**	**0x07**	**427 µs**	**0x0b**	**671 µs**	**0x0f**	**915 µs**

Normal Setting: This register is completely application specific. Its setting does not correspond to current, so a conversion using the application Sense Resistor value is required to determine the proper setting for this register. Be sure that this value is **below** AFE OC Dsg.

AFE SC Recovery

See the important note about all AFE fault conditions at the beginning of the **Current** section.

AFE SC Recovery is one of several recovery methods used for either a charge or discharge AFE short circuit fault. This value is used for either nonremovable packs ([NR] in *Operation Cfg B =1*) or for removable packs that this function is configured ([SCD] for discharge or [SCC] in charge in *Non-Removable Cfg*). With either of these settings, *AverageCurrent* must rise **above** this value (for discharge fault) or **below** this value (for charge fault) for *Current Recovery Timer* in seconds to clear the [SCD] or [SCC] in *Safety Status* if either is set.

Normal Setting: Care must be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This register is application dependent, but is normally set close to 0 mA to prevent quick oscillation in the Charge/Discharge FET. If it is set to far from 0 mA, then the Charge/Discharge FET oscillates with a frequency that is fast enough to cause damage to the battery pack because the *AverageCurrent* is within this threshold value too quickly.

Temperature

Over Temp Chg

When the pack temperature measured by ***Temperature*** rises to or above this threshold while charging (***Current***> *Chg Current Threshold*), then the Over Temperature in charge direction (OTC) protection process is triggered and [OTC] is set in ***Safety Alert*** for *OT Chg Time*. If the OTC condition clears prior to the expiration of the *OT Chg Time* timer, then the [OTC] is cleared in ***Safety Alert*** and no [OTC] is set in ***Safety Status***. If the condition does not clear, then [OTC] is set in ***Safety Status*** and if [OTFET] is set in *Operation Cfg B* the Charge FET is opened. If [OTFET] is not set in *Operation Cfg B*, then the Charge FET is not opened by this fault. This fault condition causes [TCA] and [OTA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0.

Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while charging and verify these setting are sufficient for the application temperature. The default is 55°C which should be sufficient for most Li-Ion applications.

OT Chg Time

See *Over Temp Chg*. This is a buffer time allotted for Over Temperature in the charge direction condition. The timer starts every time the [OTC] in ***Safety Alert*** is initially set. When the timer expires, the bq20z80 forces an [OTC] in ***Safety Status*** and opens the Charge FET if enabled with [OTFET] in *Operation Cfg B*. If [OTC] in ***Safety Alert*** clears (fault condition clears) prior to the expiration of the *OT Chg Time* timer, then [OTC] in ***Safety Alert*** is cleared and the *OT Chg Time* timer resets. Setting the *OT Chg Time* to 0 disables this function.

Normal Setting: This is normally set to 2 seconds which should be sufficient for most applications. Temperature is normally a slow acting condition that does not need high speed triggering. It must be set long enough to prevent false triggering of the [OTC] in ***Safety Status***, but short enough to prevent damage to the battery pack.

OT Chg Recovery

OT Chg Recovery is the temperature at which the battery recovers from an *OT Temp Chg* fault. This is the only recovery method for an *OT Temp Chg* fault.

Normal Setting: This register is application dependent, but is normally set low enough below the fault condition temperature to prevent quick oscillation in the Charge FET if it was opened with the fault. The default is 50°C which is a 5 degree difference which is sufficient to protect against oscillation during the transition between conditions.

Over Temp Dsg

When the pack temperature measured by ***Temperature*** rises to or above this threshold while discharging (***Current*** <(-)(*Dsg Current Threshold*)), then the Over Temperature in discharge direction (OTD) protection process is triggered and [OTD] is set in ***Safety Alert*** for *OT Dsg Time*. If the OTD condition clears prior to the expiration of the *OT Dsg Time* timer, then the [OTD] is cleared in ***Safety Alert*** and no [OTD] is set in ***Safety Status***. If the condition does not clear, then [OTD] is set in ***Safety Status*** and if [OTFET] is set in *Operation Cfg B* the Discharge FET is opened. If [OTFET] is not set in *Operation Cfg B* then the Discharge FET is not opened by this fault. This fault condition causes [TDA] and [OTA] in ***Battery Status*** to be set. It also causes ***Charging Current*** to be set to 0.

Normal Setting: This setting depends on the environment temperature and the battery specification. Verify the battery specification allows temperatures up to this setting while charging and verify these setting are sufficient for the application temperature. The default is 60°C which is sufficient for most Li-Ion applications. The default *Over Temp Dsg* setting is higher than the default *Over Temp Chg* because Li-Ion can handle a higher temperature in the discharge direction than in the charge direction.

OT Dsg Time

See *Over Temp Dsg*. This is a buffer time allotted for Over Temperature in the discharge direction condition. The timer starts every time the [OTD] in ***Safety Alert*** is initially set. When the timer expires, then the bq20z80 forces an [OTD] in ***Safety Status*** and opens the Discharge FET if enabled with [OTFET] in Operation Cfg B. If [OTD] in ***Safety Alert*** clears (fault condition clears) prior to the expiration of the *OT Dsg Time* timer, then [OTD] in ***Safety Alert*** is cleared and the *OT Dsg Time* timer resets. Setting the *OT Chg Time* to 0 disables this function.

Normal Setting: This is normally set to 2 seconds which is sufficient for most applications. Temperature is normally a slow acting condition that does not need high speed triggering. It should be set long enough to prevent false triggering of the [OTD] in ***Safety Status***, but short enough to prevent damage to the battery pack.

OT Dsg Recovery

OT Dsg Recovery is the temperature at which the battery recovers from an *OT Temp Dsg* fault. This is the only recovery method for an *OT Temp Dsg* fault.

Normal Setting: This register is application dependent, but is normally set low enough below the fault condition temperature to prevent quick oscillation in the Discharge FET if it was opened with the fault. The default is 55°C which is a 5 degrees difference which is sufficient to protect against this oscillation during the transition between conditions.

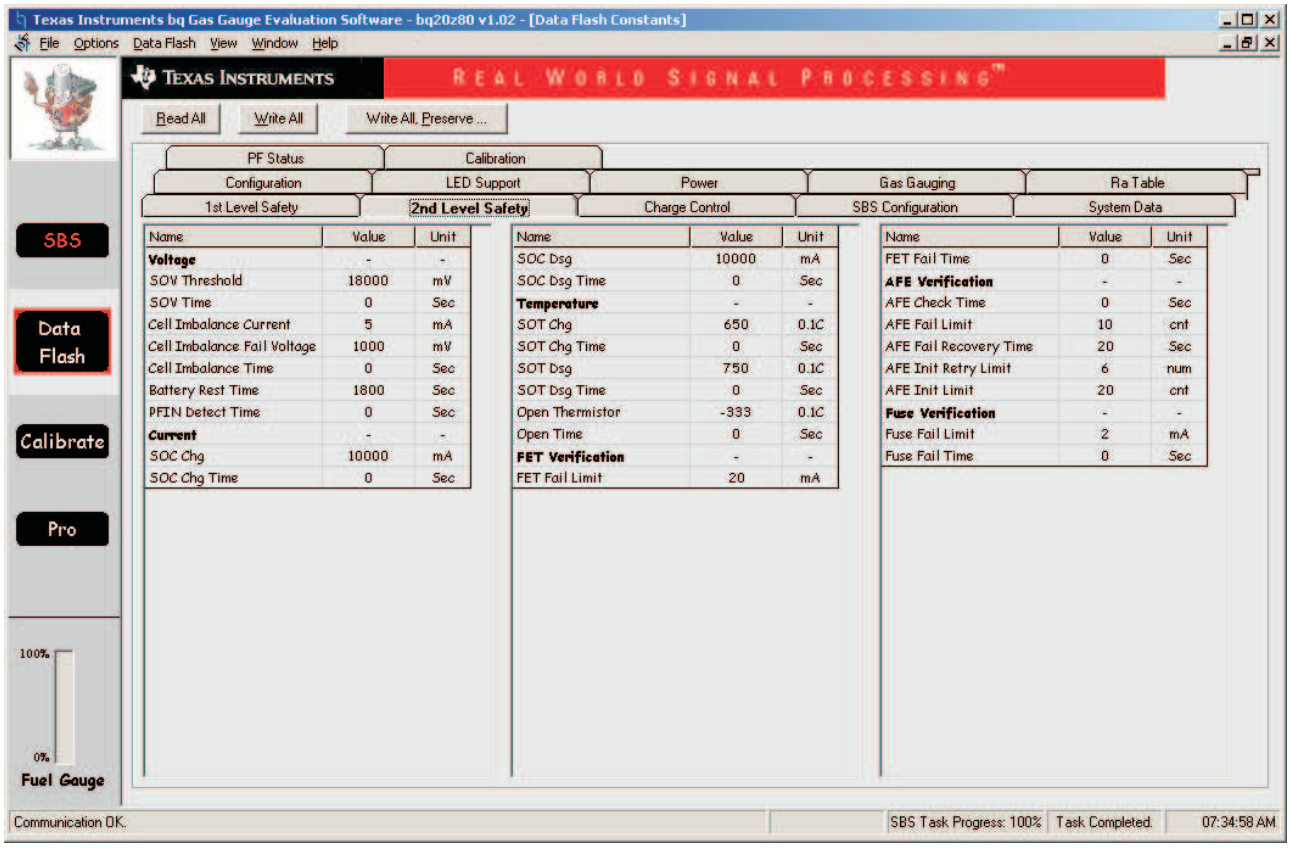
Host Comm

Host Watchdog Timeout

This function is only active when the bq20z80 is in Normal Power Mode (not asleep or in shutdown mode). It is also disabled if set to 0. If there is no communication to the bq20z80 via the SMBus for *Host Watchdog Timeout* time in seconds, then the bq20z80 reports [HWDG] set in ***Safety Status*** and opens the Charge, Discharge, and Pre-Charge FETs if enabled. This fault causes [TCA] and [TDA] in ***Battery Status*** to be set., and [XDSG] in ***Operation Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. It is difficult to monitor this function because any SMBus communication clears the fault condition. To monitor the function using SMBus, then the SMBus command that is used to clear the fault condition must be an SMBus read of ***Safety Status***. The [HWDG] flag is set on this read. Then on the next read (if its within the *Host Watchdog Timeout* window) the [HWDG] flag is cleared. The [HWDG] flag in ***Safety Alert*** as displayed in the EV Software is not used in this algorithm, and serves no purpose.

Normal Setting: This is not a common function and its default setting is 0. This provides another method for turning off the FETs, and preventing charge or discharge because the corresponding FETs are turned off when the fault occurs. It is also important to note that if the *Host Watchdog Timeout* is less than the *Bus Low Time*, then the fault condition occurs prior to the *Bus Low Timeout* which normally occurs prior to going to sleep. This function is disabled when in sleep mode, and the bq20z80 detects going to sleep mode as soon as the *Bus Low Timeout* expires. So, if the *Host Watchdog Timeout* timer expires prior to detecting bus low, then it triggers this fault.

2.3 2nd Level Safety



Name	Value	Unit
Voltage	-	-
SOV Threshold	18000	mV
SOV Time	0	Sec
Cell Imbalance Current	5	mA
Cell Imbalance Fail Voltage	1000	mV
Cell Imbalance Time	0	Sec
Battery Rest Time	1800	Sec
PFIN Detect Time	0	Sec
Current	-	-
SOC Chg	10000	mA
SOC Chg Time	0	Sec

Name	Value	Unit
SOC Dsg	10000	mA
SOC Dsg Time	0	Sec
Temperature	-	-
SOT Chg	650	0.1C
SOT Chg Time	0	Sec
SOT Dsg	750	0.1C
SOT Dsg Time	0	Sec
Open Thermistor	-333	0.1C
Open Time	0	Sec
FET Verification	-	-
FET Fail Limit	20	mA

Name	Value	Unit
FET Fail Time	0	Sec
AFE Verification	-	-
AFE Check Time	0	Sec
AFE Fail Limit	10	cnt
AFE Fail Recovery Time	20	Sec
AFE Init Retry Limit	6	num
AFE Init Limit	20	cnt
Fuse Verification	-	-
Fuse Fail Limit	2	mA
Fuse Fail Time	0	Sec

Voltage

SOV Threshold

This is a final level of protection. It is permanent. When the pack voltage measured by ***Voltage*** rises to this threshold, then the Safety Over Voltage (SOV) protection process is triggered. This process starts by setting [SOV] in ***PF Alert*** for *SOV Time*. If the SOV condition clears prior to the expiration of the *SOV Time* timer, then the [SOV] is cleared in ***PF Alert***, and no [SOV] is set in ***PF Status***. If the SOV condition does not clear, then [SOV] is set in ***PF Status***. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOV] in *Permanent Fail Cfg*, then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a voltage above the POV Threshold. This is meant to be a permanent condition, and it is recommended that [XSOV] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOV Time

See *SOV Threshold*. This is a buffer time allotted for an SOV condition. The timer starts after [SOV] is set in ***PF Alert***. When it expires, then the bq20z80 forces an [SOV] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOV Time* timer, then [SOV] is cleared in ***PF Alert***, and the *SOV Time* timer resets without setting [SOV] in ***PF Status***. If *SOV Time* is 0, then the *SOV Threshold* function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. Enabling this function in the final application is recommended . The most common values for this register are between 2–5 seconds.

Cell Imbalance Current

This is part of the safety cell imbalance detection algorithm. There are 4 registers that go together to make up this algorithm. *Cell Imbalance Current* is the value that ***Current*** must be below for the entire *Battery Rest Time* before Cell Imbalance detection is enabled. The bq20z80 does not start detecting a cell imbalance for this safety algorithm until the battery ***Current*** has been below this ***Cell Imbalance Current*** for at least the *Battery Rest Time*.

Normal Setting: This register should be set low to ensure the battery is completely relaxed when this algorithm is enabled. This Safety algorithm if triggered is permanent, and renders the battery useless. It is imperative that all data is valid prior to activation. The default setting is 5 mA which is sufficient for most applications.

Cell Imbalance Fail Voltage

This is part of the safety cell imbalance detection algorithm. For the purpose of this description:

Cell Voltage H = the highest SBS cell voltage

Cell Voltage L = the lowest SBS cell voltage

Delta Cell Voltage = ***Cell Voltage H*** - ***Cell Voltage L***

There are 4 registers that go together to make up this algorithm. After the *Battery Rest Time* portion of the Cell Imbalance algorithm has passed the test criteria (see *Battery Rest Time* and *Cell Imbalance Current*), then if ***Delta Cell Voltage*** is greater than the *Cell Imbalance Fail Voltage* in millivolts, then the *Cell Imbalance Fail Voltage* protection process is triggered. This process starts by setting [CIM] in ***PF Alert*** for *Cell Imbalance Time*. If the cell imbalance condition clears prior to the expiration of the *Cell Imbalance Time* timer, then the [CIM] is cleared in ***PF Alert*** with no [CIM] being set in ***PF Status***. If the cell imbalance condition does not clear, then [CIM] is set in ***PF Status***. This triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XCIM] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a voltage high enough to prevent any possibility of false triggering because this application is irreversible. This is meant to be a permanent condition and it is recommended that [XCIM] be set in Permanent Fail Cfg with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

Cell Imbalance Time

See *Cell Imbalance Fail Voltage*. This is a buffer time allotted for a cell imbalance safety condition. The timer starts after the *Battery Rest Time* has expired with current below the *Cell Imbalance Current* and ***Delta Cell Voltage*** (see *Cell Imbalance Fail Voltage*) is above the *Cell Imbalance Fail Voltage*. When the *Cell Imbalance Time* timer starts [CIM] is set in ***PF Alert***. When the timer expires, then the bq20z80 forces a [CIM] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *Cell Imbalance Time* timer, then [CIM] is cleared in ***PF Alert***, and the *Cell Imbalance Time* timer resets without setting [CIM] in ***PF Status***. The *Cell Imbalance Fail Voltage* function is disabled with *Cell Imbalance Time* equal to 0 or *Battery Rest Time* set to 0.

Normal Setting: This register defaults to 0. This disables the function. It is recommended that this function be enabled and the [XCIM] be enabled in *Permanent Failure Cfg* to protect against a potentially dangerous condition. *Battery Rest Time* helps prevent false triggering of this condition, so a good setting for Cell imbalance Time is 5 seconds. This gives several readings to ensure that the condition does exist.

Battery Rest Time

See *Cell Imbalance Current*. *Battery Rest Time* is the time in seconds that the battery ***Current*** must be below the *Cell Imbalance Current* for before Cell Imbalance detection is enabled. The bq20z80 does not start detecting a cell imbalance for this safety algorithm until the battery ***Current*** has been below *Cell Imbalance Current* for at least the *Battery Rest Time*. The *Cell Imbalance Fail Voltage* function is disabled with *Cell Imbalance Time* equal to 0 or *Battery Rest Time* set to 0.

Normal Setting: This register should be set for a relatively long time period to ensure the battery is completely relaxed when this algorithm is enabled. This safety algorithm, if triggered, is permanent and renders the battery useless. It is imperative that all data is valid prior to activation. The default setting is 1800 seconds which is sufficient for most applications.

PFIN Detect Time

This is a buffer time allotted for an $\overline{\text{PFIN}}$ safety condition. The timer *PFIN Detect Time* timer starts after the $\overline{\text{PFIN}}$ input pin has been set logic low by some external device (normally an external protector) which forces the [PFIN] is set in ***PF Alert***. When it expires, then the bq20z80 forces an [PFIN] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *PFIN Detect Time* timer, then [PFIN] is cleared in ***PF Alert***, and the *PFIN Detect Time* timer resets without setting [PFIN] in ***PF Status***. If *PFIN Detect Time* is 0, then this function is disabled. This fault condition triggers many permanent protection features as listed here:

1. The Charge FET , Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XPFIN] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

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Normal Setting: If this fault condition occurs then it is because an external device has already triggered a fault that should be nonrecoverable. This is meant to be a permanent condition, and it is recommended that [XPFIN] be set in *Permanent Fail Cfg*. If a fault occurs, and the external device sets the $\overline{\text{PFIN}}$ input low, the fuse will blow. If the fuse does not blow, then the bq20z80 attempts to blow the fuse (SAFE pin is set high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80). There is a clear function for this condition, but it is only intended to be used during the development process. The default for this function is 0. If the $\overline{\text{PFIN}}$ input is not used, then this function should be disabled. It is recommended that this function be used, and that [XPFIN] be set to ensure safe operation

Current

SOC Chg

SOC Chg is a final level of current protection from the bq20z80. This is not related to the 3rd level (AFE) protection which is a fast acting protection. It is also intended to be permanent. When the charge current as measured by ***Current*** rises to or above this threshold, then the Safety Over Current in the Charge direction (SOCC) protection process is triggered. This process starts by setting [SOCC] in ***PF Alert*** for *SOC Chg Time*. If the SOCC condition clears prior to the expiration of the *SOC Chg Time* timer, then the [SOCC] is cleared in ***PF Alert*** and with no [SOCC] being set in ***PF Status***. If the SOC condition does not clear, then [SOCC] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET ware all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOCC] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins is activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and should be set to a current above *OC(2nd Tier) Chg*. It is not necessarily required to set above *AFE OC Chg* which is a fast acting fault condition meant for high current spike detection. This function is meant to be a permanent condition, and it is recommended that [XSOCC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOC Chg Time

See *SOC Chg*. This is a buffer time allotted for an SOCC condition. The timer starts after [SOCC] is set in ***PF Alert***. When it expires, then the bq20z80 forces an [SOCC] in ***PF Status***, and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOC Chg Time* timer, then [SOCC] is cleared in ***PF Alert***, and the *SOC Chg Time* timer resets without setting [SOCC] in ***PF Status***. If *SOC Chg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2-5 seconds.

SOC Dsg

SOC Dsg is a final level of current protection from the bq20z80. This is not related to the 3rd level (AFE) protection which is a fast acting protection. It is also intended to be permanent. When the discharge current as measured by ***Current*** falls **down** to or **below** a negative of this threshold (–(*SOC Dsg*)), then the Safety Over Current in the discharge direction (SOCD) protection process is triggered. This process starts by setting [SOCD] in ***PF Alert*** for *SOC Dsg Time*. If the SOCC condition clears prior to the expiration of the *SOC Dsg Time* timer, then the [SOCD] is cleared in ***PF Alert*** with no [SOCC] being set in ***PF Status***. If the SOC condition does not clear, then [SOCD] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOCD] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class are filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: Care must taken when interpreting discharge descriptions in this document when

interpreting the direction and magnitude of the currents because they are in the negative direction. This is the last level of protection and must be set to a current below *OC(2nd Tier) Dsg*. It is not required to set above *AFE OC Dsg* which is a fast acting fault condition meant for high current spike detection. This is meant to be a permanent condition and it is recommended that [XSOCD] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOC Dsg Time

See *SOC Dsg*. This is a buffer time allotted for an SOCD condition. The timer starts after [SOCD] is set in ***PF Alert***. When it expires, then the bq20z80 forces an [SOCD] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOC Dsg Time* timer, then [SOCD] is cleared in ***PF Alert***, and the *SOC Dsg Time* timer resets without setting [SOCD] in ***PF Status***. If *SOC Dsg Time* is 0, then this function is disabled.
Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

Temperature

SOT Chg

SOT Chg is a final level of temperature protection from the bq20z80. This fault condition is intended to be permanent. When the temperature as measured by ***Temperature*** rises to or above this threshold while charging ([DSG] cleared in ***Battery Status***), then the Safety Over Temperature in the Charge direction (SOTC) protection process is triggered. This process starts by setting [SOTC] in ***PF Alert*** for *SOT Chg Time*. If the SOTC condition clears prior to the expiration of the *SOT Chg Time* timer, then the [SOTC] is cleared in ***PF Alert*** and with no [SOTC] being set in ***PF Status***. If the SOT condition does not clear, then [SOTC] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET ware all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOTC] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a temperature above *Over Temp Chg*. This is meant to be a permanent condition and it is recommended that [XSOTC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOT Chg Time

See *SOT Chg*. This is a buffer time allotted for a Safety Over Temperature Condition. The timer starts after [SOTC] is set in ***PF Alert***. When it expires, then the bq20z80 forces an [SOTC] in **PF Status** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOT Chg Time* timer, then [SOTC] is cleared in ***PF Alert***, and the *SOT Chg Time* timer resets without setting [SOTC] in **PF Status**. If *SOT Chg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

SOT Dsg

SOT Dsg is a final level of temperature protection from the bq20z80. This fault condition is intended to be permanent. When the temperature as measured by ***Temperature*** rises to or above this threshold while discharging ([DSG] set in ***Battery Status***), then the Safety Over Temperature in the discharge direction (SOTD) protection process is triggered. This process starts by setting [SOTD] in ***PF Alert*** for SOT Dsg Time. If the SOTD condition clears prior to the expiration of the *SOT Dsg Time* timer, then the [SOTD] is cleared in ***PF Alert*** and with no [SOTD] being set in ***PF Status***. If the SOT condition does not clear then [SOTD] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all be opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOTD] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This is the last level of protection and must be set to a temperature above *Over Temp Chg*. This is meant to be a permanent condition, and it is recommended that [XSOTC] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

SOT Dsg Time

See *SOT Dsg*. This is a buffer time allotted for a Safety Over Temperature Condition. The timer starts after [SOTD] is set in ***PF Alert***. When it expires, then the bq20z80 forces an [SOTD] in ***PF Status*** and opens the Charge FET Discharge FET and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *SOT Dsg Time* timer, then [SOTD] is cleared in ***PF Alert***, and the *SOT Dsg Time* timer resets without setting [SOTD] in ***PF Status***. If *SOT Dsg Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function must not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

Open Thermistor

Setting *Open Thermistor Time* to 0 disables this function. The *Open Thermistor* register is part of a thermistor circuit fault protection algorithm in the bq20z80 that detects an open circuit in the thermistor circuit because ***Temperature*** reaches impossible values due to open circuit ADC readings. This fault condition is intended to be permanent. When the temperature as measured by ***Temperature*** falls to or below this threshold, then the Open Thermistor protection process is triggered. This process starts by setting [OTS] in ***PF Alert*** for *Open Thermistor Time*. If the OTS condition clears prior to the expiration of the Open Thermistor Time timer, then the [OTS] is cleared in ***PF Alert*** and with no [SOTS] being set in ***PF Status***. If the OTS condition does not clear, then [OTS] is set in ***PF Status***. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XOTS] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: This function is a good safety feature that is particularly useful in detecting

thermistors that have come loose from the Gas Gauge PCB during the assembly process or if the wire of a thermistor comes lose from vibration. The value in this register does not need to be changed. This is meant to be a permanent condition, and it is recommended that [XOTS] be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

Open Thermistor Time

See *Open Thermistor*. This is a buffer time allotted for an Open Thermistor Condition. The timer starts after [OTS] is set in ***PF Alert***. When it expires, then the bq20z80 forces [OTS] set in **PF Status** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *Open Thermistor Time* timer, then [OTS] is cleared in ***PF Alert***, and the *Open Thermistor Time* timer resets without setting [OTS] in **PF Status**. If *Open Thermistor Time* is 0 then the *Open Thermistor* function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

FET Verification

FET Fail Limit

FET Fail Limit register is part of a FET circuit fault protection algorithm in the bq20z80 that detects potentially hazardous FET circuit damage. This fault condition is intended to be permanent, and has two possible trigger functions to help prevent confusion. The functions are listed separately.

1. If the Charge and Pre-Charge FET (if enabled) have been commanded to be off for any reason by either the bq20z80 or the bq29312A (any AFE fault condition) and charge current as measured by ***Current*** still exists which is greater than *FET Fail Limit* in milliamps, then the *FET Fail Limit* protection process is triggered. This process starts by setting [CFETF] in ***PF Alert*** for *FET Fail Time*. If the [CFETF] condition clears prior to the expiration of the *FET Fail Time* timer, then the [CFETF] is cleared in ***PF Alert*** and no [CFETF] is set in ***PF Status***. If the [CFETF] condition does not clear, then [CFETF] is set in ***PF Status***. This triggers many permanent protection features as listed below:
2. If the discharge FET has been commanded to be off for any reason by either the bq20z80 or the bq29312A (any AFE fault condition) and discharge current as measured by ***Current*** still exists which is less than or equal to (–) *FET Fail Limit* in milliamps, then the *FET Fail Limit* protection process is triggered. This process starts by setting [DFETF] in ***PF Alert*** for *FET Fail Time*. If the [DFETF] condition clears prior to the expiration of the *FET Fail Time* timer, then the [DFETF] is cleared in ***PF Alert*** and no [DFETF] is set in ***PF Status***. If the [DFETF] condition does not clear, then [DFETF] is set in ***PF Status***. This triggers many permanent protection features as listed below:

Each of the above triggers (A. and B.) cause the following permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if A and [XCFETF] or B and [XDFETF] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins is activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: The Charge and Discharge FETs arguably have more stress than any other component on the gas gauge PCB. This function is an excellent safety feature to help protect against the possibility of a shorted FET that is potentially hazardous. The default value in this register must be sufficient for most applications. This is meant to be a permanent condition, and it is recommended that [XCFETF] and [XDFETF] both be set in *Permanent Fail Cfg* with a fuse designed into the application. There is a clear function for this condition, but it is only intended to be used during the development process.

FET Fail Time

See *FET Fail Limit*. This is a buffer time allotted for the *FET Fail Limit* condition. The timer starts after either [CFETF] or [DFETF] set in ***PF Alert***. When the timer expires, then the bq20z80 forces the associated flag (either [CFETF] or [DFETF]) in ***PF Status*** and opens the Charge FET, Discharge FET, and Pre-Charge FET if they were on. If the condition clears prior to the expiration of the *FET Fail Time* timer, then the associated flag (either [CFETF] or [DFETF]) is cleared in ***PF Alert***, and the *FET Fail Time* timer resets without setting the associated flag (either [CFETF] or [DFETF]) in ***PF Status***. If *FET Fail Time* is 0 then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. This function should not be left at 0. Enabling this function in the final application is recommended. The most common values for this register are between 2–5 seconds.

AFE Verification

AFE Check Time

Every *AFE Check Time* in seconds, the bq20z80 reads all the bq29312A registers through the I^2C port that is shared between the 2 parts and compares the static register read results to the AFE data in the bq20z80's Data Flash. If they do not match, then the bq20z80 attempts to repair the corruption. Then increment an internal counter (referred to in this document as AFE_P Fail Counter) which triggers the periodic AFE_P Fail protection process. This process starts by setting [AFE_P] in ***PF Alert***. As long as the AFE_P Fail Counter stays below the *AFE Fail Limit* and above 0, [AFE_P] stays set in ***PF Alert***. See *AFE Recovery Time* for a recovery description. If *AFE Check Time* is set to 0, then the periodic AFE verification (AFE_P) is completely disabled.

Normal Setting: Setting **AFE Check Time** to 0 only disables the AFE_P verification function. It does not disable the AFE_C verification function as described in *AFE Fail Limit*. *AFE Check Time* set to 0 is acceptable because there is still the AFE_C verification process. If, however, AFE Check Time is used, set it above 20 seconds since the periodic test does not need to be done often to ensure the correct function.

AFE Fail Limit

There are 2 AFE safety features that use this register. They is separated here to help prevent confusion.

1. The first safety feature is a continuation of *AFE Check Time*. If the AFE_P Fail Counter (as described above) reaches the *AFE Fail Limit* then [AFE_P] is cleared in ***PF Alert***, and then set in ***PF Status***. Setting *AFE Fail Limit* to 0 does not disable the periodic AFE verification (AFE_P). (See *AFE Check Time*)
2. The second safety feature is not associated with *AFE Check Time*. Anytime a communication with the bq29312A is performed over the I^2C bus that is not part of the periodic check described in *AFE Check Time*, then a different internal counter (referred to in this document as AFE_C Fail Counter) increments. When the AFE_C Fail Counter increments, the AFE_C Fail protection process is triggered. This process starts by setting [AFE_C] in ***PF Alert***. As long as the AFE_C Fail Counter stays below the *AFE Fail Limit* and above 0, then [AFE_C] stays set in ***PF Alert***. See *AFE Recovery Time* for a recovery description. If the AFE_C Fail Counter reaches the *AFE Fail Limit*, then [AFE_C] is cleared in ***PF Alert***, and then set in ***PF Status***. Setting *AFE Fail Limit* to 0 disables the AFE_C Fail protection process.

Each of the above triggers (A. and B.) cause the following permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if A. [XAFE_P] set or if B and [XAFE_C] set in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the PF Status class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting:*AFE Fail Limit* defaults to 10. It is very important to note that setting *AFE Fail Limit* to 0 only disables the AFE_C functions. AFE_P functions are not disabled with the *AFE Fail Limit* set to 0. This results in [AFE_P] flag getting set in ***PF Status*** on the first failure which is not recommended. The default of 10 is appropriate for most applications. This gives sufficient buffer for ESD, resets and other unknown failures that should be recoverable.

AFE Fail Recovery Time

See *AFE Check Time* and *AFE Fail Limit*. *AFE Fail Recovery Time* function works independently with each of the AFE counters described above (AFE_C Fail Counter and AFE_P Fail Counter). While [AFE_C] or [AFE_P] is set in ***PF_Alert***, every *AFE Fail Recover Time* period in seconds AFE_C Fail Counter and/or AFE_P Fail Counter is decremented by 1 until each reaches 0. As soon as they are decremented back to 0, their associated flags ([AFE_C] or [AFE_P]) are cleared in ***PF Alert***, and the fault process is reversed.

Normal Setting: It is recommended that this register be set less than *AFE Check Time*, so that at least one recovery process can occur between periodic checks. *AFE Init Retry Limit*

This description is for reference only. The bq20z80 uses its internal ADC to measure initial AFE (bq29312A) offsets and gain values on every reset. The quality of these readings are critical to the accuracy of the voltage as displayed by ***Voltage*** and ***Cell Voltage(All)***. Poor initial offset and gain readings can alter the voltage displayed, and it can take several minutes to reacquire accurate readings due to an internal slow responding digital filter in the bq20z80 firmware. With the importance of the quality of these initial readings, the bq20z80 takes 2 successive readings of these offsets and gain values, and compare them. If the comparison fails to meet the criteria as set by *AFE Init Limit* (see below), then the bq20z80 retries this procedure *AFE Init Retry Limit* times before it forces an AFE_C permanent failure. This triggers many permanent protection features:

1. The Charge FET, Discharge FET, and Pre-Charge FET are all opened.
2. [TCA] and [TDA] in ***Battery Status*** is set
3. ***Charging Current*** and ***Charging Voltage*** is set to 0.
4. Data Flash Writes is disabled
5. if [XSOV] in *Permanent Fail Cfg* then
   - 0x3672 is programmed to the *Fuse Flag*.
   - The Safety Output pins are activated which is intended to blow a fuse.
6. All the remaining data flash registers in the **PF Status** class is filled with backups of many of the SBS data set registers and AFE data.

Normal Setting: Modifying this register is not recommended; however, if unexplained AFE_C failures occur after resets, then this might be the function that caused the failure. Increasing this value can help, but the problem is normally a noisy environment due to switching from radio frequencies or PCB layout.

AFE Init Limit

This description is only for reference. This data flash location should never be modified. The bq20z80 uses its internal ADC to measure initial AFE (bq29312A) offsets and gain values on every reset. The quality of these readings are critical to the accuracy of the voltage as displayed by ***Voltage*** and ***Cell Voltage(All)***. Poor initial offset and gain readings can alter the voltage displayed, and it can take several minutes to reacquire accurate readings due to an internal slow responding digital filter in the bq20z80 firmware. With the importance of the quality of these initial readings, the bq20z80 takes multiple readings (see *AFE Init Retry Limit* above) of these offsets and gain values, and compare them. The *AFE Init Limit* is the maximum difference in successive respective offset and gain value comparisons allowed for the values to be declared accurate. (Gain reading 2–Gain reading 1) must be below *AFE Init Limit*, (Offset reading 2–Offset reading 1) must be below *AFE Init Limit etc*.

Normal Setting: This register is in a reserved unit format; therefore, it is recommended that this value not be modified. It should be acceptable for most applications except for poor PCB layouts and noisy environments which affect voltage measurements. If this occurs, contact Texas Instruments for the value to put in this register.

Fuse Verification

Fuse Fail Limit

Fuse Fail Limit register is part of a Fuse circuit fault protection algorithm in the bq20z80 that detects potentially hazardous conditions. The *Fuse Fail Limit* is used in both the charge and the discharge direction. If the *Fuse Flag* has been set to 0x3672 (SAFE pin is set high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80) and the current as measured by ***Current*** still exists which is greater than *Fuse Fail Limit* in milliamps, or less than a (–) *Fuse Fail Limit* then the *Fuse Fail Limit* protection process is triggered. This process starts by setting [FBF] in ***PF Alert*** for *Fuse Fail Time*. If the [FBF] condition clears prior to the expiration of the *Fuse Fail Time* timer, then the [FBF] is cleared in ***PF Alert*** and no [FBF] is set in ***PF Status***. If the [FBF] condition does not clear, then [FBF] is set in ***PF Status***. This causes the normal Permanent Failure conditions except that with this function they are already set. This function only works with an existing permanent failure.

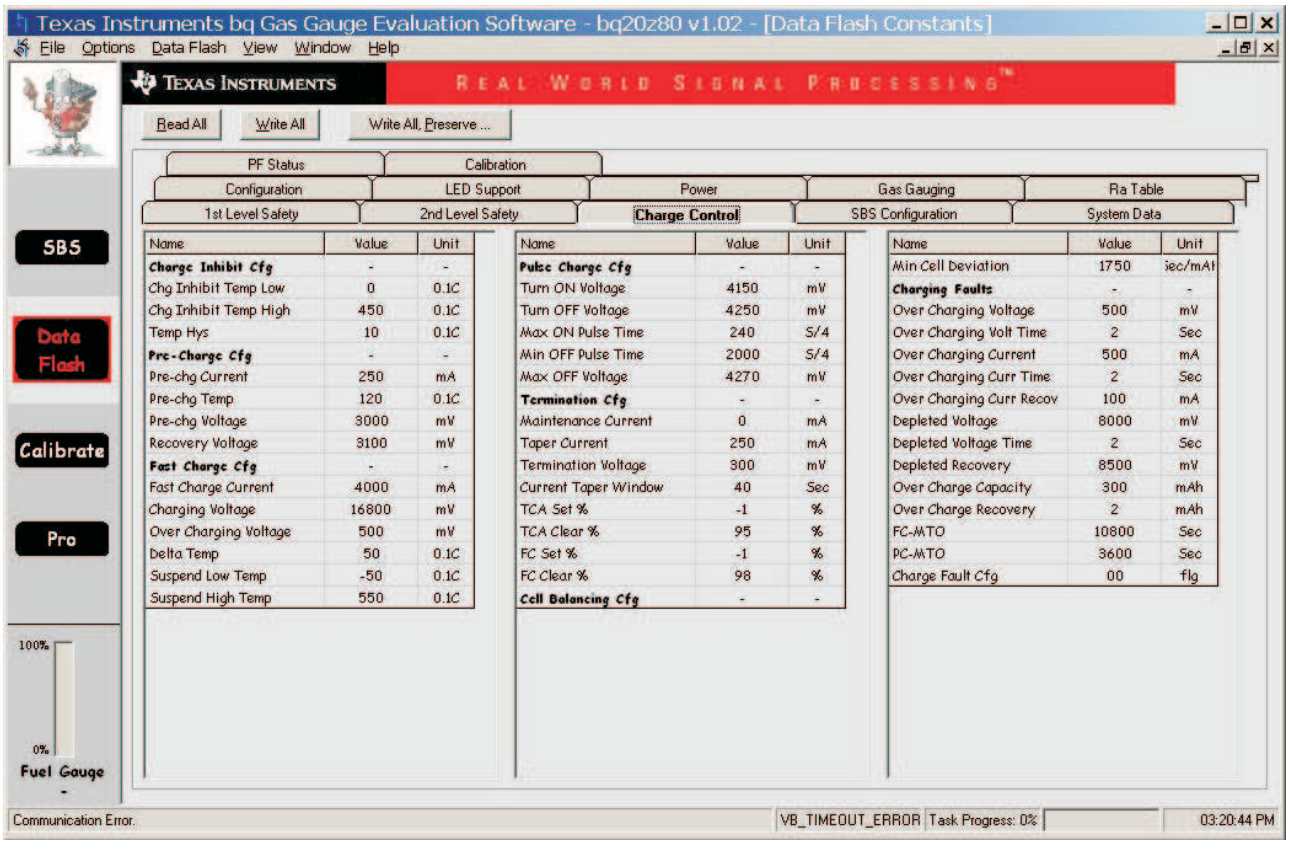
Normal Setting: The purpose of this function is for reporting and retaining the fact that the fuse was supposed to blow but did not. The fact that it causes an [FBF] flag being set in ***PF Status*** serves no purpose except for this fact being recorded for future data retrieval since the fuse was already supposed to be blown. The hope is that the bq20z80 will survive this potentially violent failure enough to be sent to the factory so that the Data Flash that this information was stored in can be read and analyzed to determine the cause of the failure. If the bq20z80 does not survive then this information is useless.

Fuse Fail Time

See *Fuse Fail Limit*. This is a buffer time allotted for the *Fuse Fail Limit* condition. The timer starts after [FBF] is set in ***PF Alert***. When the timer expires, then the bq20z80 forces [FBF] in ***PF Status***. If the condition clears prior to the expiration of the *Fuse Fail Time* timer, then [FBF] is cleared in ***PF Alert*** and the *Fuse Fail Time* timer resets without setting [FBF] in ***PF Status***. If *Fuse Fail Time* is 0, then this function is disabled.

Normal Setting: This register defaults to 0 only for the development process. The only purpose of this function is to report that a fuse was instructed to blow and did not. The bq20z80 may not survive to report this information but it is possible. It is an uncommon event unless the fuse blow circuit design is faulty. The most common values for this register are between 2–5 seconds.

2.4 Charge Control



Charge Inhibit Config

Chg Inhibit Temp Low

When the pack temperature measured by ***Temperature*** falls to or below this threshold while discharging ([DSG] flag set in ***Battery Status***), the Charge Inhibit Mode is triggered. This causes ***Charging Current*** and ***Charging Voltage*** to be set to 0, [XCHG] is set in ***Charging Status***, and if [CHGIN] set in *Operation Cfg B*, then Charge FET is turned off and/or the Pre-Charge FET is turned off. There are two primary possible recoveries to this mode.

1. The primary recovery is if ***Temperature*** rises above (*Charge Inhibit Temp Low + Temp Hys*).
2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the inhibit mode is reactivated with [DSG] flag set in ***Battery Status***.

With either of these recoveries, [XCHG] is cleared in ***Charging Status***. This enables the charging process to initiate.

Normal Setting: The purpose of this low inhibit temperature is not to suspend charging, but to prevent it from starting when the conditions are not acceptable, This prevents damage to the pack. The default for this is 0 degrees, and can be modified to fit the application.

Chg Inhibit Temp High

When the pack temperature measured by ***Temperature*** rises to or above this threshold while discharging ([DSG] flag set in ***Battery Status***) the Charge Inhibit Mode is triggered. This causes Charging Current and Charging Voltage to be set to 0, [XCHG] is set in ***Charging Status***, and if [CHGIN] set in *Operation Cfg B* then Charge FET is turned off and/or the Pre-Charge FET is turned off. There are two primary possible recoveries to this mode.

1. The primary recovery is if ***Temperature*** falls below (*Charge Inhibit Temp Low – Temp Hys*).

2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists then, the inhibit mode is reactivated with [DSG] flag set in ***Battery Status***.

With either of these recoveries, [XCHG] is cleared in ***Charging Status***. This enables the charging process to initiate.

Normal Setting: The purpose of this high inhibit temperature is not to suspend charging but to prevent it from starting when the conditions are not acceptable. This prevents damage to the pack. The default for this is 45°. Notice that this is less than the default charge suspend mode (see *Suspend High Temp*).

Temp Hys

This register works with both *Chg Inhibit High* and *Chg Inhibit Low* in the recovery process.

1. With charge inhibited resulting from a high temperature and if ***Temperature*** falls below (*Charge Inhibit Temp High – Temp Hys*), then the [XCHG] is cleared in ***Charging Status***. This enables the charging process to initiate.
2. With charge inhibited resulting from low temperature and if ***Temperature*** rises above (*Charge Inhibit Temp Low + Temp Hys*), then the [XCHG] is cleared in ***Charging Status***. This enables the charging process to initiate.

Normal Setting: this register defaults to 1°C. For most applications, this is considered low for a hysteresis value. This register should be set to at least 2°C to 3°C to prevent oscillation of this condition.

Pre-Charge Config

Pre-Charge Current

This is the current that the bq20z80 reports in the ***Charging Current*** register when the bq20z80 is in Pre-Charge mode (see *Pre-Chg Temperature* and *Pre-Chg Voltage*). This current is broadcast to a smart charger when bq20z80 master mode broadcasts are enabled ([BCAST] set in *Operation Cfg B*). When in Pre-Charge Mode (***Charging Current*** = *Pre-Charge Current*), [PCHG] is set in ***Charging Status***, then the appropriate charging FET is enabled as set with [ZVCHG1] and [ZVCHG0] in *Operation Cfg A*.

ZVCHG1	ZVCHG0	FET Used
0	0	ZVCHG
0	1	CHG
1	0	OD
1	1	No Action

There are three primary recoveries from Pre-Charge mode:

1. Independent of the method (*Pre-Chg Voltage* or *Pre-Chg Temperature*) that caused the Pre-Charge Mode:
   a. ***Cell Voltage (All)*** must be above *Recovery Voltage*
   b. ***Temperature*** must be above (*Pre Chg Temperature + Temp Hys*)

   Either of these conditions cause the bq20z80 to enter Fast Charge Mode (See *Fast Charge Current*)
2. Pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the inhibit mode is reactivated with any of the Pre-Charge criteria.
3. This is considered a recovery, but it is really a transition from one mode to another. A charge suspend condition (see *Suspend High Temp* and *Suspend Low Temp*) which forces the bq20z80 to transition from Pre-Charge Mode to Charge Suspend Mode.

Normal Setting: This register is application dependent. If a Pre-Charge FET and a current limiting resistor is used to control the current allowed into the battery during Pre-Charge Mode ([ZVCHG1] and [ZVCHG1] both equal 0), then this register accuracy is not as important as if it were used for a smart charger which initiate a current equal to the requested Pre-Charge current. It is important to note that use of the OD pin is not recommended because it does not have limiting circuitry to ensure "hard" on control for a Zero Volt charging condition. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is always recommended.

Pre-Chg Temperature

See *Pre-Charge Current*. With either the *Pre-Chg Voltage* or the *Pre-Chg Temperature* criteria being met, then the bq20z80 triggers Pre-Charge Mode. With ***Temperature*** falling to or below *Pre-Chg Temperature*, but above Charge Inhibit Temp Low, then the bq20z80 enters the Pre-Charge Mode (see *Pre-Charge Current*).

Normal Setting: Ensure that this register is above the *Charge Inhibit Temp Low* . This ensures that *Pre-Chg Temperature* is above the charge suspend temperature because the charge suspend is below the charge inhibit. (See *Charge Inhibit Temp Low* and *Charge Suspend Temp Low*). At cold temperatures, lower currents are better for the battery cells. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is recommended.

Pre-Chg Voltage

See *Pre-Charge Current*. With either the *Pre-Chg Voltage* or the *Pre-Chg Temperature* criteria being met, then the bq20z80 triggers Pre-Charge Mode. With ***Cell Voltage (Any)*** falling to or below *Pre-Chg Voltage*, then the bq20z80 enters Pre-Charge Mode (see *Pre-Charge Current*).

Normal Setting: Ensure that this voltage is set per the battery cell specifications. Setting this value too high is not harmful (except for slower charging from empty), but setting this value too low can damage cells. This register gives the cells a chance for a Pre-Charge voltage which brings them up to a normal charging voltage before hitting them with a fast current. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is recommended.

Recovery Voltage

If the battery pack is in Pre-Charge mode due to ***Cell Voltage (Any)*** falling to or below *Pre-Chg Voltage*, then it exits the Pre-Charge mode and enter the Fast Charge Mode (see *Fast Charge Current*) when ***Cell Voltage (All)*** rises above *Recovery Voltage*. This is one of three primary recovery methods for a battery pack in Pre-Charge mode.

Normal Setting: This is battery cell dependent. Ensure that it is set per the battery cell specifications. Setting this value too high is not harmful (except for slower charging from empty), but setting this value too low can damage cells. This register gives the cells a chance for a Pre-Charge voltage which brings them up to normal charging voltage before hitting them with a fast current. Use of a Pre-Charge FET or smart charger that supports low Pre-Charge currents is recommended.

Fast Charge Config

Fast Charge Current

This is the current that the bq20z80 reports in the ***Charging Current*** register when the bq20z80 is in Fast Charge mode (see *Pre-Chg Temperature*, *Pre-Chg Voltage*, and *Pre-Chg Current*). This current is also broadcast to a smart charger when bq20z80 master mode broadcasts are enabled ([BCAST] set in *Operation Cfg B*). When in Fast Charge Mode (***Charging Current*** = *Fast Charge Current*), [FCHG] is set in ***Charging Status*** and the Charge FET is enabled There are three primary criteria that must be met to be in Fast Charge Mode:

1. Assuming all temperature faults are configured correctly (*Pre-Chg Temperature* configured in Data Flash as the highest low temperature mode), ***Temperature*** is above *Pre-Chg Temperature* with [PCHG] clear in ***Charging Status***
2. ***Temperature*** is below *Suspend High Temp* and no [CHGSUSP] in ***Charging Status***
3. ***Voltage*** must be above *Pre-Chg Voltage* with [PCHG] clear in ***Charging Status***
4. ***Voltage*** must be below ***Charging Voltage*** + *Over Charging Voltage*

While in Fast Charge Mode, there is an option called Charge Throttling that is enabled/disabled by *Delta Temperature* as described below (See *Delta Temperature*).

Normal Setting: This register is application dependent. It depends on the battery cell specifications, the battery Gas Gauge circuit current handling ability, and the charger output current.

Charging Voltage

When in any charging mode without a fault condition present, the *Charging Voltage* is the voltage that is put in ***Charging Voltage***. With most fault conditions ***Charging Voltage*** is set to 0. This is also used in bq20z80 charge qualification and termination algorithms.

Normal Setting: This register is normally set based on the charger specifications. Charger tolerances are considered when setting this register.

Over Charging Voltage

THIS REGISTER IS NOT USED BY THE bq20z80. IT IS REMOVED FROM FUTURE VERSIONS. It is not used because there is an *Over Charging Voltage* register in the **Charging Faults** subclass as described in that section.

Delta Temp

Delta Temp is used in a "throttling" algorithm for maximizing the charging algorithm. This description starts in Fast Charge Mode with Temperature in the normal range and ***Charging Current*** = *Fast Charge Current*. The value that is in ***Charging Current*** is broadcast to smart chargers if master mode broadcasts are enabled ([BCAST] set in *Operation Cfg B*)

1. When the ***Temperature*** rises to (*Suspend High Temp – (Delta Temp* $\times$ *2*)) then the bq20z80 initiates stage 2 throttling. In this mode, the ***Charging Current*** register is changed from *Fast Charge Current* to (*Fast Charge Current –Pre-Chg Current)* / 2. Also, [TCHG2] is set in ***Charging Status***. The purpose of this stage is to request a slower ***Charging Current*** to prevent overheating of the battery. If Temperature continues to climb then see step B).
2. If the ***Temperature*** continues to rise even though the ***Charging Current*** was decreased, then when the ***Temperature*** rises to (*Suspend High Temp – Delta Temp*), the bq20z80 initiates stage 1 throttling. In this mode, the ***Charging Current*** register is changed from [(*Fast Charge Current – Pre-Chg Current*) / 2] to *Pre-Chg Current*. Also [TCHG1] is set in ***Charging Status*** and [TCHG2] is cleared.
3. If the ***Temperature*** continues to climb, then it reaches the *Suspend High Temp* which halts charging completely. (see *Suspend High Temp*).

The battery returns to Fast Charge Mode when the temperature falls back below (*Suspend High Temp – (Delta Temp*$\times$ 2)) which clears [TCHG1] and [TCHG2] in ***Charging Status***. If *Delta Temp* is set to 0, then this function is disabled.

Normal Setting: Ensure that this value is large enough to keep the battery from switching modes rapidly; however, setting it to high increases the charging time and reduces the algorithms effectiveness. This register is only required in either high temperature environments, or with extreme charge currents.

Suspend Low Temp

When the pack temperature measured by ***Temperature*** falls to or below *Suspend Low Temp* while charging ([DSG] flag clear in ***Battery Status***), then the Charge Suspend Mode is triggered. This causes ***Charging Current*** to be set to 0, [CHGSUSP] is set in ***Charging Status***, and if [CHGSUSP] set in *Operation Cfg B*, then the Charge FET and Pre-Charge FET are both opened regardless of their prior open/close state. There are two primary possible recoveries to this mode

1. The primary recovery is if ***Temperature*** rises above (*Suspend Low Temp* + *Temp Hys*).
2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the suspend mode is reactivated with [DSG] flag cleared in ***Battery Status***.

With either of these recoveries, [CHGSUSP] is cleared in ***Charging Status***. This enables the charging process to resume.

Normal Setting: Notice that default *Suspend Low Temp* is lower than *Chg Inhibit Low Temp*. This value is application and battery cell dependent.

Suspend High Temp

When the pack temperature measured by ***Temperature*** rises to or above *Suspend High Temp* while charging the ([DSG] flag in ***Battery Status***), then the Charge Suspend Mode is triggered. This causes ***Charging Current*** to be set to 0, [CHGSUSP] is set in ***Charging Status***, and if [CHGSUSP] set in *Operation Cfg B*, then the Charge FET and Pre-Charge FET are both opened regardless of their prior open/close state. There are two primary possible recoveries to this mode.

1. The primary recovery is if ***Temperature*** falls below (*Suspend High Temp – Temp Hys*).
2. The condition is also cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*. If the condition still exists, then the suspend mode is reactivated with [DSG] flag cleared in ***Battery Status***.

With either of these recoveries, [CHGSUSP] is cleared in ***Charging Status***. This enables the charging process to resume.

Normal Setting: Notice that default *Suspend High Temp* is higher than *Chg Inhibit High Temp*. This value is application and battery cell dependent.

Pulse Charge Config

Pulse Charge Config is one of the most confusing setups in the bq20z80. In application, however, it is a relatively simple function. When charging, these settings can be used to turn ON and OFF the Charge FET to provide a pulse charging function. Figure 6 shows an example of a pulse charging voltage vs time wave form with all the Pulse Charge Config registers explained graphically.

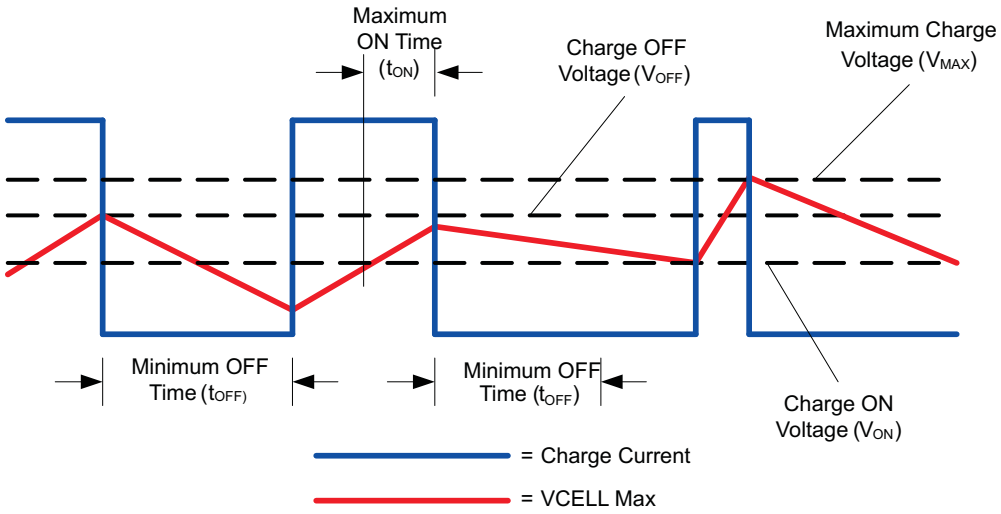


Figure 6. Pulse Charging Voltage vs Time

Turn Off Voltage

While charging ([DSG] clear in ***Battery Status***) and in Fast Charge Mode ([FCHG] set in ***Charging Status***), when ***Cell Voltage (MAX)*** rises to or above *Turn Off Voltage*, then the *Max On Pulse Time* timer initiates (see *Max On Pulse Time* for the rest of this process). If *Max On Pulse Time* is set to 0, then the process acts as if the *Max On Pulse Time* timer expired immediately (see *Max On Pulse Time* for the rest of this process).

Normal Setting: This is application dependent, if Pulse Charging is required, then *Turn Off Voltage* should be set below *Max Off Voltage* so that *Max On Pulse Time* is given time to expire throughout most of each charge cycle. This maximizes charge efficiency.

This explanation is continued from *Min Off Pulse Time* (see *Min Off Pulse Time*). While charging ([DSG] clear in ***Battery Status***) and in Fast Charge Mode ([FCHG] set in ***Charging Status***), the *Min Off Pulse Time* timer is initiated as soon as the Charge FET opens. Regardless of whether or not the ***Cell Voltage (MAX)*** falls below the *Turn On Voltage*, the *Min Off Pulse Time* timer must expire before the bq20z80 allows the Charge FET to be closed, and allows charge current to flow. If *Min Off Pulse Time* timer expires prior to ***Cell Voltage (MAX)*** falling below *Turn On Voltage*, the Charge FET is not closed until ***Cell***

Voltage (MAX) reaches *Turn On Voltage*. When the Charge FET is closed, then [PLSOFF] is cleared in ***Charging Status***.

Normal Setting: This is battery cell specification specific. See the Cell manufacturer data sheet for maximum voltage allowed. Note that the cell voltage readings for this algorithm are updated every 250 ms when in pulse charging mode instead of 1 second updates with ***Cell Voltage (ALL)***.

Max On Pulse Time

This explanation is continued from *Turn Off Voltage* above (see *Turn Off Voltage*). While charging ([DSG] clear in ***Battery Status***) and in Fast Charge Mode ([FCHG] set in ***Charging Status***), when ***Cell Voltage (MAX)*** rises to or above *Turn Off Voltage*, then the *Max On Pulse Time* timer initiates. If *Max On Pulse Time* is set to 0, then the process acts as if the *Max On Pulse Time* timer expired immediately. The expiration of the *Max On Pulse Time* timer forces the Charge FET to open, [PLSOFF] and [PULSE] to be set in ***Charging Status***, and the *Min Off Pulse Time* timer to be initiated (See *Min Off Pulse Time*). If *Max On Pulse Time* timer does not expire prior to ***Cell Voltage (MAX)*** reaching *Max Off Voltage*, then *Max Off Voltage* forces the Charge FET to open (See *Max Off Voltage*).

Normal Setting:

This register should be set to such a time that the Charge FET will shut off by this timer most of the time and not by the *Max Off Voltage*. It is not uncommon for this register to be 0 which would only use the *Max Off Voltage* for turning off the Charge FET. Care should be taken when setting it to 0 to ensure that the voltage does not overrun enough to produce a COV condition. The default for this register is 240 ms. This register is in units of Seconds/4 or 250 ms which is one minute.

Min Off Pulse Time

This explanation is continued from one of the following condition descriptions.

1. *Max On Pulse Time*
2. *Max Off Voltage*
3. *Turn Off Voltage*

While charging ([DSG] clear in ***Battery Status***) and in Fast Charge Mode ([FCHG] set in ***Charging Status***), the *Min Off Pulse Time* timer is initiated as soon the Charge FET opens from one of these listed conditions (1–3 above). Regardless of whether or not the ***Cell Voltage (MAX)*** falls below the *Turn On Voltage*, the *Min Off Pulse Time* timer must expire before the bq20z80 allows the Charge FET to be closed, and allows charge current to flow. If *Min Off Pulse Time* timer expires prior to ***Cell Voltage (MAX)*** falling below *Turn On Voltage*, the Charge FET is not closed until ***Cell Voltage (MAX)*** reaches *Turn On Voltage* (see *Turn On Voltage*).

Normal Setting: This register defaults to 0. This is a buffer to prevent fast oscillation of the Charge FET.

Max Off Voltage

This explanation is continued from *Max On Pulse Time* above (see *Max On Pulse Time*). While charging ([DSG] clear in ***Battery Status***) and in Fast Charge Mode, when ***Cell Voltage (MAX)*** rises to or above *Turn Off Voltage*, then the *Max On Pulse Time* timer initiates. If *Max On Pulse Time* timer does not expire prior to ***Cell Voltage (MAX)*** reaching *Max Off Voltage* then *Max Off Voltage* forces the Charge FET to open, [PLSOFF] and [PULSE] to be set in ***Charging Status***, and the *Min Off Pulse Time* timer to be initiated (See *Min Off Pulse Time*).

Normal Setting: This is battery cell specification specific. See the Cell manufacturer data sheet for maximum voltage allowed. Note that the cell voltage readings of this algorithm are updated every 250 ms when in pulse charging mode instead of 1 second updates with ***Cell Voltage (ALL)***.

Termination Config

Maintenance Current

Maintenance Current is only put into the ***Charging Current*** register when [TCA] is set in ***Battery Status*** by a primary charge termination (See *Taper Current*), or *TCA Set%* condition (see *TCA Set%*), or many of the fault conditions from the **1st Level Safety** and **2nd Level Safety** classes. Even with [TCA] set, if configured for Charge FET to be turned off ([CHGFET] set in *Operation Cfg B*) then ***Charging Current*** is set to 0, and [MCHG] is cleared in *Charging Status*.

Normal Setting: This register should be 0 for most if not all Li-Ion chemistries.

Taper Current

Taper Current is used in the Primary Charge Termination algorithm. ***Current*** is integrated over each of the two *Current Taper Window* periods separately, and then they are averaged separately to give two averages. Both of these averages must be below the *Taper Current* to qualify for a Primary Charge Termination. In total, a primary charge termination has the following requirements:

1. ***Voltage*** must be above (*Charging Voltage – Termination Voltage*) for the bq20z80 to start trying to qualify a termination. It must be above this voltage before bq20z80 starts trying to detect a primary charge termination.
2. An average of all ***Current*** measurements must be below *Taper Current* for two consecutive periods of *Current Taper Window* from beginning to end of each window.
3. An average of all ***Current*** measurements during each of two consecutive periods of *Current Taper Window* from beginning to end of each window must be above 0.25 mAh as integrated, and averaged over the two *Current Taper Windows*.

When these conditions are met, the primary charge termination has occurred and the following happens:

1. 1. if *TCA Set %* = –1 (disabled) then [TCA] is set in ***Battery Status*** and either of the following happens:
   a. if [CHGFET] set in *Operation Cfg B* then and ***Charging Current*** is set to 0, and the Charge FET is opened.
   b. if [CHGFET] is cleared in *Operation Cfg B* then and ***Charging Current*** is set to *Maintenance Current*.
2. If *FC_Set %* = –1 (disabled), then [FC] is set in ***Battery Status***
3. If [CSYNC] is set in *Operation Cfg B*, then ***Remaining Capacity*** is written to ***Full Charge Capacity***.

The primary charge termination mode has two clearing methods:

1. It is cleared when ***RSOC*** falls below *FC Clear %*
2. if [CHGTERM] in *Operation Cfg B* set, and ***Current*** is less than *Chg Current Threshold* for two consecutive periods of *Current Taper Window.*

Normal Settings: This register is dependent on battery cell characteristics and charger specifications, but typical values are C/10 to C/20. ***Average Current*** is not used for this qualification because its time constant is not the same as the *Current Taper Window*. The reason for making two Current Taper qualifications is to prevent false current taper qualifications. False primary terminations happens with pulse charging and with random starting and stopping of the charge current. This is particularly critical at the beginning or end of the qualification period. It is important to note that as the *Current Taper Window* value is increased, the current range in the 3rd requirement for primary charge termination is lowered. If you increase the *Current Taper Window*, then the current used to integrate to the 0.25 mAh is decreased, so this threshold becomes more sensitive. Therefore, care should be taken when modifying the *Current Taper Window*.

Termination Voltage

During Primary Charge Termination detection, one of the 3 requirements is that ***Voltage*** must be above (*Charging Voltage – Termination Voltage*) for the bq20z80 to start trying to qualify a termination. It must be above this voltage before bq20z80 starts trying to detect a primary charge termination.

Normal Setting: This value is dependent on charger characteristics. It needs to be set so that ripple voltage, noise, and charger tolerances are taken into account. A low value selected can cause early termination. If the value selected is too high, then it can cause no or late termination detection. An example value is 200 mV (see *Taper Current*).

Current Taper Window

During Primary Charge Termination detection, all three requirements as described in *Maintenance Current* must be valid for two periods of this *Current Taper Window* for the bq20z80 to detect a primary charge termination (see *Taper Current*).

Normal Setting: This register does not need to be modified for most applications. It is important to note that as the *Current Taper Window* value Is increased, the current range in the 3rd requirement for primary charge termination is lowered. If the user increases the *Current Taper Window*, then the current used to integrate to the 0.25 mAh is decreased, so this threshold becomes more sensitive. Therefore, care should be taken when modifying the *Current Taper Window*.

TCA Set %

This is an alternative method to setting [TCA] in ***Battery Status***. If this is set to anything but (-)1, then this is the only normal (nonfault condition) function that sets [TCA]. This means that a Primary Charge Termination is not set [TCA] with *TCA Set %* set between 0 and 100%. IF set to (-)1, then the Primary Charge Termination algorithm is the only normal mode algorithms used to set [TCA]. If set between and including 0 and 100%, then whenever charging ([DSG] not set in ***Battery Status***) and ***RSOC*** rises above this value then [TCA] is set in ***Battery Status***. Regardless of this setting or any Primary Charge Termination setting, any fault condition that has [TCA] as part of its fault process works completely independent of these functions.

Normal Setting: This is a user preference. TCA Set % may be used if it is mandatory that [TCA] be set during the Charge process. It is a good process to use if the Primary Charge Termination is not assured every charge cycle (see *Maintenance Charge*). If the [CSYNC] bit is set in *Operation Cfg B*, then a Primary Charge Termination writes ***Remaining Capacity*** up to ***Full Charge Capacity*** and writes ***RSOC*** to 100% so [TCA] is set with this method even if *TCA Set %* is set between 0 and 100%

TCA Clear %

If during discharge ([DSG] set in ***Battery Status***), RSOC falls below this value then [TCA] is cleared.

Normal Setting: Must be set below *TCA Set %* if used.

FC Set %

This is an alternative method to setting [FC] in ***Battery Status***. If this is set to anything but (-)1, then this is the only normal function that sets [FC]. IF set to (-)1, then the Primary Charge Termination algorithm is used to set [FC]. If set between and including 0 and 100%, then whenever charging ([DSG] not set in ***Battery Status***) and ***RSOC*** rises above this value, then [FC] is set in ***Battery Status***. Regardless of this setting, any fault condition that has [FC] as part of its fault process works completely independent of this function.

Normal Setting: This is user preference. *FC Set %* may be used if it is mandatory that [FC] be set during the Charge process. It is a good process to use if the Primary Charge Termination is NOT assured ever charge period (see *Taper Current*).

FC Clear %

If during discharge ([DSG] set in ***Battery Status***), ***RSOC*** falls below this value, then [FC] is cleared.

Normal Setting: Must be set below *FC Set %* if used.

Cell Balancing Config

Min Cell Deviation

The cell balancing algorithm with be active only during charging ([DSG] cleared in ***Battery Status***). The function is disabled completely if *Min Cell Deviation* is set to 0. With impedance track, the bq20z80 knows the Full Charge Capacity for each cell independently. Each cell input in the bq29312A has an internal FET that shorts the cell filtering resistors, and an internal 500-Ω resistor across the cells that need reduced charging to help balance the cells. The bq20z80 use impedance track information along with the value for *Min Cell Deviation* to know how long to turn on the shorting FET. The algorithm works based on the formula:

Min Cell Deviation = dQ × R / (V × duty cycle)

Where:

dQ = correction factor = 3600 seconds/hour

V = nominal cell voltage = 3600 mV

duty cycle = 40% = 0.4

R = Total resistance from cell top to cell bottom (2 filter resistors and internal 500-Ω resistor), so for the bq20z80 EVM, the filter resistors are 100 Ω; therefore, R = 100 × 2 + 500 = 700 Ω

So for 700 Ω in resistance Min Cell Deviation = 1750 sec/mAh

Normal Setting: The bq20z80 default value for this register is 1750 s/mAH. The only values that is needed to be changed in the formula are R (Resistance), and V (nominal cell voltage). (See SLUA340 for more information)

Charging Faults

Over Charging Voltage

When the pack voltage measured by ***Voltage*** rises to or above (*Charging Voltage* + *Over Charging Voltage*), then Over Charging Voltage fault process is triggered which initiates the *Over Charging Volt Time* timer. If ***Voltage*** falls below (*Charging Voltage* + *Over Charging Voltage*) prior to the expiration of the *Over Charging Volt Time* timer, then the Over Charging Voltage fault process halts and the *Over Charging Volt Time* timer resets. If the ***Voltage*** continues to be above (*Charging Voltage* + *Over Charging Voltage*) until the *Over Charging Volt Time* timer expires, then the bq20z80 sets the [OCHGV] in ***Charging Status*** and if [OCHGV] is set in *Charge Fault Cfg*, then the Charge FET and Pre-Charge FET are both opened regardless of their status prior to the fault. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. The bq20z80 clears the Over Voltage fault condition when ***Voltage*** falls to or below Charging .

Voltage.**Normal Setting:** This value should be high enough that ripple on the charger voltage does not cause a false Over Charging Voltage fault, but low enough to allow for a normal fault condition.

Over Charge Voltage Time

When the *Over Charging Voltage* criteria are met then Over Charging Voltage fault process is triggered which initiates the *Over Charging Volt Time* timer. If the Over Charging Voltage criteria continue to be met until the *Over Charging Volt Time* timer expires, then the bq20z80 sets [OCHGV] in ***Charging Status***, and if [XCHGV] is set in *Charge Fault Cfg*, then the Charge FET and Pre-Charge FET are both opened regardless of their status prior to the fault. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. If ***Voltage*** falls below *Over Charging Voltage* criteria any time prior to the expiration of the *Over Charging Volt Time* timer, then the Over Charging Voltage fault process halts and the *Over Charging Volt Time* timer resets. The bq20z80 clears the Over Voltage fault condition when ***Voltage*** falls to or below *Charging Voltage*. (See *Over Charging Voltage*)

Normal Setting: The default for this register is 2 seconds. This should be sufficient for most applications. This function is not disabled if set to 0. Instead it triggers immediately.

Over Charging Current

When the current as measured by ***Current*** rises up to or above (***Charging Current*** + *Over Charging Current*) then Over Charging Current fault process is triggered which initiates the *Over Charging Current Time* timer. If ***Current*** falls below (***Charging Current*** + *Over Charging Current*) prior to the expiration of the *Over Charging Current Time* timer, then the Over Charging Current fault process halts and the *Over Charging Current Time* timer resets. If the ***Current*** continues to be above (***Charging Current*** + *Over Charging Current*) until the *Over Charging Current Time* timer expires, then the bq20z80 sets [OCHGI] in ***Charging Status*** and if [XCHGI] is set in *Charge Fault Cfg*, then the Charge FET and Pre-Charge FET are both opened regardless of their status prior to the fault. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes Charging Current and Charging Voltage to be set to 0. The bq20z80 clears the Over Current fault condition when ***Average Current*** falls to or below *Over Charging Recovery Current*.

Normal Setting: This setting should be set high enough to prevent false triggering, but low enough to prevent battery cell damage. 500 mA is the default setting which is sufficient for most applications.

Over Charging Current Time

When the *Over Charging Current* criteria are met, then Over Charging Current fault process is triggered which initiates the *Over Charging Current Time* timer. If the *Over Charging Current* criteria continue to be met until the *Over Charging Current Time* timer expires, then the bq20z80 set the [OCHGI] in ***Charging Status*** and if [XCHGV] is set in *Charge Fault Cfg*, then the Charge FET and Pre-Charge FET are both opened regardless of their status prior to the fault. This fault condition causes [TCA] in ***Battery Status*** to be set. It also causes ***Charging Current*** and ***Charging Voltage*** to be set to 0. If ***Current*** falls below *Over Charging Current* criteria any time prior to the expiration of the *Over Charging Current Time* timer, then the Over Charging Current fault process halts and the *Over Charging Current Time* timer resets. The bq20z80 clears the Over Current fault condition when ***Average Current*** falls to or below *Over Charging Recovery Current*.

Normal Setting: The default for this register is 2 seconds. This is sufficient for most applications. This function is not disabled if set to 0. Instead it triggers immediately.

Over Charging Recov Curr

When the *Over Charging Current* criteria are met to the point of forcing an Over Charging Condition Fault, then the bq20z80 clears the Over Current fault condition when ***Average Current*** falls to or below *Over Charging Recovery Current*.

Normal Setting: The default for this register is 100 mA. This is sufficient for most applications.

Depleted Voltage

When the voltage measured by ***Voltage*** falls to *Depleted Voltage* threshold and stays at or below this level for more than *Depleted Voltage Time* seconds, then the bq20z80 sets the [XCHGLV] in ***Charging Status*** and the [TDA] in ***Battery Status***. If [CS_XCHGLV] bit is set in *Charge Fault Cfg*, then the discharge FET is turned off. A charger must be detected as present for a *Depleted Voltage* fault to occur. See *Charger Present* for a description on how to detect a charger.

Normal Setting: This function is not recommended if there is any external voltage source that could interfere with *Charger Present*. Set *Depleted Voltage Timer* to 0 to disable this function. This register is variable depending on the lowest possible system voltage. Set this value just above what the system requires for the lowest possible voltage.

Depleted Voltage Time

See *Depleted Voltage*. The ***Voltage*** must be equal to or below the Depleted Voltage for at least this time (*Depleted Voltage Time*) for the bq20z80 to register a [XCHGLV] fault in ***Charging Status***. If set to 0, then *Depleted Voltage* function is completely disabled.

Normal Setting: The default value for this register is 2 seconds. Ensure that this register is set to prevent false readings or spiked load currents from triggering a premature fault. With high current loads, be sure that this register is set short enough to prevent the system from detecting a low voltage since voltage is normally dropping very rapidly at this level.

Depleted Recovery

When the voltage as measured by ***Voltage***, rises to or above this value while charging then the [OCHGLV] flag is cleared in *Charging Status*. If the discharge FET was turned off, it returns to the on state.

Normal Setting: This register should be set at least several hundred millivolts higher than the *Depleted Voltage* to ensure hysteresis through this transition.

Over Charge Capacity

Over Charge Capacity is detected in a two-step process. First the battery must be charged to the point where Remaining Capacity reaches ***FCC*** (***Full Charge Capacity***). Then any charge applied after this point is still measured but not displayed by the bq20z80. When this charge as measured by the bq20z80 reaches a threshold as defined by ***FCC*** + *Over Charge Capacity*, then the bq20z80 goes into a charging fault condition. The [OC] in ***Charging Status*** is set. ***Charging Voltage*** and ***Charging Current*** are both set to 0. If [OC] set in *Charge Fault Cfg*, then the Charge FET is turned off.

Normal Setting: This register is application dependent but a good example is 100 to 300 mAh for each cell in parallel. To small of a value could force false detections, and to large a value could damage the cells if normal charge termination methods fail.

Over Charge Recovery

There are three recovery methods for the bq20z80.

1. The first involves *Over Charge Recover* and only happens if [NR] in *Operation Cfg B* is set. With this setting, the bq20z80 recovers from an overcharged condition with a continuous discharge of “Over Charge Recovery” mAHs.
2. With [NR] cleared in *Operation Cfg B*, the bq20z80 recovers from the overcharge fault with a pack removal and reinsertion ($\overline{\text{PRES}}$ transition).
3. The third recovery happens when ***RSOC*** falls below the *FC Clear %*. This recovery also is the only one that returns ***Charging Voltage*** and ***Charging Current*** to normal.

Normal Setting: This value is normally small. Typically around 2 mAh. Its only purpose is to ensure small discharge spikes or false discharge detections do not clear the condition prematurely.

FC-MTO

If charging current is greater than *Chg Current Threshold* and [FCHG] is set in ***Charging Status*** for *FC-MTO* time in seconds, then the bq20z80 sets [FC-MTO] (fast time mode timeout) in ***Charging Status***, ***Charging Voltage*** and ***Charging Current*** are set to 0, [TCA] is set in ***Battery Status***, and if [FCMTO] is set in *Charge Fault Cfg* then the Charge FET is turned off. If charging is interrupted ([DSG] in ***Battery Status*** sets) and an *Over Charging Curr Recov* amount of discharge is detected anytime during the charging process prior to *FC-MTO* timer expiring, then the *FC-MTO* timer is reset and starts counting from 0. The bq20z80 recovers from an *FC-MTO* fault with the following conditions:

1. The fault condition is cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*.
2. If Current falls below *Dsg Current Threshold*

If *FC-MTO* is 0, then this function is disabled.

Normal Settings: The purpose of this register is another form of charge protection. If this timer has timed out, then something has gone wrong and the battery is taking to long to charge. The default setting for this register is 10800 seconds. This may be short for some applications. Be sure and give plenty of time for all possible scenarios. Smaller charge currents may require longer settings. It is also important to note that as a battery ages, the charge time increases due to increased impedance. Setting this value short limits the capacity of aged cells.

PC-MTO

If charging current is greater than *Chg Current Threshold*, and [PCHG] is set in ***Charging Status*** for *PC-MTO* time in seconds, then the bq20z80 sets [PC-MTO] (precharge time mode timeout) in ***Charging Status***, ***Charging Voltage*** and ***Charging Current*** are set to 0, [TCA] is set in ***Charging Status***, and if [PCMTO] is set in *Charge Fault Cfg* then the Charge FET/Pre-Charge FET is turned off. If charging is interrupted ([DSG] in ***Charging Status*** sets) and an *Over Charging Curr Recov* amount of discharge is detected anytime during the charging process prior to *FC-MTO* timer expiring, then the *FC-MTO* timer is reset and starts counting from 0. The bq20z80 recovers from a *PC-MTO* fault with the following conditions:

1. The fault condition is cleared with pack removal and reinsertion ($\overline{\text{PRES}}$ transition) if [NR] is cleared in *Operation Cfg B*.
2. If ***Current*** falls below *Dsg Current Threshold*

If *PC-MTO* is 0 then this function is disabled.

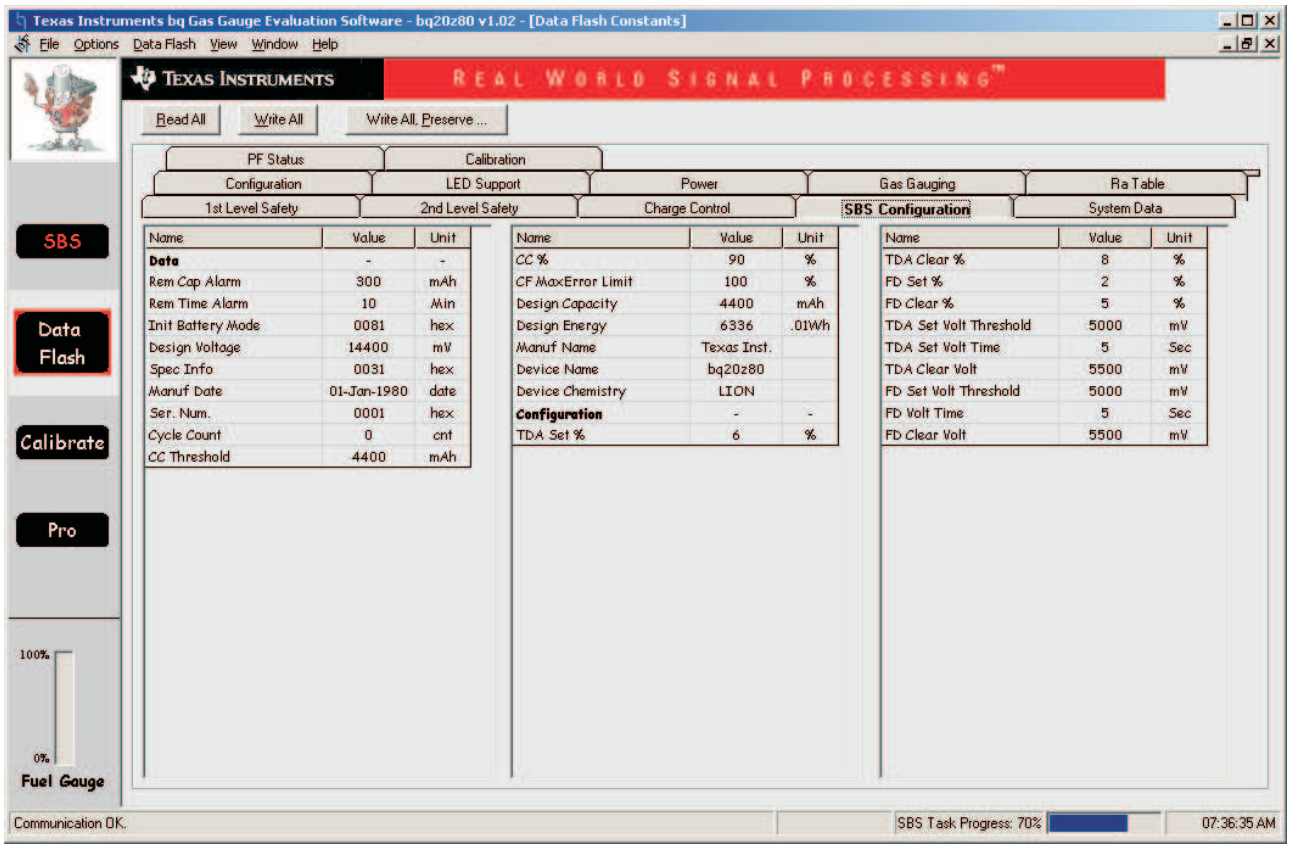
Normal Settings: The purpose of this register is another form of charge protection. If this timer has timed out, then something has gone wrong and the battery is taking to long to charge. The default setting for this register is 3600 seconds. This is good for most applications. Smaller charge currents may require longer settings.

Charge Fault Configuration

—	—	PCMTO	FCMTO	OCHGV	OCHGI	OC	CS_XCHGLV

- PCMTO: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *PC-MTO* fault condition occurs.
  Normal Setting: Default is 0 (disabled)
- FCMTO: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *FC-MTO* fault condition occurs.
  Normal Setting: Default is 0 (disabled)
- OCHGV: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *Over Charging Voltage* fault condition occurs.
  Normal Setting: Default is 0 (disabled)
- OCHGI: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *Over Charging Current* fault condition occurs.
  Normal Setting: Default is 0 (disabled)
- OC: If set, then the Charge FET or Pre-Charge FET (depending on which is active at the time) is turned off when an *Over Charge* fault condition occurs.
  Normal Setting: Default is 0 (disabled)
- CS_XCHGLV: If set, then the discharge FET is turned off when a Depleted Voltage fault condition occurs.
  Normal Setting: Default is 0 (disabled)

2.5 SBS Configuration



Data

Rem Cap Alarm

When the ***Remaining Capacity*** falls below this value, [RTA] is set in ***Battery Status***.

Normal Setting: About 10% of the *Full Charge Capacity*. This value is programmed into ***RemainingCapacityAlarm*** on device initialization

Rem Time Alarm

When the average time to empty falls below this value, then the [RTA] flag is set in ***Battery Status***.

Normal Setting: Approximately 10 minutes. This value is programmed into ***RemainingTimeAlarm*** on device initialization.

Init Battery Mode

This is the default value loaded into ***Battery Mode*** on all resets, and when the bq20z80 wakes from sleep. The primary purpose of having an initial value for this register is to enable milliwatt mode whenever the bq20z80 resets or wakes up from sleep.

Normal Setting: In most applications, this register should be 0x0081. If the application requires the bq20z80 to wake in mW mode, then this value can be set to 0x8081. Care should be taken with this setting; however, because the ***Battery Mode*** register is writable even when the bq20z80 is sealed. The mW mode bit can be accidentally written to a 0.

Design Voltage

This is the theoretical nominal voltage of the battery pack. This value is used in ***ATRATE*** calculations and milliWatt mode (***Battery Mode*** MSByte bit 7).

Normal Setting: This varies by cell manufacturer, but Li-Ion is normally about 3.6-V per cell. See the cell manufacturer data sheet for the exact numbers. This value is programmed into ***DesignVoltage*** on device initialization.

Spec Info

This performs two purposes. The high byte has the current and voltage multipliers. The bq20z80 does not require any multiplier, so use 0x00. The low byte is the SBS specification revision. See the SBS Implementers Forum web page for more information (http://www.sbs-forum.org/specs/index.html).

Normal Setting: 0x0031 for SBS specification v1.1 with PEC error checking, or 0x0021 for SBS specification V1.1 without PEC error checking.

Mfg Date

This is the date of manufacture. It is stored in the Data Flash in packed format. All bqEV Software and bqMTester both accept input of this date in standard date format so the packed format does not need to be used input. It is then translated by the software to packed format. This data does not affect the operation, nor is it used by the part in any way.

Ser Num

This is a 16 bit serial number that does not affect the operation nor is it used by the part in any way. It is normally used for battery identification.

Cycle Count(CC)

There are two methods to increment *Cycle Count*:

1. If [CCT] is set in *Operation Cfg B*, then this CC% is used to increment *Cycle Count*. When the bq20z80 accumulates enough discharge capacity equal to (*CC%* × ***Full Charge Capacity***), then it increments *Cycle Count* by 1. If at any time (*CC%* × ***Full Charge Capacity***) is less than *Cycle Count Threshold*, then the *Cycle Count Threshold* is used to increment *Cycle Count*.
2. If [CCT] is cleared in Operation Cfg B, then *Cycle Count Threshold* is always be used to increment Cycle Count. When the bq20z80 accumulates enough discharge capacity equal to the *Cycle Count Threshold*, then it increments Cycle Count by 1.

This discharge capacity used by either of these methods does not have to be consecutive. The internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the *Cycle Count Threshold* or *CC %* depending on [CCT]. Then *Cycle Count* is incremented. Every increment of *Cycle Count* between QMAX updates increments ***MaxErr*** by 0.05%. It takes 20 increments of *Cycle Count* to increment ***MaxErr*** by 1%, so that it is visible in the SBS register.

Normal Setting: This should be set to 0.

Cycle Count Threshold

If [CCT] is cleared in *Operation Cfg B*, then this value is always used to increment *Cycle Count*. When the bq20z80 accumulates enough discharge capacity equal to the *Cycle Count Threshold*, then it increments *Cycle Count* by 1. This discharge capacity does not have to be consecutive. The internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the *Cycle Count Threshold*, and increments *Cycle Count*. If [CCT]is set, then see *CC%*

Normal Setting: This is normally set to about 80% of the *Design Capacity*.

CC%

If [CCT] is set in *Operation Cfg B*, then this value is used to increment *Cycle Count*. When the bq20z80 accumulates enough discharge capacity equal to (*CC%* × *FCC*), then it increments *Cycle Count* by 1. If at any time (*CC%* × ***Full Charge Capacity***) is less than *Cycle Count Threshold*, then the *Cycle Count Threshold* is used to increment *Cycle Count*. This discharge capacity does not have to be consecutive. The internal register that accumulates the discharge is not cleared at any time except when the internal accumulating register equals the (*CC%* × *FCC*), and increments *Cycle Count*. If [CCT] is clear, then see *Cycle Count Threshold*.

Normal Setting: This is normally set to 80–90%. This can be set closer to *FCC* than the *Cycle Count Threshold* method because it tracks with *FCC* as it decreases with age. This keeps cycle count tracking closely with each discharge cycle as the battery ages. Ensure that *Cycle Count Threshold* has a meaningful value even if *CC%* is used because the *Cycle Count Threshold* is used if (*CC%*×***Full Charge Capacity***) is less than *Cycle Count Threshold*.

CF Max Error Limit

The bq20z80 forces [CF] to be set in ***Battery Mode*** if ***MaxErr*** goes above the value stored in this register. This value is used to give an alternate method for setting the [CF] flag in ***Battery Mode***, other than the impedance track algorithm. The [CF] flag is a condition request flag indicating the battery would like a full charge/discharge cycle, and rarely is set by impedance track because accurate capacity measurements are always updated.

Normal Setting: This register is normally set to 100 and is in units of %.

Design Capacity

Design Capacity is the data flash location that is reported in the ***Design Capacity*** register when [CapM] is clear in ***Battery Mode***. If [CapM] is set in ***Battery Mode***, then *Design Energy* is reported in ***Design Capacity***. This value is used also for the ***ASOC*** calculation by the bq20z80 if [CapM] is cleared in ***Battery Mode***.

Normal Setting: This value should be set based on the application battery specification. See the battery manufacturer data sheet.

Design Energy

Design Energy is the data flash location that is reported in the ***Design Capacity*** register if [CapM] is set in ***Battery Mode***. If [CapM] is clear in ***Battery Mode***, then *Design Capacity* is reported in *Design Capacity*. This value is used also for the ASOC calculation by the bq20z80 if [CapM] is set in ***Battery Mode***.

Normal Setting: This value is be set based on the application battery specification. See the battery manufacturer data sheet. At higher rates of discharge, energy is less, so referring to discharge data similar to the typical rate of the user's application is important to obtain a meaningful value.

Manuf Name

String data that can be a maximum of 11 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x20.

Device Name

String data that can be a maximum of 7 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x21.

Device Chemistry

String data that can be a maximum of 4 characters. This field does not affect the operation, nor is it used by the part in any way. It is returned by an SMBus block read to command 0x22 .

Configuration

These are alternative methods for setting and clearing [TDA] and [FD] in ***Battery Status***. They are in addition to traditional methods or fault conditions explained in other areas of this document.

TDA Set %

If set to a value between 0 and 100 then when ***RSOC*** falls to or below this value, then [TDA] in ***Battery Status*** is set. If set to (-)1, then this function is disabled. *TDA Set Volt Threshold* is not affected by this register. They are completely independent. Any fault condition that specifies setting [TDA] is completely unaffected by this register.

Normal Setting: This is user preference. This is the threshold that the bq20z80 requests that discharge be halted because the battery is nearing depletion. If used, it is normally set around 6%. Be sure that if *TDA Clear %* is used, then this should be used as well. They only work together.

TDA Clear %

If set to a value between 0 and 100 then when ***RSOC*** rises to or above this value after being set by *TDA Set %*, then [TDA] in ***Battery Status*** is cleared. This register can only be used to clear [TDA] if it was set by TDA Set %. If set to (-)1 then this function is disabled. *TDA Clear Volt Threshold* is not affected by this register. They are completely independent.

Normal Setting: This is user preference. If used it is normally set around 8%. Be sure that if *TDA Set %* is used then this should be used as well. They only work together.

FD Set %

If set to a value between 0 and 100 then when ***RSOC*** falls to or below this value then [FD] in ***Battery Status*** is set. If set to (-)1 then this function is disabled. *FD Set Volt Threshold* is not affected by this register. They are completely independent. Any fault condition that specifies setting [FD] is completely unaffected by this register.

Normal Setting: This is user preference. This is a stronger request than TDA. The battery is presumed dead at this point. If used it is normally set around 2%. Be sure that if FD *Clear %* is used then this should be used as well.

FD Clear %

If set to a value between 0 and 100 then when ***RSOC*** rises to or above this value after being set by *FD Set %*, then [FD] in ***Battery Status*** is cleared. If set to (-)1 then this function is disabled. *FD Clear Volt Threshold* is not affected by this register. They are completely independent.

Normal Setting: This is user preference. If used it is normally set around 5%. If FD Set % is used, then this should be used as well. They only work together.

TDA Set Volt Threshold

When battery voltage as measured by ***Voltage*** falls to or below the *TDA Set Volt Threshold* value for *TDA Set Volt Time* seconds, then [TDA] in ***Battery Status*** is set. This works completely independent of *TDA Set %*. Any fault condition that specifies setting [TDA] is completely unaffected by this register.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 6% ***RSOC***.

TDA Set Volt Time

See *TDA Set Volt*. This is the time that the battery voltage must be equal to or below *TDA Set Volt Threshold* before [TDA] is set in ***Battery Status***.

Normal Setting: This is normally set to 5 seconds but depends on the application.

TDA Clear Volt Threshold

When battery voltage (as measured by ***Voltage***) rises to or above this value, then [TDA] in ***Battery Status*** is cleared. [TDA] is only cleared with this threshold if it was set by *TDA Set Volt* criteria, and it is not cleared if it was set by any other methods.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 8% ***RSOC***.

FD Set Volt Threshold

When battery voltage as measured by ***Voltage*** falls to or below the *FD Set Volt Threshold* value for *FD Set Volt Time* seconds, then [FD] in ***Battery Status*** is set. This register works completely independent of *FD Set %*. Any fault condition that specifies setting [FD] is completely unaffected by this register.

Normal Setting: This is user preference but should be a voltage that the battery is at under normal loads at around 2% ***RSOC***.

FD Set Volt Time

See *FD Set Volt*. This is the time that the battery voltage must be equal to or below *FD Set Volt Threshold* before [FD] is set in ***Battery Status***.

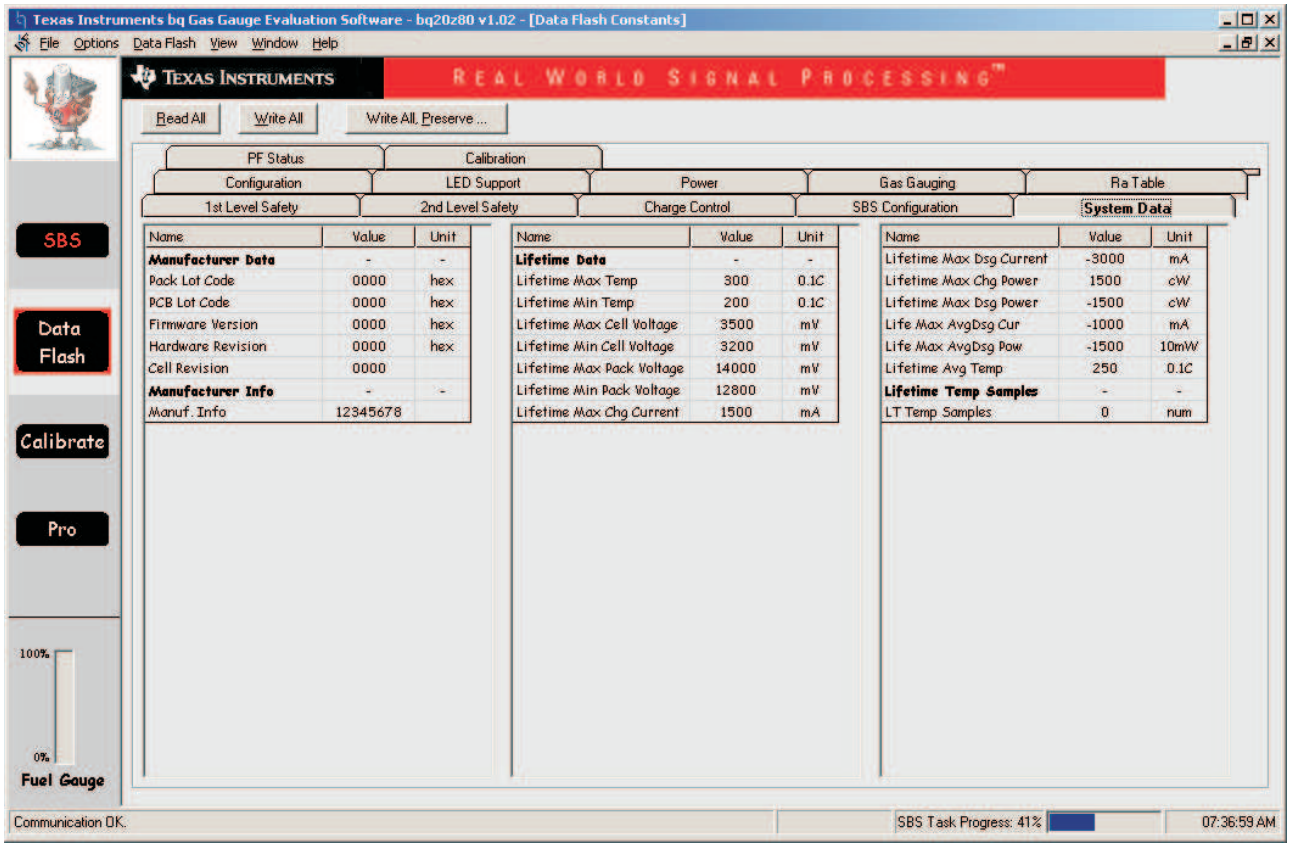
Normal Setting: This is normally set to 5 seconds but depends on the application.

FD Clear Volt Threshold

When battery voltage as measured by ***Voltage*** rises to or above this value, then [FD] in ***Battery Status*** is cleared. [FD] is cleared from this threshold only if it was set by *FD Set Volt* criteria.

Normal Setting: This is user preference, but it must be a voltage that the battery is at under normal loads at around 5% ***RSOC***.

2.6 System Data



Manufacturer Data

Pack Lot Code

This is a 16 bit value that does not affect operation nor is it used by the part in any way.

Normal Setting: The most common use of this register is as an extension to the *Serial Number* as a form of pack identification. It is only readable via ***Manufacturer Data*** (0x23) string read.

PCB Lot Code

This is a 16 bit value that does not affect operation nor is it used by the part in any way.

Normal Setting: The most common use of this register is as an extension to the *Serial Number* as a form of pack identification. It is only readable via ***Manufacturer Data*** (0x23) string read.

Firmware Version

This is a 16 bit value that does not affect operation nor is it used by the part in any way. It is intended as a firmware revision however it is not protected so it is not reliable. Use ***Manufacturing Access Commands*** to get a reliable firmware version of the bq20z80.

Normal Setting: This can be used for any user data. It is only readable via ***Manufacturer Data*** (0x23) string read.

Hardware Revision

This is a 16 bit value that does not affect operation nor is it used by the part in any way. It is intended as a IC hardware revision; however, it is not protected so it is not reliable. Use ***Manufacturing Access Commands*** to get a reliable firmware version of the bq20z80.

Normal Setting: This can be used for any user data. It is only readable via ***Manufacturer Data*** (0x23) string read.

Cell Revision

This is a 16 bit value that does not affect operation nor is it used by the part in any way.

Normal Setting: This can be used for any user data. It is only readable via ***Manufacturer Data*** (0x23) string read.

Manufacturer Info

Manuf. Info

This is string data that can be any user data. It can be a maximum of 8 characters.

Normal Setting: Can be used for any user data.

Lifetime Data

Lifetime Max Temp

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum temperature as measured by ***Temperature*** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Temp* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Temp* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Temp* by at least 1°C
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Min Temp

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the minimum temperature as measured by ***Temperature*** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Min Temp* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Min Temp* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Min Temp* by at least 1°C
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Cell Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum cell voltage as measured by ***Cell Voltage (Max)*** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Cell Voltage* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Cell Voltage* for 60 seconds

2. If the internal RAM location is greater than *Lifetime Max Cell Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Min Cell Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the minimum cell voltage as measured by ***Cell Voltage (Min)*** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Min Cell Voltage* in Data Flash with one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Min Cell Voltage* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Min Cell Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Pack Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum pack voltage as measured by ***Voltage*** is updated continuously in a reserved RAM location. To prevent flash wear out, this RAM only updates with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Pack Voltage* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Pack Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Min Pack Voltage

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the minimum cell voltage as measured by ***Voltage*** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Min Pack Voltage* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Min Pack Voltage* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Min Pack Voltage* by at least 25 mV.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Chg Current

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum current in the charge direction as measured by ***Average Current*** is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Chg Current* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Chg Current* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Chg Current* by at least 100 mA.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Dsg Current

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum current in the discharge direction as measured by ***Average Current*** is updated continuously in a reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Dsg Current* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is less than (–)*Lifetime Max Chg Current* for 60 seconds
2. If the internal RAM location is less than (–) *Lifetime Max Chg Current* by at least 100 mA.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Chg Pwr

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum power in the charge direction as measured by a reserved continually updated average power register (uses ***Voltage***×***Current*** in an internal averaging algorithm) is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Chg Pwr* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is greater than *Lifetime Max Chg Power* for 60 seconds
2. If the internal RAM location is greater than *Lifetime Max Chg Power* by at least 100 in units of 100 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Max Dsg Pwr

When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), and the maximum power in the discharge direction as measured by a reserved continually updated average power register (uses ***Voltage***×***Current*** in an internal averaging algorithm) is updated continuously in a lifetime reserved RAM location. To prevent flash wear out, this RAM only updates *Lifetime Max Dsg Power* in Data Flash with any one of the following 3 conditions:

1. Whenever the internal RAM location is less than (–)*Lifetime Max Chg Current* for 60 seconds.
2. If the internal RAM location is less than (–) *Lifetime Max Chg Current* by at least 100 in units of 100 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Life Max Avg Dsg Pwr

Power is averaged over every discharge cycle. Every discharge cycle an internal unaccessible RAM Register (LastAveragePower) is updated with this average power. The maximum power in the discharge direction as measured by this last average discharge power register (uses ***Voltage***×***Current*** in an internal averaging algorithm) is updated continuously in a lifetime data reserved RAM location. When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), the *Life Max Avg Dsg Pwr* data flash register is updated from this RAM location but only with any one of the following 3 conditions:

1. Whenever the internal RAM location is **less** than (–) *Lifetime Max Avg Dsg Power* for 60 seconds.
2. If the internal RAM location is **less** than (–) *Lifetime Max Avg Dsg Power* by at least 100 in units of 100 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Life Min Avg Dsg Pwr

Power is averaged over every discharge cycle. Every discharge cycle an internal unaccessible RAM Register (LastAveragePower) is updated with this average power. The minimum power in the discharge direction as measured by this last average discharge power register (uses ***Voltage***×***Current*** in an internal averaging algorithm) is updated continuously in a lifetime data reserved RAM location. When the Impedance Track Algorithm is enabled ([QEN] set in Operation Status), the *Life Min Avg Dsg Pwr* data flash register is updated from this RAM location but only with any one of the following 3 conditions:

1. Whenever the internal RAM location is **greater** than (–) *Lifetime Min Avg Dsg Power* for 60 seconds.
2. If the internal RAM location is **greater** than (–) *Lifetime Min Avg Dsg Power* by at least 100 in units of 100 mW.
3. Any other Lifetime Data was updated in data flash with the same criteria as step 1 and 2 for their respective RAM and Flash locations.

Lifetime Avg Temp

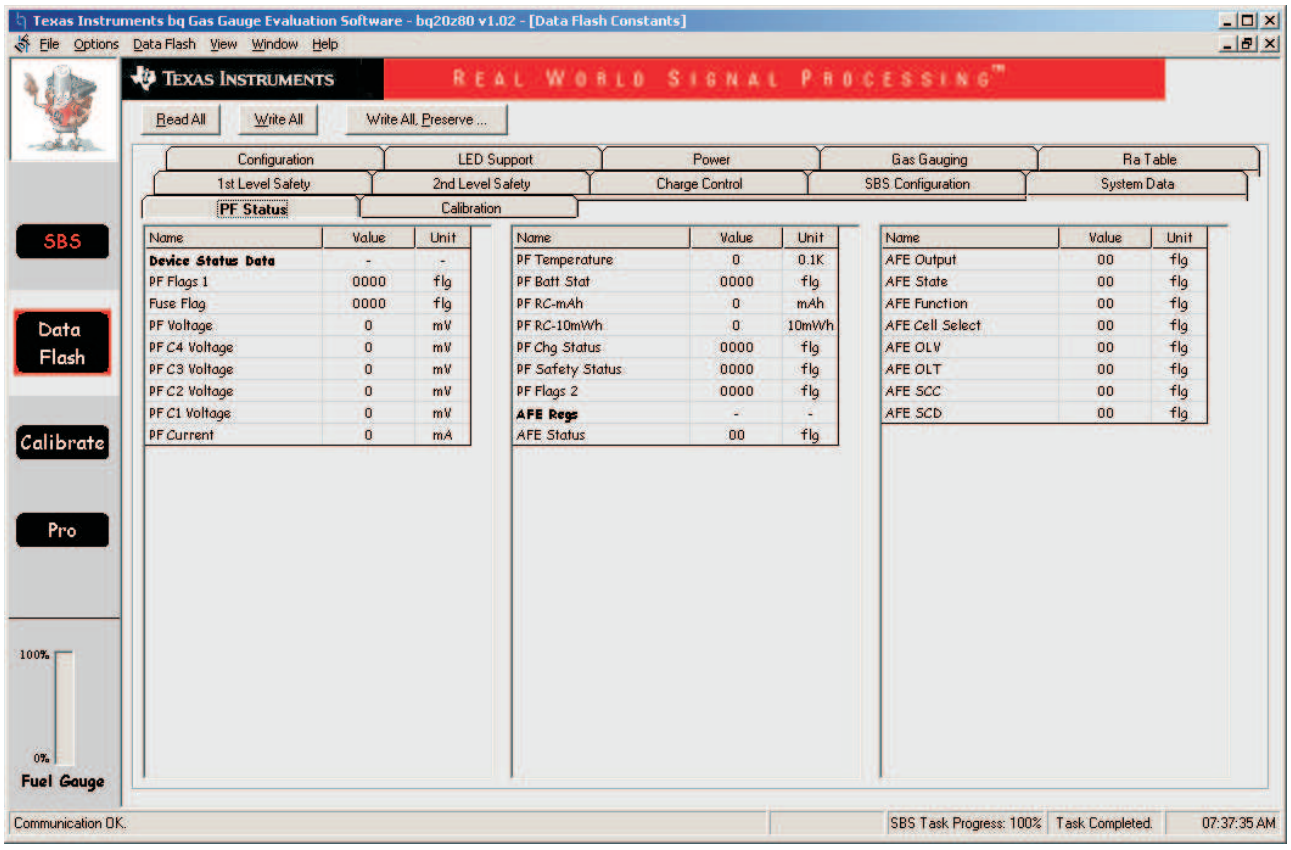
Temperature is averaged over the entire life of the battery. The temperature is sampled from the ***Temperature*** register every 1/16th of an hour. Then summed given the last Temperature Sum (***Temperature*** + Previous ***Temperature*** Sum)as updated the previous 1/16th of an hour sample and then divided by *LT Temp Samples*. This is then updated continuously in a lifetime data reserved RAM location. To prevent flash wear out, this RAM only updates to data flash when any other Lifetime Data locations update to data flash after meeting their update criteria. Impedance Track must be enabled ([QEN] set in Operation Status) for this data flash update to occur.

Lifetime Temp Samples

LT Temp Samples

LT Temp Samples are used to compute the *Lifetime Avg Temp*. Temperature is averaged over the entire life of the battery. The temperature is sampled from the ***Temperature*** register every 1/16th of an hour, then summed given the last Temperature Sum (***Temperature*** + Previous ***Temperature*** Sum)as updated the previous 1/16th of an hour sample and then divided by *LT Temp Samples*. *LT Temp Samples* is then incremented by 1. *LT Temp Samples* is updated continuously in a lifetime data reserved RAM location. To prevent flash wear out, this RAM location only updates when any other Lifetime Data location updates to data flash after meeting their update criteria. Impedance Track™ must be enabled ([QEN] set in Operation Status) for this data flash update to occur.

2.7 PF Status



There is no configuration or settings required for the PF Status Class. The entire PF Status class should all be zeros for every register. This class is intended only for reporting failure information to the factory and Texas Instruments. In fact, it only reports any information with catastrophic failures or during development time as a tool to help with configuration or layout issues.

Device Status Data

PF Flags 1

This location indicates all the causes of permanent failures that have occurred from the time the bq20z80 was last programmed with new firmware or the last time this register was cleared. It is important to understand that more than one fault can be recorded here if multiple faults have occurred. *PF Flags 1* bit locations and definitions correspond to ***PF Status***. If the corresponding bit in PF Flags 1 is enabled in the *Permanent Fail Cfg* register then the bq20z80 attempts to blow the fuse in addition to record the permanent failure in the *PF Flags 1 register*. This register is cleared (set to 0x0000) if the manufacturers access clear PF command is sent to the bq20z80 (See the bq20z80 data sheet). This is the only register in the data flash which ignores the disabled data flash writing setting when a permanent failure occurs. (See *Permanent Fail Cfg*)

FBF	–	–	SOPT	SOCD	SOCC	AFE_P	AFE_C
DFF	DFETF	CFETF	CIM	SOTD	SOTC	SOV	PFIN

- FBF: Set if *Fuse Fail Limit* fault has occurred and the function is enabled. If the *Fuse Flag* has been set to 0x3672 (SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80) and the current as measured by ***Current*** still exists which is greater than *Fuse Fail Limit* in milliamps, or less than a (–) *Fuse Fail Limit* for *Fuse Fail Time*, then the this flag is set. See *Fuse Fail Limit*.
- SOPT: Set if a Safety Open Thermistor Fault has occurred and the function is enabled. If *Open Thermistor Time* is set to 0, then this function is disabled. If [XSOPT] is set in *Permanent Fail Cfg* then 0x3672 is written to the *Fuse* Flag. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80 (See *SOC Dsg*).
- SOCD: Set if a Safety Over Current Discharge Fault has occurred and the function is enabled. If *SOC Dsg Time* is set to 0, then this function is disabled. If [XSOCD] is set in *Permanent Fail Cfg* then 0x3672 is written to the *Fuse* Flag. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80 (See *SOC Dsg*).
- SOCC: Set if a Safety Over Current Charge Fault has occurred and the function is enabled. If *SOC Chg Time* is set to 0, then this function is disabled. If [XSOCC] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80 (See *SOC Chg*).
- AFE_P: Set if a Periodic AFE Check Fault has occurred and the function is enabled. If *AFE Check Time* is set to 0, then this function is disabled. If [XAFE_P] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80 (See *AFE Check Time*).
- AFE_C: Set if an AFE Communication Fault has occurred. If *AFE Fail Limit* is set to 0, then this function is disabled. If [XAFE_C] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80 (See *AFE Fail Limit*).
- DFF: The bq20z80 verifies all data flash writes and will set [DFF] if a Data Flash Verify Fault has occurred Only the setting of [DFF] can be disabled. If [XDFF] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80.
- DFETF: Set if a Discharge FET Fault has occurred and the function is enabled. If *FET Fail Time* is set to 0, then that function is disabled. If [XDFETF] is set in *Permanent Fail Cfg* then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80 (See *FET Fail Time*).
- CFETF: Set if a Charge FET Fault has occurred and the function is enabled. If *FET Fail Time* is set to 0, then that function is disabled. If [XCFETF] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80 (See *FET Fail Time*).
- CIM: Set if a Cell Imbalance Fault has occurred and the function is enabled. If *Battery Rest Time* is set to 0, then that function is disabled. If [XCIM] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80(See *Battery Rest Time*).
- SOTD: Set if a Safety Over Temperature Discharge Fault has occurred and the function is enabled. If *SOT Dsg Time* is set to 0, then this function is disabled. if [XSOTD] is set in *Permanent Fail Cfg,* then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80 (See *SOT Dsg*).

- SOTC: Set if a Safety Over Temperature Charge Fault has occurred and the function is enabled. If *SOT Chg Time* is set to 0, then this function is disabled. If [XSOTC] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag.* The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80 (See *SOT Chg*).
- SOV: Set if a Safety Over Voltage Threshold Fault has occurred and the function is enabled. If *SOV Time* is set to 0, then this function is disabled. if [XSOV] is set in *Permanent Fail Cfg*, then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80 (See *SOV Threshold*).
- PFIN: The bq20z80 monitors the PFIN line. When the PFIN line goes low for *PFIN Detect Time*, then the bq20z80 attempts to report a PFIN Fault if the function is enabled. If *PFIN Detect Time* is set to 0 then this function is disabled. if [XPFIN] is set in *Permanent Fail Cfg* then 0x3672 is written to the *Fuse Flag*. The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80 (See *PFIN Detect Time*)

Fuse Flag

This is set to 0x3672 when the bq20z80 sets any permanent failure flags in ***PF Status***. Otherwise this register is 0x0000. This register is cleared (set to 0x0000) if the manufacturers access clear PF command is sent to the bq20z80. See the bq20z80 Technical Reference Manual (SLUU241) for more information on clearing permanent failures.

PF Voltage

The ***Voltage*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF C1 Voltage

The ***Cell Voltage 1*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF C2 Voltage

The ***Cell Voltage 2*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF C3 Voltage

The ***Cell Voltage 3*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF C4 Voltage

The ***Cell Voltage 4*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Current

The ***Current*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Temperature

The ***Temperature*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Batt Stat

The ***Battery Status*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF RC (mAh)

The ***Remaining Capacity*** register in mAh is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF RC (10mWh)

The ***Remaining Capacity*** register in mWh is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Charging Status

The ***Charging Status*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Safety Status

The ***Safety Status*** register is captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

PF Flags 2

This register reports the first permanent failure that occurred from the time the bq20z80 was last programmed with new firmware. The difference between this register and PF Flags 1 is that this register only records one failure and it is the first one in a possible series of failures. This method gives a better chance to learn what could have caused a whole series of failures by knowing what the first failure was.

AFE Regs

All AFE registers are captured at the time that the most recent permanent failure occurred. This subclass should always be 0 unless a permanent failure has occurred.

AFE Status

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE Output

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE State

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE Function

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE Cell Select

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE OLV

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE OLT

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

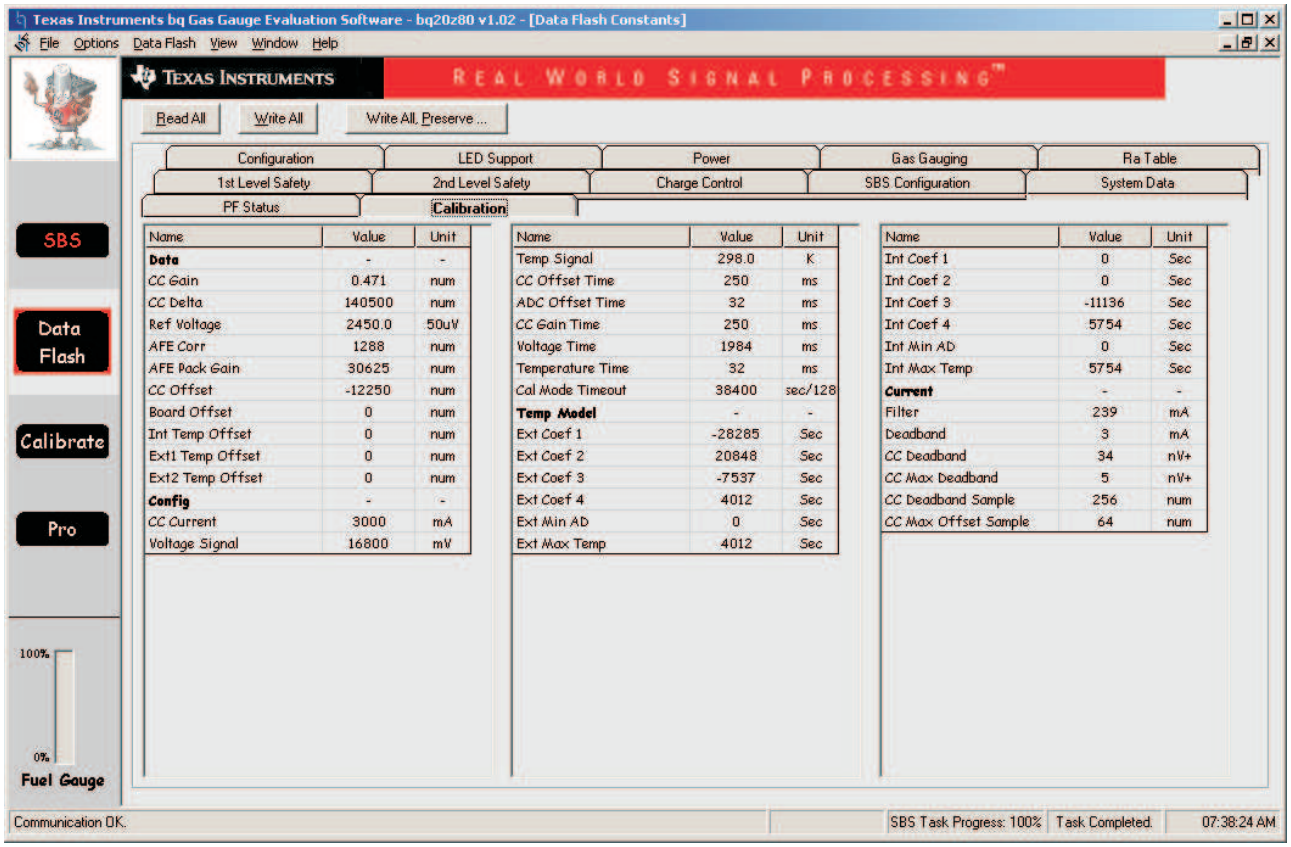
AFE SCC

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

AFE SCD

The internal RAM copy in the AFE Status register in the bq20z80 captured at the time that the most recent permanent failure occurred and is stored in this location. Anytime that a new permanent failure occurs this value is not rewritten. It is only written with the first PF failure.

2.8 Calibration



Data

Most of these values should never need to be modified by the user. They should only be modified by the Calibration commands in Calibration mode as explained in the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note SLUA355A.

CC Gain

This is the gain factor for calibrating out Sense Resistor, Trace, and internal Coulomb Counter (integrating ADC Delta Sigma) errors. It is used in the algorithm that reports ***Current***. The difference between *CC Gain* and *CC Delta* is that the algorithm that reports Current cancels out the time base since ***Current*** does not have a time component (it reports in mA) and CC Delta requires a time base for reporting ***Remaining Capacity*** (it reports in mAh).

Normal Setting:*CC Gain* should never need to be modified directly by the user. It is modified by the current calibration function from Calibration Mode. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note SLUA355A for more information.

CC Delta

This is the gain factor for calibrating out Sense Resistor, Trace, and internal Coulomb Counter (integrating ADC Delta Sigma) errors. It is used in the algorithm that reports charge and discharge in and out of the battery through the ***Remaining Capacity*** register. The difference between *CC Gain* and *CC Delta* is that the algorithm that reports ***Current*** cancels out the time base since ***Current*** does not have a time component (it reports in mA) and *CC Delta* requires a time base for reporting ***Remaining Capacity*** (it reports in mAh).

Normal Setting:*CC Delta* should never need to be modified directly by the user. It is modified by the current calibration function from Calibration Mode. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note SLUA355A for more information.

Ref Voltage

The *Ref Voltage* is based on the actual reference voltage that the bq29312A uses for reference when sending voltage readings to the bq20z80. Therefore this is a required constant in all the bq20z80 voltage computation formulas for displaying individual cell voltages (***Cell Voltage 1-4***) and the computed battery voltage (***Voltage***) in millivolts. By tweaking this value before it is used in the voltage computation formulas, then the errors introduced by the bq20z80 ADC and bq29312A reference are canceled out before they affect the reported voltages.

Normal Setting:*Ref Voltage* should never need to be modified by the user. It is modified by the voltage calibration command in Calibration mode. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note SLUA355A for more information.

AFE Corr

The AFE gain varies slightly as a function of in the input voltage. This variation is relatively constant and predictable so *AFE Corr* is used to correct for this common mode gain error of the input voltage.

Normal Setting: This register will only need to be changed under special circumstances. Its default setting is 1288. It is not modified by calibration commands.

AFE Pack Gain

The *AFE Pack Gain* is used for calibrating out errors in the bq29312A reference and bq20z80 ADC. It is used for reporting the ***Pack Voltage*** as measured on the PACK pin of the bq29312A. Therefore, this is a required constant in all the bq20z80 voltage computation formulas for displaying ***Pack Voltage*** in millivolts. By tweaking this value before it is used in the voltage computation formulas, then it changes the gain of the reported voltage which gives a method for calibrating this reported voltage.

Normal Setting: AFE Pack Gain may not need to be calibrated depending on the application. Unless ***Pack Voltage*** is used for display by the application then it will only be used for charger detection, and it does not need to be accurate for function. *AFE Pack Gain* should never need to be modified by the user. It is modified by the pack voltage calibration command in Calibration mode. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note SLUA355A for more information.

CC Offset

There are 2 offsets for calibrating the offset of the internal Coulomb Counter, board layout, sense resistor, copper traces and other offsets from the Coulomb Counter readings. *CC Offset* is the calibration value that primarily corrects for the offset error of the bq20z80 Coulomb Counter circuitry. The other offset calibration is *Board Offset* described below. To minimize external influences when doing *CC Offset* calibration either by either automatic *CC Offset* calibration or by the *CC Offset* calibration function in Calibration Mode an internal short is places across the SR1 and SR2 pins inside the bq20z80. *CC Offset* is a correction for very small noise/errors; therefore, to maximize accuracy it takes about 20 seconds to calibrate out the offset. Since it is not practical to do a 20 second offset during production, 2 different methods for calibrating CC Offset were developed.

1. The first method is to calibrate CC Offset by the putting the bq20z80 in Calibration Mode and initiating the CC Offset function as part of the entire bq20z80 calibration suite. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note SLUA355A for more information on the Calibration Mode. This is a short calibration that is not as accurate as the second method described below. Its primary purpose is to calibrate CC Offset enough so it will not affect any other Coulomb Counter calibrations. This is only intended as a temporary calibration because the automatic calibration described below is done the first time SMBus is low for more than 20 seconds which is a much more accurate calibration.
2. During normal Gas Gauge Operation (***Temperature*** is between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High*) when the SMBus clock and data lines are low for more than *Bus Low Time* seconds and ***Current*** is less than *Sleep Current* in milliAmps then an automatic *CC Offset* calibration is performed. This takes around 16 seconds and is much more accurate than the method in Calibration mode.

Normal Setting: *CC Offset* should never be modified directly by the user. It is modified by the current calibration function from Calibration Mode or by Automatic Calibration. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note SLUA355A for more information on calibration.

Board Offset

Board Offset is the second offset register. Its primary purpose is to calibrate all that the *CC Offset* does not calibrate out. This includes board layout, sense resistor and copper trace and other offsets that are external to the bq20z80 IC. This is a very long calibration and can take up to 20 seconds. Since *Board Offset* is primarily used to cancel out offsets external to the bq20z80 IC then it only has to be done on a sample LOT of bq20z80 modules for a particular PCB design. Then average the results and use this as a Board Offset throughout the life of the design. Anytime a PCB is revised then this should be done again to ensure the offset has not been affected by the board change.

Normal Setting: This value should only be set one time when all the other Data Flash constants are modified during the pack production process. It is important to note that the bq20z80 EV software uses *CC Offset Time* in the EV software formula for computing board offset. It is recommended that *CC Offset Time* be modified to 20,000 to get an accurate board offset with the above procedure (See *CC Offset Time*).

Int Temp Offset

The bq20z80 has a temperature sensor built into the IC. The *Int Temp Offset* is used for calibrating out offset errors in the measurement of the reported ***Temperature*** if the internal temperature sensor is used. The gain of the internal temperature sensor is accurate enough that a calibration for Gain is not required.

Normal Setting:*Int Temp Offset* should never need to be modified by the user. It is modified by the internal temperature sensor calibration command in Calibration mode. *Int Temp Offset* should only be calibrated if the internal temperature sensor is used. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note SLUA355A for more information on calibration.

Ext1 Temp Offset

Ext1 Temp Offset is for calibrating the offset of the thermistor connected to the TS1 pin of the bq20z80 as reported by ***Temperature***. The gain of the thermistor is accurate enough that a calibration for gain is not required.

Normal Setting:*Ext1 Temp Offset* should never need to be modified by the user. It is modified by the external temperature sensor calibration command in Calibration mode. *Ext1 Temp Offset* should only be calibrated if a thermistor is connected to the TS1 pin of the bq20z80. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note SLUA355A for more information on calibration.

Ext2 Temp Offset

Ext2 Temp Offset is for calibrating the offset of the thermistor connected to the TS2 pin of the bq20z80 as reported by ***Temperature***. The gain of the thermistor is accurate enough that a calibration for gain is not required.

Normal Setting: *Ext2 Temp Offset* should never need to be modified by the user. It is modified by the external temperature sensor calibration command in Calibration mode. *Ext2 Temp Offset* should only be calibrated if the a thermistor is connected to the TS1 pin of the bq20z80. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note SLUA355A for more information on calibration.

Config

These are all setting for adjusting Calibration Mode applied voltage, current, and temperature as well as the times associated with these calibrations. The Times should not need to be modified with normal applications. The values in Data Flash for these registers are defaults for Calibration Mode. If no other values are assigned to the calibration commands associated with each of these registers when in Calibration Mode then these default values is used. See the *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* application note SLUA355A for more information on calibration.

CC Current

This register holds the default current that is applied during the calibration process while in Calibration mode. If, while in calibration mode, the *CC Current* is not modified by calibration command then this value is what is used to calibrate *CC Gain* and *CC Delta*. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z80.
Normal Setting: This depends on the sense resistor used. Higher currents increase the voltage across the SR1 and SR2 pins which decreases noise and offset errors. It also increases the calibration accuracy because the granularity has less effect on the measurements. Good numbers for a 10 milliohm sense resistor are 2 to 3 amps.

Voltage Signal

This register holds the default voltage that is applied during the calibration process while in Calibration Mode. If, while in calibration mode, the *Voltage Signal* is not modified by calibration command then this value is what is used to calibrate *Reference Voltage* and *AFE Pack Gain*. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z80. This value is a pack voltage, not a cell voltage.
Normal Setting: This depends on the number of cells, but it is good idea to use a voltage that is within the normal operating voltages of the cells used in the application times the number of cells.

Temperature Signal

This register holds the default Temperature that is applied during the calibration process while in Calibration Mode. If, while in calibration mode, the *Temperature Signal* is not modified by calibration command then this value is what is used to calibrate all the Temperature inputs that are used in this application. Time can be saved in the calibration process if the Data Flash value can be used because that eliminates some communications to the bq20z80.
Normal Setting: This value more than any of the others must be modified using the calibration commands in Calibration Mode instead of using this Data Flash location because temperature is continually changing.

CC Offset Time

CC Offset Time is the time that the calibration command for initiating a *CC Offset* calibration will take to do a *CC Offset* calibration. This is also used in Board Offset calibration in the bq20z80 EV software.
Normal Setting: The default is 250 and the units are in milliseconds. Only use values in multiples of 250 ms. The calibration function rounds the *CC Offset Time* down to the next lower multiple of 250 ms if an exact multiple of 250 is not used. It reports a calibration error if a value less than 250 is used. Remember that this is only a temporary calibration to minimize offset effects on other CC calibrations. The Automatic Offset calibration that happens during normal Gas Gauging mode does a more accurate calibration. It is important to note that this is also used by the bq20z80 EV software to do Board Offset calibration. It is a good idea to increase this number to 20,000 to get a very accurate board offset measurement for production testing (see Board Offset) .

ADC Offset Time

ADC Offset Time is the time that the calibration command for initiating an ADC Offset calibration takes for an ADC Offset calibration. *ADC Offset* is not associated with a Data Flash location, but it is done every time Automatic *ADC Offset* is done in Gas Gauging mode and should be initiated at the same time as *ADC Offset* when in Calibration Mode.
Normal Setting: The default is 32 and the units are in milliseconds. Only use values in multiples of 32 ms. The calibration function rounds the ADC Offset Time down to the next lower multiple of 32 ms if an exact multiple of 32 is not used. It reports a calibration error if a value less than 32 is used. Remember that this is only a temporary calibration. The Automatic Offset calibration that happens during normal Gas Gauging mode keeps this value accurate.

CC Gain Time

CC Gain Time is the time that the calibration command for initiating a CC Gain calibration takes for a *CC Gain Time* calibration. It uses the value in *CC Current* over *CC Gain Time* to do the calibration.
Normal Setting: The default is 250 and the units are in milliseconds. Only use values in multiples of 250 ms. The calibration function will round the *CC Gain Time* down to the next lower multiple of 250 ms if an exact multiple of 250 is not used. It reports a calibration error if a value less than 250 is used. Depending on the current used, it is possible that 250 ms not enough time for a good calibration . It is recommended that 500 ms to 1000 ms be used for best results.

Voltage Time

Voltage Time is the time that the calibration commands for initiating a Reference Voltage or *AFE Pack Gain* calibration takes for a *Reference Voltage* or *AFE Pack Gain* calibration. These commands use the value in *Voltage Signal* over *Voltage Time* to do the calibration.
Normal Setting: The default is 1984 and the units are in milliseconds. Only use values in multiples of 1984 ms. The calibration function will round the *Voltage Time* down to the next lower multiple of 1984 ms if an exact multiple of 1984 is not used. It will report a calibration error if a value less than 1984 is used.

Temperature Time

Temperature Time is the time that the calibration commands for initiating any of the 3 temperature calibrations takes for the respective calibrations. These commands uses the value in *Temperature Signal* over *Temperature Time* to do the calibration.
Normal Setting: The default is 32 and the units are in milliseconds. Only use values in multiples of 32 ms. The calibration function rounds the *Temperature Time* down to the next lower multiple of 32 ms if an exact multiple of 32 is not used. It will report a calibration error if a value less than 32 is used.

Cal Mode Timeout

Cal Mode Timeout is the maximum amount of time allowed for all calibrations to complete before the bq20z80 reverts to Gas Gauge mode automatically. The timer for this function starts when the Call Mode command is initiated.
Normal Setting: The purpose of this function is ensure that the bq20z80 has the ability to get out of Calibration Mode on its own if it was accidentally put into Calibration Mode for any unknown reason. The default for this register is 38400 which is in units of seconds/128. This translates to 5 minutes. It is unlikely that this register will need to be modified.

Temp Model

None of these registers must not be changed for any reason. The only reason these values are listed is for the purpose of using a different thermistor; however, this is not recommended, and has not been tested with the bq20z80.

Ext Coef 1, Ext Coef 2, Ext Coef 3, Ext Coef 4

These are the coefficients for a close approximation curve match formula to the temperature curve specified for the Semitec 103AT Thermistor.

Ext Min AD

This is the minimum ADC value allowed for the Temperature conversion formula.
Normal Setting: This value is 0 and should not be changed.

Ext Max Temp

This is the maximum temperature value allowed for the Temperature conversion formula.
Normal Setting: This value is 4012 and should not be changed.

Int Coef 1, Int Coef 2, Int Coef 3, Int Coef 4

These are the coefficients for a close approximation curve match formula to the temperature curve specified for the Semitec 103AT Thermistor.

Int Min AD

This is the minimum ADC value allowed for the Temperature conversion formula. Normal Setting: This value is 0 and should not be changed.

Int Max Temp

This is the maximum temperature value allowed for the Temperature conversion formula.
Normal Setting: This value is 4012 and should not be changed.

Current

Filter

This constant defines the filter constant used in the ***Average Current*** formula. This is a very common question how this is calculated. The formula used to compute ***Average Current*** is :

New (***Average Current***) = A $\times$ *Old* (***Average Current***) + (1-A) $\times$ ***Current***

A = *Filter*/256. Default value is 239

The time constant = 1 sec/ln(1/a) (default 14.5 sec)
Normal Setting: It is unlikely that this value should ever need to be changed.

Deadband

The purpose of the *Deadband* is to create a filter window to the reported ***Current*** register where the current is reported as 0. Any negative current above this value or any positive current below this value is displayed as 0.
Normal Setting: This defaults to 3 mA. There are not many reasons to change this value. Here are a few.

1. If the bq20z80 is not calibrated.
2. *Board Offset* has not been characterized.
3. If the PCB layout has issues that cause inconsistent board offsets from board to board.
4. An extra noisy environment in conjunction with number 3.

If this value must be modified be sure and verify the CC Deadband as well.

CC Deadband

This is also referred to as Digital Filter. This works much in the same way as the *Deadband* except it works for capacity counting on the ***Remaining Capacity*** register. Any absolute voltage between SR1 and SR2 below this value does not contribute to capacity measurement. The purpose of this is to minimize the possibility of unwanted noise from being counted towards capacity.
Normal Setting: The default for this register is 34 and it is in units of 290 nanovolts. This gives a *CC Deadband* of 9.86 mV. This value is most likely too small for most applications. A better value would be 2 or 3 times this default. Unlike *Deadband* this value is not influenced by what value of sense resistor is used since this value is stored in microvolts and not milli-amps.

CC Max Deadband

This constant defines the limit in coulomb counter counts (about 10 µV/cnt) at which the coulomb counter input is measured using a sample size defined by *CC Deadband Sample*. A larger sample size is needed to measure greater resolution than can be measured with a single sample.
Normal Setting: This value should not need to be modified for any normal setting of the *CC Deadband*.

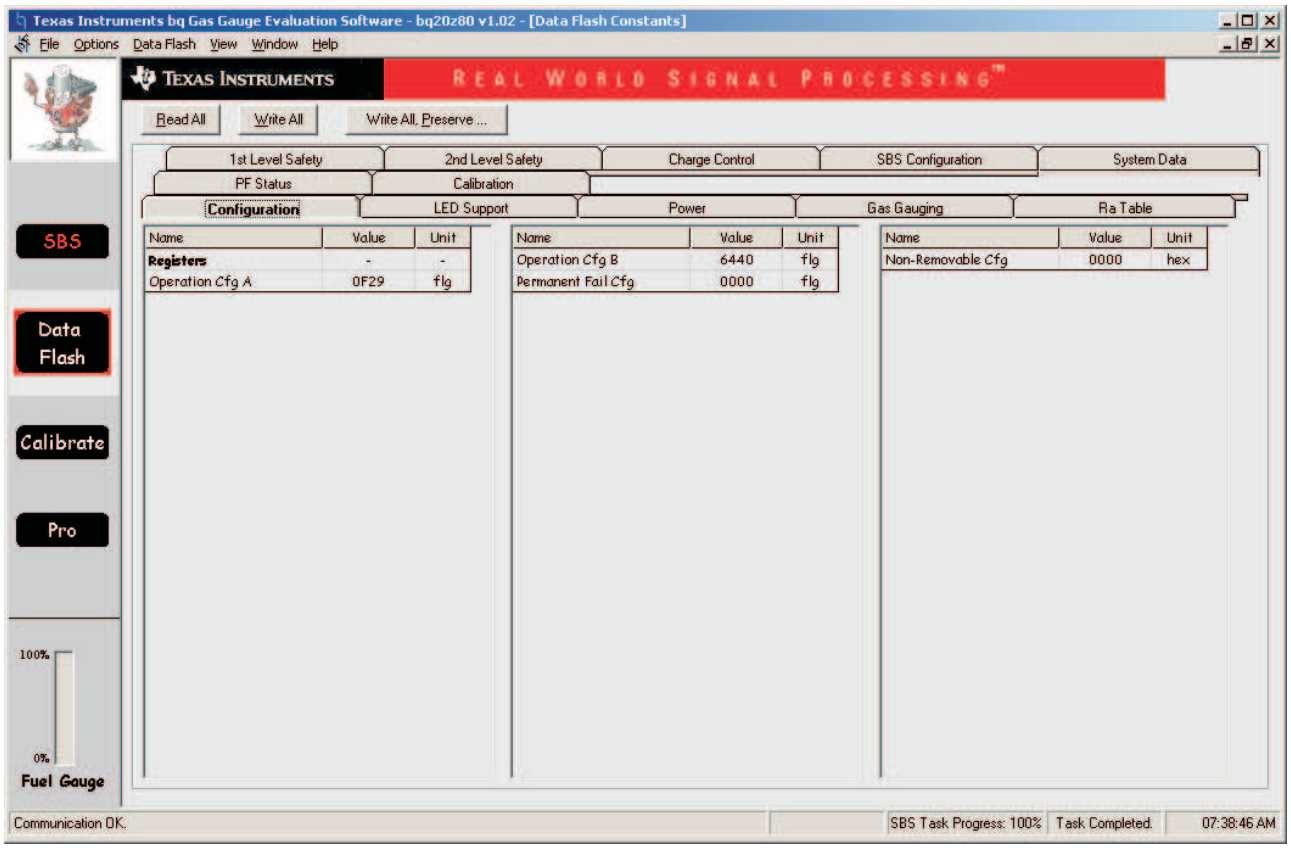
CC Deadband Sample

This constant defines the sample size of coulomb counter conversions used to measure the coulomb counter input for *CC Deadband* evaluation. A larger sample size is needed to measure greater resolution than can be measured with a single sample.
Normal Setting: This value should not need to be modified for any normal setting of the *CC Deadband*.

CC Offset Sample

CC Offset Sample is the number of coulomb counter readings that are required for an automatic *CC Offset* calibration. This is not to be confused with the CC Offset calibration done in Calibration Mode. This calibration is only done when SMBus clock and data lines are low for more than *Bus Low Time* seconds and ***Current*** is below *Sleep Current*.
Normal Setting: This default value is 64. There are 4 coulomb counter conversions per second. This results in a 16 second *CC Offset* calibration

2.9 Configuration



Registers

Operation Cfg A

This register is used to enable or disable various functions on the bq20z80. These bits are continued in *Operation Cfg B*.

LEDR	LEDRCA	CHGLED	DMODE	LED1	LED0	CC1	CC0
–	–	SLEEP	TEMP1	TEMP0	SLED	ZVCHG1	ZVCHG0

- LEDR [15]: This bit is useful to watch for device resets. If enabled, it activates the LED display with the present ***RSOC*** state after a reset has occurred. LEDs operates exactly the same as a DISP button transition function (See **LED Support** class).
  - 0: LEDs do not illuminate on reset
  - 1: LEDs illuminate in the same manner as a DISP button press after a reset has occurred.

  Normal Setting: This bit defaults to a 0 which should be used in production. This bit should normally only be set during development.

  LEDRCA [14]: If enabled, this bit forces the bq20z80 to force the LEDs to flash with a period of (2 ×*LED Flash Rate*) whenever [RCA] is set in ***Battery Status*** and the LEDs are activated. In Discharge Mode ([DSG] flag clear in ***Battery Status***), a transition from high to low on the DISP pin of the bq2z80 (DISP button transition) is required to activate the LEDs. During Charge ([DSG] flag clear in ***Battery Status***), if [CHGLED] set in *Operation Cfg A*, then DISP button transition is not required because the LEDs are activated (See **LED Support** class).
  - 0: LEDs do not flash at the *LED Flash Rate* period with [RCA] set in ***Battery Status***.
  - 1: LEDs do flash at (2 ×*LED Flash Rate*) period with [RCA] set in ***Battery Status*** if activated.

  Normal Setting: This bit defaults to a 0. It is set based on user preference.
- CHGLED [13]: If enabled, this bit forces the bq20z80 to activate the LED display whenever charging (***Current*** greater than *CHG Current Threshold*). LEDs operate exactly the same as a DISP button transition function except they do not time out and deactivate until ***Current*** is less than *CHG Current Threshold*. (See **LED Support** class)
  - 0: LEDs do not illuminate on reset
  - 1: LEDs illuminate in the same manner as a DISP button press.

  Normal Setting: This bit defaults to a 0. It is set based on user preference.
- DMODE [12]: This is the Display Mode bit which refers to LED configuration. If the Display mode bit is 0, then the display is in “Relative Mode”. If it is 1, then it is in “Absolute Mode”. In relative mode, the LED display is based on a percentage of the ***Full Charge Capacity***, which is stored in the ***RSOC*** register. If it is in absolute mode, then the LED display is based on a percentage of ***Design Capacity***, which is stored in the ***ASOC*** register.
  - 0: Number of LEDs that illuminated when activated are based on ***RSOC***.
  - 1: Number of LEDs that illuminated when activated are based on ***ASOC***.

  Normal Setting: This bit defaults to a 0 which is Relative Mode. This is the most common mode that customers use. It is important to note that ***ASOC*** can be greater than 100%. The LEDs treat any ***ASOC*** greater than 100% as 100%
- LED1, 0 [11, 10]: These bits are used to inform the bq20z80 of the number of LEDs that are being used in the application.
  - 1,1 = 5 LEDs
  - 1,0 = 4 LEDs
  - 0,1 = 3 LEDs
  - 0,0 = This is for a user defined setting as set in the **LED Support** class.

  Normal Setting: The default setting for these bits is both bits set. This is based on user preference and application.
- CC1,0 [9,8]: These bits are used to inform the bq20z80 of the number of Li-Ion battery cells in a series for the application. This setting is critical for every aspect of the Data Flash configuration with regards to voltage based functions.
  - 1,1 = 4 series cell application
  - 1,0 = 3 series cell application

– 0,1 = 2 series cell application
– 0,0 = Reserved (Not Valid)

Normal Setting: The default value for these bits are both set for a 4-series cell application. These bits are application and user dependant.

- RESERVED [7,6]: These bits are reserved

  SLEEP [5]: This bit enables or disables the ability to go to sleep when SMBus Clock and Data lines go low for Bus Low Time and ***Current*** is below *Sleep Current* (See *Sleep Current* and *Bus Low Time*)

  – 0: bq20z80 do not go to sleep with the above criteria
  – 1: bq20z80 do go to sleep when the sleep criteria is set

  Normal Setting: This bit defaults to a 1 which should be used in most applications. There are few reasons for this bit to be set to 0.
- Temp1,0 [4,3]: These bits are used to tell the bq20z80 the temperature sensor configuration. The bq20z80 can use up to 2 external sensors and there is also an internal sensor available if needed. All of these sensors are able to use various configurations to report temperature in the ***Temperature*** register.

  – 1,1 = The Average of TS1 and TS2 external inputs are used to generate ***Temperature***.
  – 1,0 = Greater Value of TS1 and TS2 external inputs are used to generate ***Temperature***.
  – 0,1 = Only Temperature sensor TS1 is used to generate ***Temperature***.
  – 0,0 = Only internal temperature sensor is used to generate ***Temperature***.

  Normal Setting: The default setting for these bits is [Temp1] cleared and [Temp0] set. This requires one external temperature sensor on TS1. The bq20z80 default configuration is for a Semitec 103AT thermistor as briefly described in the **Temp Model** subclass (See **Temp Model**). The internal temperature sensor is slightly less accurate than using a Semitc 103AT and is not recommended. It also is not as accurate because it cannot be put as close to the battery cells in the application as can be done with an external thermistor.
- SLED [2]: The serial LED option can be used to implement a much brighter display at the expense of additional hardware components. With the parallel connection, the 3.3 V output from the bq29312A. is used to power the LEDs. Using that approach, current in each LED should be limited to 3 mA. With the serial option, all LEDs can be powered from the battery voltage and driven in series through a simple constant current regulator. The current is then diverted to ground at the various nodes between the series LEDs in order to program the desired pattern. If this function is enabled, then the Permanent Failure display mode using the LEDs is disabled. (See *Operation Cfg B*). The 2 options for this bit are:

  – 0: Parallel LED configuration
  – 1: Serial LED Configuration

  Normal Setting: This bit defaults to a 0 which should be used in production for most applications. Given that serial LEDs require more components and 3 mA is usually sufficient for most applications then 0 is the most common setting for this bit.
- ZVCHG1,0 [1,0]: These bits are also known as Pre-Charge 1,0. These bits are used to tell the bq20z80 how the Pre-Charge circuit is configured in the application. It tells the bq2z80 what pin on the bq29312A to use for Pre-Charge functions when required.

  – 1,1 = No action is taken in Pre-Charge functions with this setting.
  – 1,0 = OD pin is used for Pre-Charge functions.
  – 0,1 = Charge FET is used for Pre-Charge functions.
  – 0,0 = ZVCHG FET is being used for Pre-Charge functions.

  Normal Setting: If using a separate Pre-Charge FET it is recommended not to use the OD pin for this function because it does not have good “zero volt charging” capabilities when a battery is completely dead. Therefore, the ZVCHG pin should be used because it has excellent clamping abilities. The default is for using the Charge FET pin on the bq29312A.

Operation Cfg B

This register is used to enable or disable various functions on the bq20z80. This is a continuation of *Operation Cfg A*.

PFD1	PFD0	RESCAP	NCSMB	NRCHG	CSYNC	CHGTERM	CCT
CHGSUP	OTFET	CHGFET	CHGIN	NR	CPE	HPE	BCAST

- PFD1,0 [15,14]: These bits are used to configure how the bq20z80 is supposed to display permanent failure data through the LEDs if enabled. If [SLED] set in *Operation Cfg A* then this function is disabled. If there is no permanent failure, then no action is taken on the LEDs even if this function is enabled.
  - 1,1 = Permanent Failure data is displayed on the LEDs after the LEDs display the state of charge data (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) when the DISP button is activated. The DISP button does not have to be activated for more than *LED Hold Time*.
  - 1,0 = Permanent Failure data is disabled with this setting
  - 0,1 = Permanent Failure data is displayed on the LEDs after the LED display indicates the SOC data (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*), but only if DISP button is activated for more than *LED Hold Time*.
  - 0,0 = Permanent Failure display is disabled with this setting

  Normal Setting: The default setting here is [PFD1] cleared and [PFD0] set. This gives the ability to get permanent failure data from a damaged battery pack even if communications are not possible as long as the bq20z80 CPU is still functioning.
- RESCAP [13]: The bq20z80 reports ***Remaining Capacity*** and ***Full Charge Capacity*** that is falsely lower than the actual capacity of the battery as defined by the *Reserve Cap-mAh* in mAh mode or *Reserve Cap-mW* in mWh mode (configured by [CAPM] in ***Battery Mode***). RESCAP sets a load compensation for this function.
  - 0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
  - 1: If set to a 1, then a more normal rate of load compensation as defined by Load Select is applied to this reserve capacity. (See **IT Cfg** class)

  Normal Setting: This bit defaults to a 1. For most applications, this along with *Load Select* should be left at the default values.
- NCSMB [12]: This bit is used to enable a special mode for the SMBus engine in the bq20z80 where it allows for unlimited timeouts for SMBus communications more like I^2C. This mode was made for customers that were using older legacy parts that had longer timeouts and were not SMBus compliant.
  - 0: Timeout extension is disabled.
  - 1: Unlimited Timeout extension enabled.

  Normal Setting: The default for this register is 0. It is recommended that this always be set to 0. There have been many complications with customers using this function in the past. When set to a 1, it is important to note that if clocking in data with a SMBus read command and the communication gets interrupted with data low then data can be stuck low until more clocks are sent to finish the communication.
- NRCHG [11]: This bit is used to configure whether or not the bq20z80 turns off the Charge FET when it goes to Sleep if [NR] bit is set in Operation Cfg B. If [NR] cleared then this bit is not used.
  - 0: Charge FET turns off in sleep mode as long as the bq20z80 is setup with [NR] set.
  - 1: Charge FET remains on in sleep mode with the [NR} bit set.

  Normal Setting: This bit defaults to a 0 which should be used for most applications with [NR] set. This could be a problem for some applications that expect the battery to start charging immediately when charge is applied when asleep.
- CSYNC [10]: This bit is used in the Primary Charge Termination Algorithm (See *Maintenance Current*). When this bit is set, then with a Primary Charge Termination the bq20z80 writes the ***Remaining Capacity*** to ***Full Charge Capacity***
  - 0: ***Remaining Capacity*** is not written up to ***Full Charge Capacity*** on Primary Charge Termination.
  - 1: ***Remaining Capacity*** is written up to ***Full Charge Capacity*** on Primary Charge Termination.

  Normal Setting: The default setting for this bit is 1. This should be used for most applications to ensure that the Remaining Capacity starts from Full Charge Capacity when the charger terminates charging. This is a synchronization function to ensure the bq20z80 discharges from full when it has

been determined that the battery is full.

- CHGTERM [9]: This bit enables the ability for the bq20z80 to turn off [TCA] and [FC] in ***Battery Status*** after a Primary Charge Termination is detected and then current falls below the *Taper Current* for 2 consecutive periods of *Taper Current Window*.
  - 0: bq20z80 does not clear [TCA] and [FC] in ***Battery Status*** after a Primary Charge Termination.
  - 1: bq20z80 does clear [TCA] and [FC] in Battery Status after a Primary Charge Termination.

  Normal Setting: This bit defaults to 0. This should be acceptable for most applications.
- CCT [8]: This bit configures which method the bq20z80 will use for incrementing ***Cycle Count***.
  - 0: If set to 0, then the bq20z80 increments ***Cycle Count*** by 1 with every cumulative discharge of *Cycle Count Threshold* in mAh. This discharge does not have to be consecutive. The bq20z80 accumulates all discharge current for this calculation even when broken up by periods of charge.
  - 1: if set, then when the bq20z80 accumulates enough discharge capacity equal to (*CC%*×*FCC*) then it increments *Cycle Count* by 1

  Normal Setting: This bit defaults to a 0. This setting is application specific.
- CHGSUSP [7]: This bit enables the ability to turn off the Charge FET and/or Pre-Charge FET in charge suspend mode (See **Charge Control** Class).
  - 0 = The Charge FET is unaffected by any type of charge suspension.
  - 1 = The Charge FET and/or Pre-Charge FET are opened with any charge suspension.

  Normal Setting: the default setting for this bit is 0. It is common for this to be set to 1 to give the bq20z80 the control for additional protection.
- OTFET [6]: This bit is used to configure how the bq20z80 controls the current FETs (Charge or Discharge) during *Over Temp Chg* or *Over Temp Dsg* faults. (See *Over Temp Chg* and *Over Temp Dsg*)
  - 0: FET control is unaffected by any *Over Temp Chg* or *Over Temp Dsg* faults.
  - 1: During a *Over Temp Chg* fault the Charge FET is opened. During a *Over Temp Dsg* fault the Discharge FET is opened.

  Normal Setting: This bit defaults to a 1 which should be used in production for most applications. Over temperature conditions can be dangerous and every level of protection possible should be used.
- CHGFET [5]: This bit is used to configure how the bq20z80 controls the Charge FETs when [TCA] gets set in ***Battery Status***. (See *TCA Set* % for an explanation for when [TCA] gets set).
  - 0: Charge FET is unaffected anytime [TCA] gets set.
  - 1: Charge FET is turned off anytime [TCA] gets set.

  Normal Setting: This bit defaults to a 0 which should be used in production for most applications. Setting it to a 1 turns the Charge FET off is only if *Maintenance Current* is set to 0.
- CHGIN [4]: This bit is used to configure how the bq20z80 controls the Charge FETs when in charge inhibit mode. (See *Chg Inhibit Temp Low* and *Chg Inhibit Temp High*).
  - 0: Charge FET is unaffected when in charge inhibit mode.
  - 1: Charge FET is turned off when in charge inhibit mode.

  Normal Setting: This bit defaults to a 0 which should be acceptable for most applications. It is important to note that this is different than charge suspend mode because this inhibits the charge cycle from occurring. This function acts while discharging.
- NR [3]: Use this bit to configure the bq20z80 for either a removable or a non removable battery pack. A removable pack uses the System Present pin (PRES) and a nonremovable pack does not. This affects many functions in the bq20z80. Primarily it affects the way it handles recovery methods of most fault conditions. A removable pack can clear many fault conditions by simple removal and reinsertion. With [NR] set, the *NR Config* register is used to enable many nonremovable pack fault recovery methods for use with a removable pack. (See *NR Config* and **Current** subclass in **1st Level Safety** class)
  - 0: Configures battery for removable mode. Transition on System Present pin (PRES) triggers certain recovery functions. *NR Config* can be used to enable nonremovable functions for this mode as well
  - 1: Configures battery for nonremovable mode.

  Normal Setting: Default for this bit is application specific. Set to 0 for batteries that are removed, and use the PRES pin. Set to 1 for packs that do not use the PRES pin.

- CPE [2]: This bit enables or disables PEC error correction on SMBus Master Mode messages that the bq20z80 broadcasts to the SMBus Device Address 0x12 (SMBus charger device address) (See SBS and SMBus specification that can be downloaded from the web).
  - 0: No PEC byte is sent to SMBus Device Address 0x12.
  - 1: Every broadcast from the bq20z80 to SMBus Device Address 0x12 includes a PEC byte as the last byte sent.

  Normal Setting: If a smart charger (SMBus Device Address 0x12) is used that is PEC capable, then this should be set to a 1. It is always recommended to use PEC when possible.
- HPE [1]: This bit enables or disables PEC error correction on SMBus Master Mode messages that the bq20z80 broadcasts to the SMBus Device Address 0x14 (SMBus Host device address)
  - 0: No PEC byte is set to SMBus Device Address 0x14. (See SBS and SMBus specification that can be downloaded from the web)
  - 1: Every broadcast from the bq20z80 to SMBus Device Address 0x14 includes a PEC byte as the last byte sent.

  Normal Setting: If a host (SMBus Device Address 0x14) is PEC capable then this should be set to a 1. It is always recommended to use PEC when possible.
- BCAST [0]: This bit enables or disables Master Mode Message broadcasting periodically to a smart charger or host. The bq20z80 broadcasts are completely disabled (See SBS and SMBus specification that can be downloaded from the web)
  - 0: The bq20z80 never masters the SMBus for any reason.
  - 1: The bq20z80 is enabled to Master the bus periodically to inform a host or charger of critical information

  Normal Setting: If a host (SMBus Device Address 0x14) is PEC capable then this should be set to a 1. It is always recommended to use PEC when possible.

Permanent Fail Cfg

This enables or disables the various permanent failure protection functions ability to activate the SAFE outputs ($\overline{\text{SAFE}}$ and SAFE pins) or not when the function is triggered.

–	–	–	XSOPT	XSOCD	XSOCC	XAFE_P	XAFE_C
XDFF	XDFETF	XCFETF	XCIM	XSOTD	XSOTC	XSOV	XPFIN

- RESERVED [15–13]: These bits are reserved.
- XSOPT [12]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with an Open Thermistor failure condition. With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high, and the $\overline{\text{SAFE}}$ pin did go low. (See *SOC Chg*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a an Open Thermistor failure condition
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for an Open Thermistor failure condition

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOPT] be set for production packs to protect against hazardous failures.
- XSOCD [11]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Current in the discharge direction condition . With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOC Chg*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Current in the discharge direction Condition
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Safety Over Current in the discharge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing

of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOCD] be set for production packs to protect against hazardous failures.

- XSOCC [10]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Current in the charge direction condition. With this function enables the bq20z80 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOC Dsg*).
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Current in the charge direction Condition
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Safety Over Current in the charge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOCC] be set for production packs to protect against hazardous failures.
- XAFE_P [9]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a periodic AFE verification failure. With this function enabled, the bq20z80 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *AFE Check Time*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a periodic AFE verification failure.
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a periodic AFE verification failure.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XAFE_P] be set for production packs to protect against hazardous failures.
- XAFE_C [8]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with an AFE communication verification failure. With this function enabled the bq20z80 will also write 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *AFE Fail Limit*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for an AFE communication verification failure.
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for an AFE communication verification failure.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XAFE_C] be set for production packs to protect against hazardous failures.
- XDFF [7]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Data Flash verification failure. With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *PF Flags 1*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Data Flash verification failure.
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Data Flash verification failure.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XDFF] be set for production packs to protect against hazardous failures.
- XDFETF [6]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin

low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Discharge FET Failure condition . With this function enabled, the bq20z80 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *FET Fail Limit*)

  – 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Discharge FET Failure Condition.
  – 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Discharge FET Failure Condition.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XDFETF] be set for production packs to protect against hazardous failures.

- XCFETF [5]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Charge FET Failure condition . With this function enabled, the bq20z80 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *FET Fail Limit*)
  – 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Charge FET Failure Condition.
  – 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Charge FET Failure Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XCFETF] be set for production packs to protect against hazardous failures.
- XCIM [4]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a extreme Cell Imbalance condition . With this function enabled, the bq20z80 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *Cell Imbalance Fail Voltage*)
  – 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a extreme Cell Imbalance Condition.
  – 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a extreme Cell Imbalance Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XCIM] be set for production packs to protect against hazardous failures.
- XSOTD [3]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the /SAFE pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Temperature in the discharge direction condition. With this function enabled, the bq20z80 writes 0x3672 in th *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOT Chg*)
  – 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Temperature in the discharge direction Condition.
  – 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Safety Over Temperature in the discharge direction Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOTD] be set for production packs to protect against hazardous failures.
- XSOTC [2]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Temperature in the charge direction condition . With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOT Chg*)
  – 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over

Temperature in the charge direction Condition.

– 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Safety Over Temperature in the charge direction Condition.

Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOTC] be set for production packs to protect against hazardous failures.

- XSOV [1]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a Safety Over Voltage condition . With this function enabled, the bq20z80 writes 0x3672 in the *Fuse Flag* to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *SOV Threshold*).
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a Safety Over Voltage Condition.
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a Safety Over Voltage Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XSOV] be set for production packs to protect against hazardous failures.
- XPFIN [0]: This bit enables the ability for the bq20z80 to force the SAFE pin high and the $\overline{\text{SAFE}}$ pin low which is intended to blow a fuse or trigger a hardware event to protect against a hazardous failure with a PF input low condition . With this function enabled, the bq20z80 writes 0x3672 in the Fuse Flag to indicate that the SAFE pin did go high and the $\overline{\text{SAFE}}$ pin did go low. (See *PFIN Detect Time*)
  - 0: The SAFE pins are not activated and the *Fuse Flag* is not written to 0x3672 for a PF input low Condition.
  - 1: The SAFE pin is driven high and $\overline{\text{SAFE}}$ pin is driven low on the bq20z80. The *Fuse Flag* is written to 0x3672 for a PF input low Condition.

  Normal Setting: This basically enables the permanency of a permanent failure. Even with the clearing of the permanent failure this is intended to render the pack useless. This bit defaults to a 0. This is only to prevent a permanent failure forcing a blown fuse during development. It is recommended that [XPFIN] be set for production packs to protect against hazardous failures.

Non-Removable Cfg

This register affects the way the bq20z80 handles recovery methods for most fault conditions. A removable pack can clear many fault conditions by simple removal and reinsertion. With [NR] set, the *NR Config* register can be used to enable many nonremovable pack fault recovery methods for use with a removable pack. NR Config can be used to enable nonremovable fault recovery functions for a battery pack that is configured as removable.

–	–	OCD	OCC	OCD2	OCC2	–	–
–	–	OC	–	–	AOCD	SCC	SCD

- RESERVED [15, 14]: These bits are reserved
- OCD [13]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with an Over Current in the discharge direction fault (See (OC*1st Tier) Dsg*).
  - 0: The nonremovable recovery option associated with *OC (1st Tier) Dsg* is not enabled.
  - 1: The nonremovable recovery option associated with *OC (1st Tier) Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- OCC [12]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with an Over Current in the charge direction fault (See *OC (1st Tier) Chg*).
  - 0: The nonremovable recovery option associated with *OC (1st Tier) Chg* is not enabled
  - 1: The nonremovable recovery option associated with *OC (1st Tier) Chg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR]

cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.

- OCD2 [11]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with a second level Over Current in the discharge direction fault (See *OC (2nd Tier) Dsg*).
  - 0: The nonremovable recovery option associated with *OC (2nd Tier) Dsg* is not enabled.
  - 1: The nonremovable recovery option associated with *OC (2nd Tier) Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- OCC2 [10]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the non removable configuration ([NR] set in *Operation Cfg B*) with a second level Over Current in the charge direction fault (See *OC (2nd Tier) Dsg*).
  - 0: The nonremovable recovery option associated with *OC (2nd Tier) Chg* is not enabled.
  - 1: The nonremovable recovery option associated with *OC (2nd Tier) Chg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- RESERVED [9-3]: These bits are reserved.
- AOCD [2]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE Over Current in the discharge direction fault (*AFE OC Dsg*).
  - 0: The nonremovable recovery option associated with *AFE OC Dsg* is disabled.
  - 1: The nonremovable recovery option associated with *AFE OC Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- SCC [1]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE short circuit in the charge direction fault (*AFE SC Chg*).
  - 0: The non removable recovery option associated with *AFE SC Chg* is disabled.
  - 1: The non removable recovery option associated with *AFE SC Chg* is enabled.

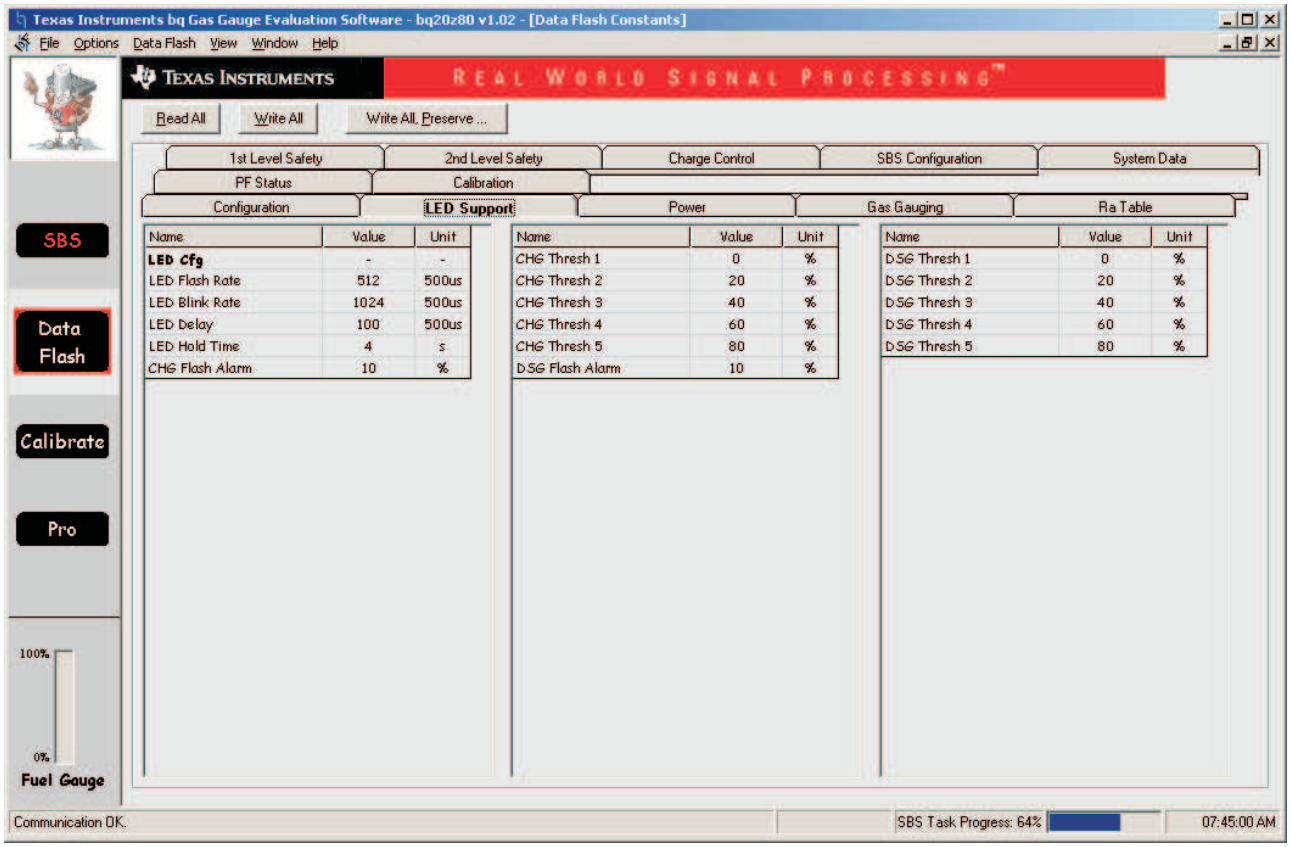
  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.
- SCD [0]: [NR] must be clear in *Operation Cfg B* for this bit setting to be used in the bq20z80. This bit enables the fault recovery method that is normally reserved for the nonremovable configuration ([NR] set in *Operation Cfg B*) with a AFE short circuit in the discharge direction fault (*AFE SC Dsg*).
  - 0: The nonremovable recovery option associated with *AFE SC Dsg* is disabled.
  - 1: The nonremovable recovery option associated with *AFE SC Dsg* is enabled.

  Normal Setting: This bit defaults to 0. It is not very common to use this bit in conjunction with [NR] cleared in *Operation Cfg B*. The available recovery methods for removable packs are usually sufficient.

2.10 LED Support

There are 3 different display modes for the LEDs that need clarification to help understand the **LED Support** class.

- Blinking: When the display is said to be blinking, then the word “blinking” is used to refer to the LED located closest to the LED used to indicate 100% that is illuminated and “blinking” when the LED display is activated and displaying SOC (state of charge). Only this “topmost” activated LED in the display blinks. All other LEDs that are activated is steady state when activated. (see *LED Blink Rate*)
- Flashing: When the display is said to be flashing then the word “flashing” means all LEDs that are activated to indicate the SOC will flash with a period of (2 ×*LED Flash Rate*).
- Delay: When the display is activate, all LEDs that are required to indicate the SOC may not illuminate at the same time. Starting from the LED that represents the lowest SOC, there can be a delay (*LED Delay*) between each LED illuminating from the LED that represents the lowest possible SOC up to the LED that represents the present SOC.



LED Cfg

LED Flash Rate

LED Flash Rate is used to configure the periodic rate at which the activated LEDs flashes with a (2 ×*LED Flash Rate*) period and a 50% duty cycle when the LEDs are required to flash. Only the LEDs that are requested to illuminate based on SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) will flash. LEDs are Required to flash with the following conditions:

1. When Charging ([DSG] cleared in ***Battery Status***) with the following conditions:
   a. When [CHGLED] set in *Operation Cfg A*
      a. [LEDRCA] set in *Operation Cfg A*
      b. [RCA] set in ***Battery Status***
   b. High to low transition on the DISP pin (button press) with the following requirements:
      a. LEDRCA] set in *Operation Cfg A*
      b. [[RCA] set in ***Battery Status***
2. When Discharging ([DSG] set in ***Battery Status***) with a high to low transition on the DISP pin (button press) and the following conditions:
   a. LEDRCA] set in *Operation Cfg A*
   b. [RCA] set in ***Battery Status***

   Normal Setting: This setting depends on user preference however for most applications the default is acceptable. *LED Flash Rate* does not affect the operation of the part in any way except the display. The default is 512 and its in units of 500 micro seconds. That means that the default is 256 ms.

LED Blink Rate

The bq20z80 can be configured to blink the topmost LED in the LED display at a rate stored in *LED Blink Rate* . When the LED display is activated, the topmost LED is the illuminated LED closest to the LED that is used to indicate 100% SOC. The topmost LED in the LED string will blink with a (2 ×*LED Blink Rate*) period and a 50% duty cycle when charging ([DSG] cleared in ***Battery Status***) with the following conditions:

1. Charging (***Current*** > *Chg Current Threshold*) and [CHGLED] set in *Operation Cfg A*.
2. High to low transition on the DISP pin (button press)

This function is disabled (no blinking of topmost LED) if *LED Blink Rate* = 0.
Normal Setting: This setting depends on user preference however for most applications the default is acceptable. *LED Blink Rate* does not affect the operation of the part in any way except the display. The default is 1024 and is in units of 500 micro seconds. That means that the default is 512 ms.

LED Delay

The bq20z80 can be configured to put a delay in between the illumination of each LED segment during the display activation sequence. Upon request for activation of the LED display either by button press or charging, the LEDs ramps up to the topmost LED with a delay in between each LED illuminating in the sequence. The topmost LED is the illuminated LED that is closest to the LED that illuminates with 100% SOC when the LEDs are requested. If *LED Delay* = 0 then this function is disabled (no delay between LEDs illuminating).
Normal Setting: This setting depends on user preference however for most applications the default is acceptable. *LED Delay* does not affect the operation of the part in any way except the display. The default for this register is 100 in units of 500 micro seconds. So this would mean the default is 50 ms.

LED Hold Time

LED Hold Time defines the time that the LEDs remain active once all LEDs required to indicate the current SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) are active. When the request is registered, either by high to low transition on the DISP pin (button press) or charging, then the LED activation sequence is initiated then the LEDs must ramp up (see *LED Delay*) to all LEDs illuminating that are requested. When the ramp up completes, then an internal *LED Hold Time* timer is initiated. When the *LED Hold Time* timer expires, the LED display is deactivated.
Normal Setting: This setting depends on user preference however for most applications the default is acceptable. *LED Delay* does not affect the operation of the part in any way except the display. The default for this register is 4 seconds.

CHG Flash Alarm

The value in *CHG Flash Alarm* is only enabled if bits [LED1] and [LED0] in Operation Cfg A are set to "User" defined (both bits clear), otherwise this register is ignored. *CHG Flash Alarm* is used in an alternative method for alerting user to a low capacity condition. This function is completely independent of [LEDRCA] set in *Operation Cfg A*. This register is set as a function of SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*). This function only operates when charging. If SOC% is at or below the *CHG Flash Alarm* then the LEDs indicating the SOC% flashes at the *LED Flash Rate* with the following conditions:

1. When Charging ([DSG] cleared in ***Battery Status***) and [CHGLED] set in *Operation Cfg A* .
2. High to low transition on the DISP pin (button press)

Normal Setting: The default setting for this register is 10%. This should be acceptable for most applications.

CHG Thresh 1

The value in *CHG Thresh 1* is only enabled if bits [LED1] and [LED0] in Operation Cfg A are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in Battery Status) for *CHG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 (The LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st LED segment is active with SOC% within 0% to *CHG Thresh 1*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers. Do not set above *CHG Thresh 2*.

CHG Thresh 2

The value in *CHG Thresh 2* is only enabled if bits [LED1] and [LED0] in Operation Cfg A are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in ***Battery Status***) for *CHG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1-5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 and LED 2 (The LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st and 2nd LED segments is active with SOC% above *CHG Thresh 1* and equal to or below *CHG Thresh 2*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers. Do not set above *CHG Thresh 3*.

CHG Thresh 3

The value in *CHG Thresh 3* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in ***Battery Status***) for *CHG Thresh 1–5* to be available for LED requests, otherwise DSG Thresh 1-5 are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1, LED2, and LED 3 (The 3rd LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st , 2nd, and 3rd LED segments is active with SOC% above *CHG Thresh 2* and equal to or below *CHG Thresh 3*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers. Do not set above *CHG Thresh 4*.

CHG Thresh 4

The value in *CHG Thresh 4* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in ***Battery Status***) for CHG Thresh 1–5 to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1, LED 2, LED 3 and LED 4 (The 4 LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st, 2nd, 3rd, and 4th LED segments is active with SOC% above *CHG Thresh 3* and equal to or below *CHG Thresh 4*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers. Do not set above *CHG Thresh 5*.

CHG Thresh 5

The value in *CHG Thresh 5* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be charging ([DSG] cleared in ***Battery Status***) for *CHG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 through LED 5 (The last LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then LED segments 1–5 is active with SOC% above *CHG Thresh 4*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *CHG Thresh 1–5* registers.

DSG Flash Alarm

The value in *DSG Flash Alarm* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. *Dsg Flash Alarm* is used in an alternative method for alerting user to a low capacity condition. This function is completely independent of [LEDRCA] set in *Operation Cfg A*. This register is set as a function of SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*). This function only operates when discharging ([DSG] set in ***Battery Status***). If SOC% is at or below the *Dsg Flash Alarm*, then the LEDs indicating the SOC% flashes at the *LED Flash Rate* with a high to low transition on the DISP pin (button press).
Normal Setting: The default setting for this register is 10%. This should be acceptable for most applications.

DSG Thresh 1

The value in *DSG Thresh 1* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in ***Battery Status***) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 (The LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st LED segment is active with SOC% within 0% to *DSG Thresh 1*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers. Do not set above *CHG Thresh 2*.

DSG Thresh 2

The value in *DSG Thresh 2* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in ***Battery Status***) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 and LED 2 (The LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st and 2nd LED segments is active with SOC% above *CHG Thresh 1* and equal to or below *DSG Thresh 2*.

Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to “User” defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers. Do not set above *CHG Thresh 3*.

DSG Thresh 3

The value in *DSG Thresh 3* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in ***Battery Status***) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1, LED2, and LED 3 (The 3rd LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st, 2nd, and 3rd LED segments is active with SOC% above *CHG Thresh 2* and equal to or below *DSG Thresh 3*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers. Do not set above *CHG Thresh 4*.

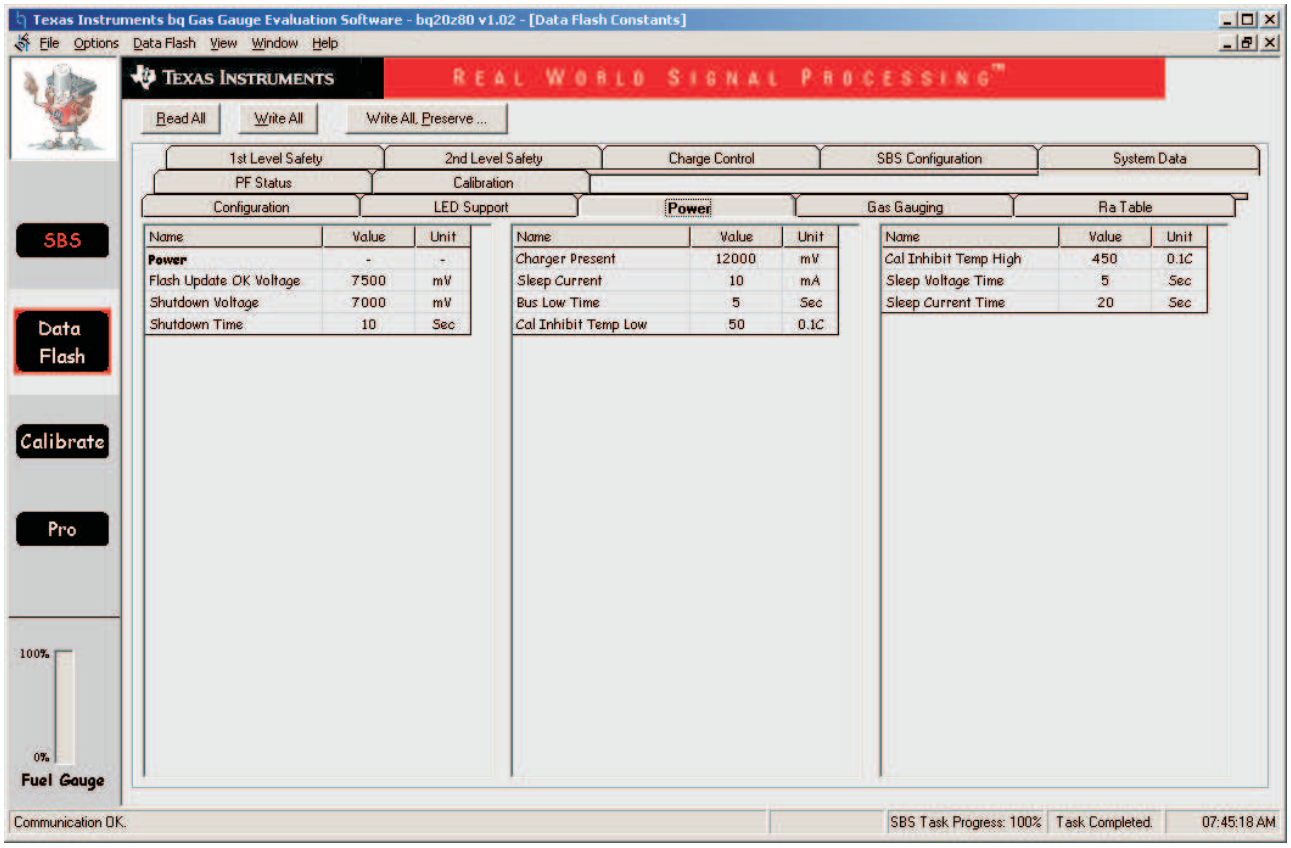
DSG Thresh 4

The value in *DSG Thresh 4* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in ***Battery Status***) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1, LED 2, LED 3 and LED 4 (The 4 LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then the 1st, 2nd, 3rd, and 4th LED segments is active with SOC% above *CHG Thresh 3* and equal to or below *DSG Thresh 4*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers. Do not set above *CHG Thresh 5*.

DSG Thresh 5

The value in *DSG Thresh 5* is only enabled if bits [LED1] and [LED0] in *Operation Cfg A* are set to "User" defined (both bits clear), otherwise this register is ignored. Also, the battery must be discharging ([DSG] set in ***Battery Status***) for *DSG Thresh 1–5* to be available for LED requests, otherwise *DSG Thresh 1–5* are used. This register configures the ranges that SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) must be within for LED 1 through LED 5 (The last LED segment above the LED segment that indicates at least 0% capacity) to illuminate when requested. If this register is enabled, then LED segments 1–5 is active with SOC% above *DSG Thresh 4*.
Normal Setting: This register is user and application dependent. It is only used if bits [LED1] and [LED0] in Operation Cfg A are set to "User" defined (both bits clear). Typical use is to divide the number of LEDs in the application and use this value to configure the *DSG Thresh 1–5* registers.

2.11 Power



Power

Flash Update OK Voltage

This register controls one of several data flash protection features. It is very critical that data flash is not updated when the battery voltage is too low. Data Flash programming takes much more current than normal operation of the bq20z80/bq29312A chipset and with a depleted battery this current can cause the battery voltage to crater (drop dramatically) forcing the bq20z80 into reset before completing a data flash write. The effects of an incomplete Data Flash write can corrupt the memory resulting in unpredictable and extremely undesirable results. The voltage setting in *Flash Update OK Voltage* is used to prevent any writes to the data flash below this value. If a charger is detected then this register is ignored.

Normal Setting: The default for this register is 7500 millivolts. For 2-cell applications, this can cause production issues with writing to the data flash because at nominal cell voltages, 2-cell applications can easily be below 7500 millivolts. The way to solve this problem is to connect a charger voltage to the battery which overrides this register while connected. Ensure that this register is set to a voltage where the battery has plenty of capacity to support data flash writes but below any normal battery operation conditions.

Shutdown Voltage

The bq20z80 goes into shutdown mode when ***Voltage*** falls below the *Shutdown Voltage* for at least Shutdown Time seconds. Also ***Current*** must be less than 0 and the ***Pack Voltage*** must be less than *Charger Present* for the entire time. (See *Shutdown Time*)

Normal Setting: This voltage should be far below any normal operating voltage but above any threshold that can cause damage to the cells. This threshold is met after the Charge and Discharge FETs are turned off from an under voltage fault condition.

Shutdown Time

When the following conditions are met:

1. ***Voltage*** is below *Shutdown Voltage*.
2. ***Current*** is less than 0.
3. ***Pack Voltage*** less than *Charger Present*

Then the *Shutdown Time* timer is initiated. If the above conditions remain until the *Shutdown Time* timer expires, then the bq20z80 goes into shutdown mode. Every time the bq20z80 wakes up from shutdown mode, then the *Shutdown Time* timer is reset meaning it is not possible for the bq20z80 to go back into shutdown mode for *Shutdown Time* seconds after waking. When in shutdown mode, VCC is completely removed from the bq20z80 by the bq29312A. (See *Shutdown Voltage*)
Normal Setting: The default for this register is 10 seconds. Between 10–20 seconds is acceptable for most applications. It is recommended not to go below 10 seconds to prevent an oscillation going into and out of shutdown mode.

Charger Present

A charger is deemed present when ***Pack Voltage*** is at or above this level.
Normal Setting: It is important to note that a charger detection because this function prevents shutdown by either a ***Manufacture Access*** command or *Shutdown Voltage*. Some applications with external voltage sources can confuse the shutdown detection which prevents the bq20z80 shutdown mode from functioning properly. The bq29312A wakes up with a voltage above the “Start-up” voltage which is a wake up feature built into the bq29312A (see the bq29312A data sheet (SLUS629A)). If there is an external voltage source that has a voltage above the “Start-up” voltage threshold, but below the *Charger Present* threshold, then the bq20z80 oscillates between awake and shutdown. This causes abnormal operational side effects. Therefore, it is recommended that *Charger Present* be set to 3500 mV if there are any external voltage sources. Otherwise, this voltage can be set to between (3000–4000 mV per cell) × (number of cells) .

Sleep Current

When ***Current*** is less than *Sleep Current* or greater than (–)*Sleep Current* in milliAmps and the following conditions are met:

1. ***Temperature*** is between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High*
2. SMBus clock and data lines are low for more than *Bus Low Time seconds*.
3. [Sleep] is set in *Operation Cfg A*.

Then the bq20z80 does a *CC Offset* calibration, and then goes to sleep.
Normal Setting: This setting should be below any normal application currents. The default is 10 mA which should be sufficient for most applications.

Bus Low Time

When SMBus clock and data lines are low for more than *Bus Low Time* seconds and the following conditions are met:

1. ***Current*** is less than Sleep Current or greater than (-)Sleep Current in milliAmps
2. ***Temperature*** is between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High*.

Then the bq20z80 does a *CC Offset* calibration and then goes to sleep. [Sleep] in *Operation Cfg A* does not affect the calibration portion of this detection.
Normal Setting: This setting should be below any normal application currents. The default is 5 seconds which should be sufficient for most applications. Do not go below 2 seconds to protect against false triggering.

Cal Inhibit Temp Low

For the bq20z80 to perform a *CC Offset* and ADC offset calibration prior to entering sleep mode, ***Temperature*** must be between *Cal Inhibit Temp Low* and *Cal Inhibit Temp High* along with the following conditions:

1. ***Current*** is less than *Sleep Current* or greater than (–)*Sleep Current* in milliAmps.
2. SMBus clock and data lines are low for more than *Bus Low Time seconds*.

Normal Setting: The default for this application is 5° or 50 in 0.1°C units. This should not need to be changed. The bq20z80 does not need to do a *CC Offset* calibration every time the bq20z80 goes to sleep and it definitely does not need to do it at extreme temperatures to prevent temperature drift from decreasing the offset calibration accuracy.

Cal Inhibit Temp High

For the bq20z80 to perform a *CC Offset* and internal ADC offset calibration prior to entering sleep mode, ***Temperature*** must be between *Cal Inhibit Temp High* and *Cal Inhibit Temp High* along with the following conditions:

1. ***Current*** is less than *Sleep Current* or greater than (–)*Sleep Current* in milliAmps
2. SMBus clock and data lines are low for more than *Bus Low Time* seconds

Normal Setting: The default for this application is 45° or 450 in 0.1°C units. This should not need to be changed. The bq20z80 does not need to do a *CC Offset* calibration every time the bq20z80 goes to sleep and it definitely does not need to do it at extreme temperatures to prevent temperature drift from decreasing the offset calibration accuracy.

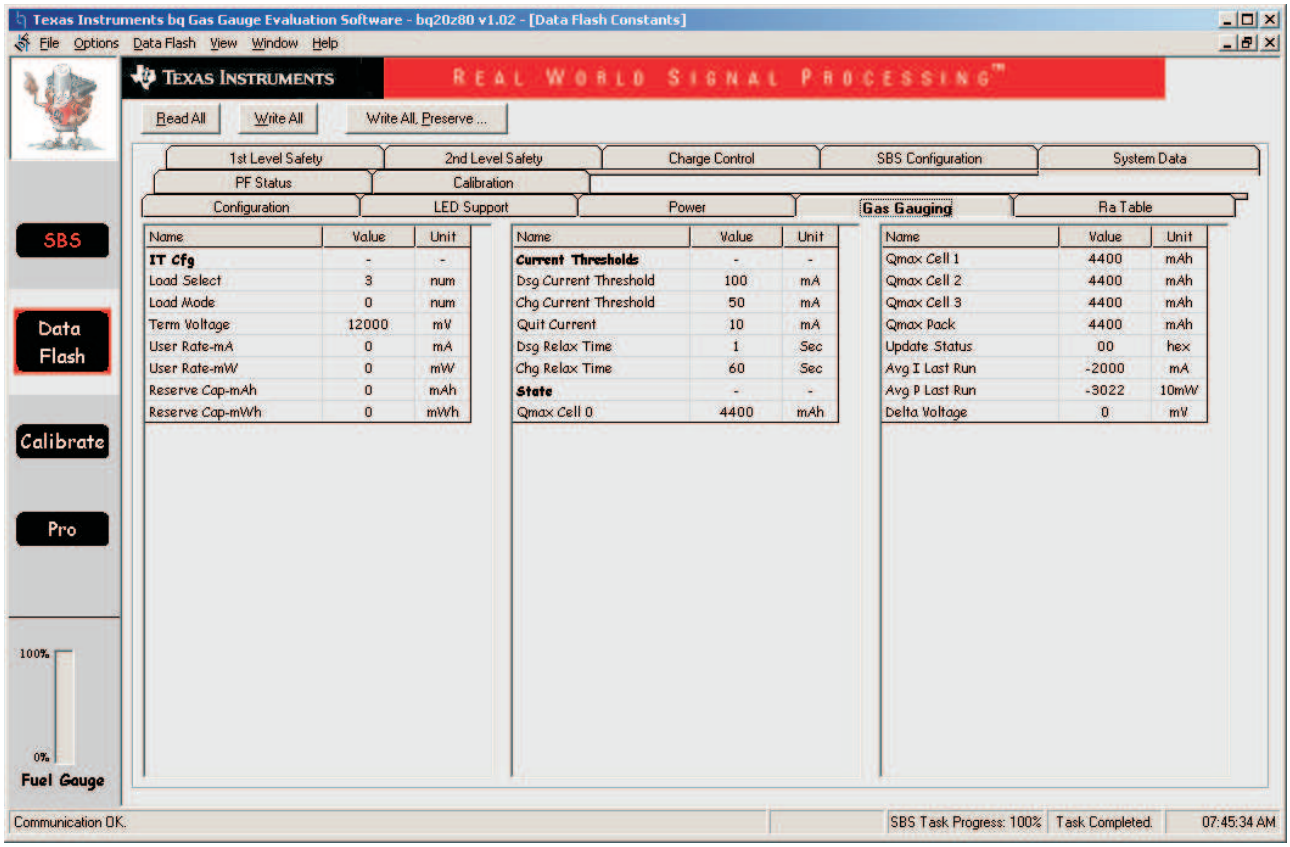
Sleep Voltage Time

While in sleep mode, the bq20z80 wakes up to measure and updates ***Voltage***, ***Cell Voltage(All)*** and ***Temperature*** every *Sleep Voltage Time* in seconds.
Normal Setting: The default for this register is 5 seconds. It is important to note for the settings of this register that it takes time to measure and update the voltage and temperature registers and the bq20z80 is awake and consuming power during this process. The more the bq20z80 is awake, the more it consumes. There is a trade off between voltage detection and power consumption. It is also important to note that the bq29312A (AFE) protection is still active and not affected by sleep.

Sleep Current Time

While in sleep mode, the bq20z80 wakes up to measure and update ***Current*** and ***Average Current*** every *Sleep Current Time* in seconds. Immediately after this update the bq20z80 goes back to sleep unless ***Current*** is above *Sleep Current* during one of these wake up periods. If it is above *Sleep Current*, then the part stays awake until the sleep conditions are met again (See *Sleep Current*).
Normal Setting: The default for this register is 20 seconds. It is important to note for the settings of this register that it takes about 1 second to measure and update the current registers and the bq20z80 is awake and consuming power during this process. The more the bq20z80 is awake, the more it consumes. There is a trade off between current detection and power consumption. It is also important to note that the bq29312A (AFE) protection is still active and not affected by sleep.

2.12 Gas Gauging



IT Config

Load Select

Load Select defines the type of power or current model to be used for Remaining Capacity computation in the Impedance Track™ algorithm. If *Load Mode* = Constant Current then the following options are available:

0 = Average discharge current from previous cycle: There is an internal register that records the average discharge current through each entire discharge cycle. The previous average is stored in this register.

1 = Present average discharge current: This is the average discharge current from the beginning of this discharge cycle till present time.

2 = *Current*: based off of *Current*

3 = *Average Current* (default): based off the *Average Current*

4 = *Design Capacity* / 5: C Rate based off of *Design Capacity* /5 or a C / 5 rate in mA.

5 = *AtRate* (mA): Use whatever current is in *AtRate*

6 = *User_Rate-mA*: Use the value in *User_Rate-mA*. This gives a completely user configurable method.

If *Load Mode* = Constant Power then the following options are available:

0 = Average discharge power from previous cycle: There is an internal register that records the average discharge power through each entire discharge cycle. The previous average is stored in this register.

1 = Present average discharge power: This is the average discharge power from the beginning of this discharge cycle till present time.

2 = *Current* × *Voltage*: based off of *Current* and *Voltage*

3 = *Average Current*×*Voltage* (default): based off the *Average Current* and *Voltage*

4 = *Design Energy* / 5: C Rate based off of *Design Energy* /5 or a C / 5 rate in mA

5 = *AtRate* (10 mW): Use whatever value is in *AtRate*.

6 = *User_Rate-10mW*: Use the value in *User_Rate-mW*. This gives a completely user configurable method.

Normal Setting: The default for this register is 3 which should be acceptable for most applications. This is application dependent.

Load Mode

Load Mode is used to select either the constant current or constant power model for the Impedance Track™ algorithm as used in *Load Select*. (See *Load Select*)

- 0: Constant Current Model
- 1: Constant Power Model

Normal Setting: This is normally set to Current Model but It is application specific. If the application load profile more closely matches a constant power model, then set to 1. This provides a better estimation of remaining run-time, especially close to the end of discharge where current increases to compensate for decreasing battery voltage.

Term Voltage

Term Voltage is used in the Impedance Track™ algorithm to help compute ***Remaining Capacity***. This is the absolute minimum voltage for end of discharge, where the remaining chemical capacity is assumed as zero.
Normal Setting: This register is application dependent. It should be set based on battery cell specifications to prevent damage to the cells or the absolute minimum system input voltage taking into account impedance drop from the PCB traces, FETs, and wires.

User Rate-mAh

User Rate-mAh is only used if *Load Select* is set to 6 and *Load Mode* = 0. If these criteria are met then the current stored in this register is used for the ***Remaining Capacity*** computation in the Impedance Track™ algorithm. This is the only function that uses this register.
Normal Setting: It is unlikely that this register is used. An example application that would require this register is one that has increased predefined current at the end of discharge. With this type of discharge, it is logical to adjust the rate compensation to this period because the IR drop during this end period is effected the moment Term Voltage is reached.

User Rate-10mWh

User Rate-10mWh is only used if Load Select is set to 6 and *Load Mode* = 1. If these criteria are met then the power stored in this register is used for the ***Remaining Capacity*** computation in the Impedance Track™ algorithm. This is the only function that uses this register.
Normal Setting: It is unlikely that this register is used. An example application that would require this register is one that has increased predefined power at the end of discharge. With this application. it is logical to adjust the rate compensation to this period because the IR drop during this end period is effected the moment Term Voltage is reached.

Reserve Cap-mAh

Reserve Cap-mAh determines how much actual remaining capacity exists after reaching SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) = 0% before *Term Voltage* is reached. This register is only used if *Load Mode* is set to 0. There are 2 ways to interpret this register depending on [RESCAP] in *Operation Cfg B*:

- [RESCAP]=0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
- [RESCAP]=1: If set to a 1, then a higher rate of load compensation as defined by *Load Select* is applied to this reserve capacity. (See *Load Select*)

This register is only used if in mA mode (configured by [CAPM] in ***Battery Mode***).
Normal Setting: This register defaults to 0 which disables this function. This is the most common setting for this register. This register is application dependent. This is a specialized function for allowing time for a controlled shutdown after 0% capacity is reached. There are other functions that can serve this purpose like *Remaining Time Alarm* or *Remaining Capacity Alarm*.

Reserve Cap-10mWh

Reserve Cap-10mWh determines how much actual remaining capacity exists after reaching SOC% (***ASOC*** or ***RSOC*** depending on [DMODE] in *Operation Cfg A*) = 0% before *Term Voltage* is reached. This register is only used if *Load Mode* is set to 1. There are 2 ways to interpret this register depending on [RESCAP] in *Operation Cfg B*:

- 0: If set to 0, then a no-load rate of compensation is applied to this reserve capacity
- 1: If set to a 1, then a more normal rate of load compensation as defined by *Load Select* is applied to this reserve capacity. (See *Load Select*)

This register is only used if in mW mode (configured by [CAPM] in ***Battery Mode***).
Normal Setting: This register defaults to 0 which basically disables this function. This is the most common setting for this register. This register is application dependent. This is a specialized function for allowing time for a controlled shutdown after 0% capacity is reached. There are other functions that can serve this purpose like *Remaining Time Alarm* or *Remaining Capacity Alarm*.

Current Thresholds

Dsg Current Threshold

This register is used as a threshold by many functions in the bq20z80 to determine if actual discharge current is flowing into and out of the part. This is independent from [DSG] in ***Battery Status*** which indicates whether the bq20z80 is in discharge mode or charge mode.
Normal Setting: SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. If the bq20z80 is charging, then [DSG] is 0 and any other time (***Current*** less than or equal to 0) the [DSG] flag is equal to 1. Many algorithms in the bq20z80 require more definitive information about whether current is flowing in either the charge or discharge direction. *Dsg Current Threshold* is used for this purpose. The default for this register is 100 mA which should be sufficient for most applications. This threshold should be set low enough to be below any normal application load current but high enough to prevent noise or drift from affecting the measurement.

Chg Current Threshold This register is used as a threshold by many functions in the bq20z80 to determine if actual charge current is flowing into and out of the part. This is independent from [DSG] in Battery Status which indicates whether the bq20z80 is in discharge mode or charge mode. Normal Setting: SBS defines the [DSG] flag in battery status as the method for determining charging or discharging. Basically, if the bq20z80 is charging then [DSG] is 0 and any other time (Current less than or equal to 0) the [DSG] flag is equal to 1. Many algorithms in the bq20z80 require more definitive information about whether current is flowing in either the charge or discharge direction. This is what Dsg Current Threshold is used for. The default for this register is 100 mA which should be sufficient for most applications. This threshold should be set low enough to be below any normal application load current but high enough to prevent noise or drift from affecting the measurement.

Quit Current

The *Quit Current* is used as part of the Impedance Track™ algorithm to determine when the bq20z80 goes into relaxation mode from a current flowing mode in either the charge direction or the discharge direction. Either of the following criteria must be met to enter relaxation mode:

1. ***Current*** is **less than** (–)*Quit Current* and then goes within (±)*Quit Current* for *Dsg Relax Time*.
2. ***Current*** is **greater than***Quit Current* and then goes within (±)*Quit Current* for *Chg Relax Time*.

After about 30 minutes in relaxation mode, the bq20z80 attempts to take accurate OCV readings. An aditional requirement of dV/dt < 4 microvolts/sec (delta voltage over delta time) is required for the bq20z80 to do Qmax updates. These updates are used in the Impedance Track™ algorithms.
Normal Setting: It is critical that the battery voltage be relaxed during OCV readings to get the most accurate results. This current must not be higher than C/20 when attempting to go into relaxation mode; however, it should not be so low as to prevent going into relaxation mode due to noise. This should always be less than *Chg Current Threshold* or *Dsg Current Threshold*.

Dsg Relax Time

The *Dsg Relax Time* is used in the function to determine when to go into relaxation mode. When ***Current*** is **less than** (–)*Quit Current* and then goes within (±)*Quit Current* the *Dsg Relax Time*, timer is initiated. If the current stays within (±)*Quit Current* until the *Dsg Relax Time* timer expires, then the bq20z80 goes into relaxation mode. After about 30 minutes in relaxation mode, the bq20z80 attempts to take accurate OCV readings. An aditional requirement of dV/dt < 4 microvolts/sec (delta voltage over delta time) is required for the bq20z80 to do Qmax updates. These updates are used in the Impedance Track™ algorithms.
Normal Setting: Care should be taken when interpreting discharge descriptions in this document when interpreting the direction and magnitude of the currents because they are in the negative direction. This is application specific.

Chg Relax Time

The *Chg Relax Time* is used in the function to determine when to go into relaxation mode. When ***Current*** is greater than *Quit Current* and then goes within (±)*Quit Current* the *Chg Relax Time*, timer is initiated. If the current stays within (±)*Quit Current* until the Chg Relax Time timer expires, then the bq20z80 goes into relaxation mode. After about 30 minutes in relaxation mode, the bq20z80 attempts to take accurate OCV readings. An aditional requirement of dV/dt < 4 microvolts/sec (delta voltage over delta time) is required for the bq20z80 to do Qmax updates. These updates are used in the Impedance Track™ algorithms.
Normal Setting: This is application specific.

State

Qmax Cell 0

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z80 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data-sheet capacity.

Qmax Cell 1

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z80 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data-sheet capacity.

Qmax Cell 2

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z80 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity.

Qmax Cell 3

This is the Maximum chemical capacity of the battery cell. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated by the bq20z80 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data-sheet capacity.

Qmax Pack

This is the maximum capacity of the entire battery pack. It also corresponds to capacity at very low rate of discharge such as C/20 rate. This value is updated to the lowest chemical capacity of all the cells (*Qmax Cell 0 – Qmax Cell 3*) by the bq20z80 continuously during use to keep capacity measuring as accurate as possible.
Normal Setting: Initially should be set to battery cell data sheet capacity. It is updated with the capacity of the lowest cell during use. This is because the capacity of the entire battery is only as much as the capacity of the lowest cell. When that cell is empty, it does not matter if any other cells have capacity.

Update Status

There are 2 bits in this register that are important.

- Bit 1 (0x02) indicates that the bq20z80 has learned new Qmax parameters and is accurate.
- Bit 2 (0x04) indicates whether Impedance Track™ algorithm is enabled.

The remaining bits are reserved.
Normal Setting: These bits are user configurable; however, bit 1 is also a status flag that can be set by the bq20z80. These bits should never be modified except when creating a golden image file as explained in the application note “Preparing Optimized Default Flash Constants for specific Battery Types” (see SLUA334.pdf). Bit 1 is updated as needed by the bq20z80 and Bit 2 is set with ***Manufacturers Access*** command 0x0021.

Avg I Last Run

The bq20z80 logs the ***Current*** averaged from the beginning to the end of each discharge cycle. It stores this average current from the previous discharge cycle in this register.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z80 when required.

Avg P Last Run

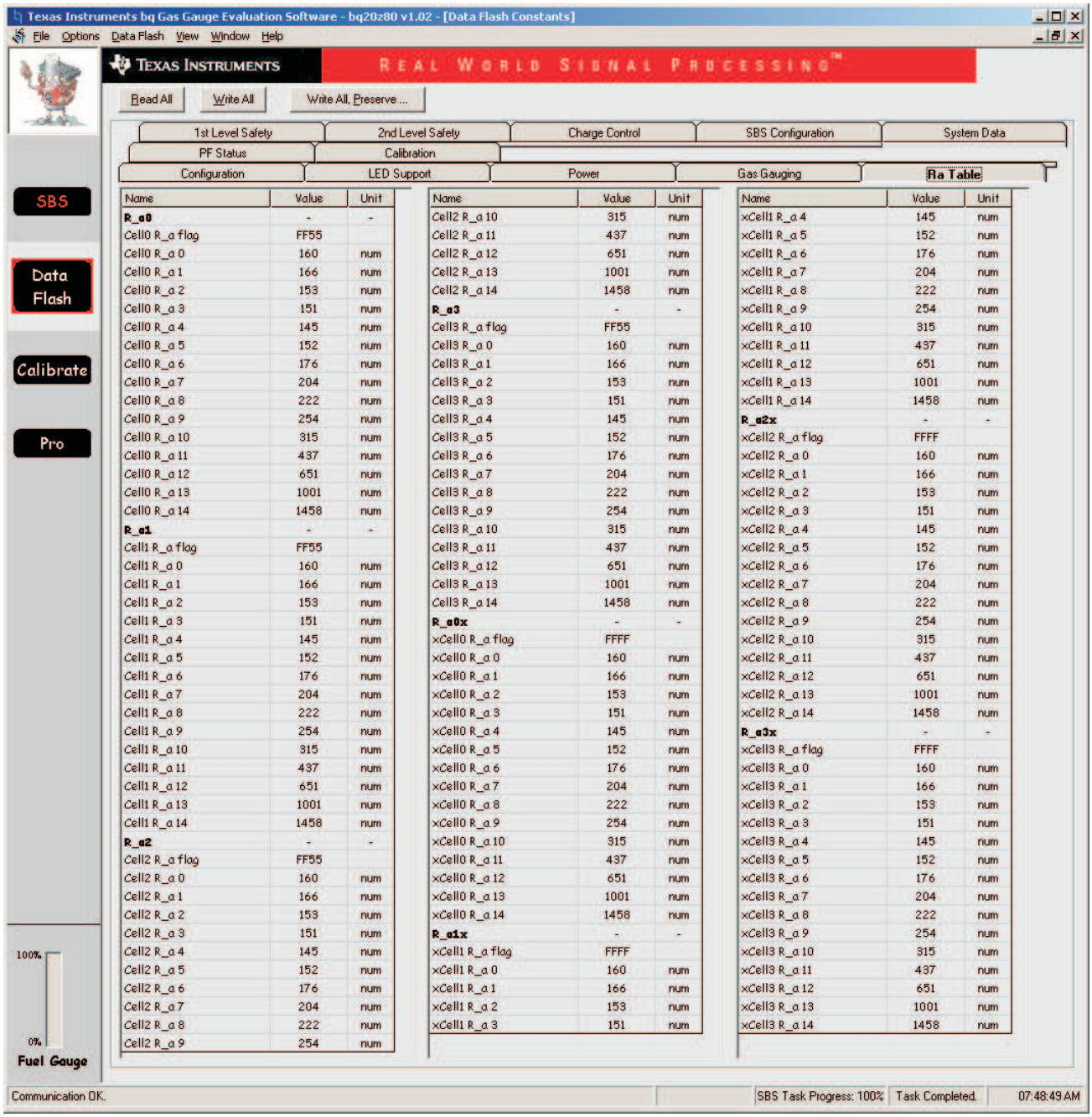
The bq20z80 logs the power averaged from the beginning to the end of each discharge cycle. It stores this average power from the previous discharge cycle in this register. To get a correct average power reading the bq20z80 continuously multiplies ***Current*** times ***Voltage*** to get power. It then logs this data to derive the average power.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z80 when the required.

Delta Voltage

The exact computation of this register is very complex so this description, while not exact, gives the general formula. Delta Voltage is derived as a function average Voltage versus immediate ***Voltage***. The average ***Voltage*** is a localized average over the most recent few seconds. The *Delta Voltage* is the maximum (average ***Voltage***–***Voltage***) at any given time. This register is only updated whenever the algorithm computes a value greater than the previous. Every SOC gridpoint (see *Cell0 R_a0*) causes a sort of reset of this computation. To prevent a 0 value in this register and to give more meaning, the reset algorithm uses a percentage of the previous SOC gridpoint *Delta Voltage* to compute a reset value and then starts the process of computing maximum *Delta Voltage* values again.
Normal Setting: This register should never need to be modified. It is only updated by the bq20z80 when required.

2.13 Ra Table

This data is automatically updated during device operation. No user changes should be made except for reading the values from another pre-learned pack for creating “Golden Image Files”. See application note “Preparation of optimized default flash constants for specific type of battery” (SLUA334). Profiles have format CellN R_a M where N is the cell serial number (from ground up), and M is the number indicating state of charge to which the value corresponds.



Name	Value	Unit
R_a0	-	-
Cell0 R_a flag	FF55	
Cell0 R_a 0	160	num
Cell0 R_a 1	166	num
Cell0 R_a 2	153	num
Cell0 R_a 3	151	num
Cell0 R_a 4	145	num
Cell0 R_a 5	152	num
Cell0 R_a 6	176	num
Cell0 R_a 7	204	num
Cell0 R_a 8	222	num
Cell0 R_a 9	254	num
Cell0 R_a 10	315	num
Cell0 R_a 11	437	num
Cell0 R_a 12	651	num
Cell0 R_a 13	1001	num
Cell0 R_a 14	1458	num
R_a1	-	-
Cell1 R_a flag	FF55	
Cell1 R_a 0	160	num
Cell1 R_a 1	166	num
Cell1 R_a 2	153	num
Cell1 R_a 3	151	num
Cell1 R_a 4	145	num
Cell1 R_a 5	152	num
Cell1 R_a 6	176	num
Cell1 R_a 7	204	num
Cell1 R_a 8	222	num
Cell1 R_a 9	254	num
Cell1 R_a 10	315	num
Cell1 R_a 11	437	num
Cell1 R_a 12	651	num
Cell1 R_a 13	1001	num
Cell1 R_a 14	1458	num
R_a2	-	-
Cell2 R_a flag	FF55	
Cell2 R_a 0	160	num
Cell2 R_a 1	166	num
Cell2 R_a 2	153	num
Cell2 R_a 3	151	num
Cell2 R_a 4	145	num
Cell2 R_a 5	152	num
Cell2 R_a 6	176	num
Cell2 R_a 7	204	num
Cell2 R_a 8	222	num
Cell2 R_a 9	254	num

Name	Value	Unit
Cell2 R_a 10	315	num
Cell2 R_a 11	437	num
Cell2 R_a 12	651	num
Cell2 R_a 13	1001	num
Cell2 R_a 14	1458	num
R_a3	-	-
Cell3 R_a flag	FF55	
Cell3 R_a 0	160	num
Cell3 R_a 1	166	num
Cell3 R_a 2	153	num
Cell3 R_a 3	151	num
Cell3 R_a 4	145	num
Cell3 R_a 5	152	num
Cell3 R_a 6	176	num
Cell3 R_a 7	204	num
Cell3 R_a 8	222	num
Cell3 R_a 9	254	num
Cell3 R_a 10	315	num
Cell3 R_a 11	437	num
Cell3 R_a 12	651	num
Cell3 R_a 13	1001	num
Cell3 R_a 14	1458	num
R_a0x	-	-
xCell0 R_a flag	FFFF	
xCell0 R_a 0	160	num
xCell0 R_a 1	166	num
xCell0 R_a 2	153	num
xCell0 R_a 3	151	num
xCell0 R_a 4	145	num
xCell0 R_a 5	152	num
xCell0 R_a 6	176	num
xCell0 R_a 7	204	num
xCell0 R_a 8	222	num
xCell0 R_a 9	254	num
xCell0 R_a 10	315	num
xCell0 R_a 11	437	num
xCell0 R_a 12	651	num
xCell0 R_a 13	1001	num
xCell0 R_a 14	1458	num
R_a1x	-	-
xCell1 R_a flag	FFFF	
xCell1 R_a 0	160	num
xCell1 R_a 1	166	num
xCell1 R_a 2	153	num
xCell1 R_a 3	151	num

Name	Value	Unit
xCell1 R_a 4	145	num
xCell1 R_a 5	152	num
xCell1 R_a 6	176	num
xCell1 R_a 7	204	num
xCell1 R_a 8	222	num
xCell1 R_a 9	254	num
xCell1 R_a 10	315	num
xCell1 R_a 11	437	num
xCell1 R_a 12	651	num
xCell1 R_a 13	1001	num
xCell1 R_a 14	1458	num
R_a2x	-	-
xCell2 R_a flag	FFFF	
xCell2 R_a 0	160	num
xCell2 R_a 1	166	num
xCell2 R_a 2	153	num
xCell2 R_a 3	151	num
xCell2 R_a 4	145	num
xCell2 R_a 5	152	num
xCell2 R_a 6	176	num
xCell2 R_a 7	204	num
xCell2 R_a 8	222	num
xCell2 R_a 9	254	num
xCell2 R_a 10	315	num
xCell2 R_a 11	437	num
xCell2 R_a 12	651	num
xCell2 R_a 13	1001	num
xCell2 R_a 14	1458	num
R_a3x	-	-
xCell3 R_a flag	FFFF	
xCell3 R_a 0	160	num
xCell3 R_a 1	166	num
xCell3 R_a 2	153	num
xCell3 R_a 3	151	num
xCell3 R_a 4	145	num
xCell3 R_a 5	152	num
xCell3 R_a 6	176	num
xCell3 R_a 7	204	num
xCell3 R_a 8	222	num
xCell3 R_a 9	254	num
xCell3 R_a 10	315	num
xCell3 R_a 11	437	num
xCell3 R_a 12	651	num
xCell3 R_a 13	1001	num
xCell3 R_a 14	1458	num

Cell0 R_a flag,
Cell1 R_a flag,
Cell2 R_a flag,
Cell3 R_a flag,
xCell0 R_a flag,
xCell1 R_a flag,
xCell2 R_a flag,
xCell3 R_a flag

Each subclass (R_a0-R_a3 and R_a0x-R_a3x) in the Ra Table class is a separate profile of resistance values normalized at 0 degrees for each of the cells in a design (cells 0–3) There are 2 profiles for each cell. They are denoted by the x or absence of the x at the end of the subclass Title:
R_a0 or **R_a0x** for cell 0
R_a1 or **R_a1x** for cell 1
R_a2 or **R_a2x** for cell 2
R_a3 or **R_a3x** for cell 3
The purpose for 2 profiles for each series cell is to ensure that at any given time there is at least one profile is enabled and being used while attempts can be made to update the alternate profile without interference. Having 2 profiles also helps reduce stress on the Flash Memory. At the beginning of each of the 8 subclasses (profiles) is a flag called *CellM R_a flag* or *xCellM R_a flag* where "M" is the cell number (0-3). This flag is a status flag indicates the validity of the table data associated with this flag and whether this particular table is enabled/disabled. There are 2 bytes in each flag:

1. The LSB (least significant byte) indicates whether the table is currently enabled or disabled. It has the following options:
   a. 0x00 : means the table has had a resistance update in the past; however, it is not the currently enabled table for this cell. (the alternate table for the indicated cell must be enabled at this time)
   b. 0xff: This means that the values in this table are default values. This table resistance values have never been updated, and this table is not the currently enabled table for this cell. (the alternate table for the indicated
   c. 0x55: This means that this table is enabled for the indicated cell (the alternate table must be disabled at this time.) cell must be enabled at this time)
2. The MSB (Most significant byte) indicates that status of the data in this particular table. The possible values for this byte are:
   a. 0x00: The data associated with this flag has had a resistance update and the *QMax Pack* has been updated
   b. 0x05: The resistance data associated with this flag has been updated and the pack is no longer discharging (this is prior to a *Qmax Pack* update).
   c. 0x55: The resistance data associated with this flag has been updated and the pack is still discharging (Qmax update attempt not possible until discharging stops).
   d. 0xff: The resistance data associated with this flag is all default data.

This data is used by the bq20z80 to determine which tables need updating and which tables are being used for the Impedance Track™ algorithm.
Normal Setting: This data is used by the bq20z80 Impedance Track™ algorithm. The only reason this data is displayed and accessible is to give the user the ability to update the resistance data on golden image files. This description of the *xCellM R_a flags* are intended for information purposes only. It is not intended to give a detailed functional description for the bq20z80 resistance algorithms.
Cell0 R_a0 – Cell0 R_a14,
xCell0 R_a0 – xCell0 R_a14,
Cell1 R_a0 – Cell1 R_a14,
xCell1 R_a0 – xCell1 R_a14,
Cell2 R_a0 – Cell2 R_a14,
xCell2 R_a0 – xCell2 R_a14,
Cell3 R_a0 – Cell3 R_a14,
xCell3 R_a0 – xCell3 R_a14,
There are 15 values for each R_a subclass in the **Ra Table** class. Each of these values represent a resistance value normalized at 0°C for the associated *Qmax Pack* based SOC gridpoint as found by the following rules:

For *CellN R_aM* where:

1. if $0 \le M \le 8$: The data is the resistance normalized at 0° for: SOC = 100% – (M × 10%)
2. if $9 \le M \le 14$: The data is the resistance normalized at 0 degrees for: SOC = 100% – [80% + (M – 8) × 3.3%]

This gives a profile of resistance throughout the entire SOC profile of the battery cells concentrating more on the values closer to 0%.

Normal Setting: SOC as stated in this description is based on *Qmax Pack*. It is not derived as a function of RSOC or ASOC. These resistance profiles are used by the bq20z80 for the Impedance Track™ algorithm. The only reason this data is displayed and accessible is to give the user the ability to update the resistance data on golden image files. This resistance profile description is for information purposes only. It is not intended to give a detailed functional description for the bq20z80 resistance algorithms. It is important to note that this data is in units of milliohms and is normalized to 0°C. Useful observations to note with this data throughout the application development cycle:

1. Watch for negative values in the **Ra Table** class. There should never be negative numbers in profiles anywhere in this class.
2. Watch for smooth consistent transitions from one profile gridpoint value to the next throughout each profile. As the bq20z80 does resistance profile updates these values should be roughly consistent from one learned update to another without huge jumps in consecutive gridpoints.

Feature Set Comparison Between bq2084 and bq20z80

Garry Elder *PMP Portable Power*

ABSTRACT

The bq20z80 differs from the bq2084 in several areas, although all bq2084 features are available in the bq20z80. Both devices support SBS1.1 with SMBus communications, but the bq20z80 has many extended SBS commands to enable additional features. The array of bq2084 safety features is expanded in the bq20z80, with a wider range of configuration options. The bq20z80 offers greater flexibility in use and configuration of the features. Each feature setup is very similar, making the device easier to understand and use. An overview of the operation of each device can be seen in the diagrams at the end of this document. Although the gas-gauge hardware is different, the pinout is the same except for an additional thermistor input (TS2).

3.1 Hardware Platform

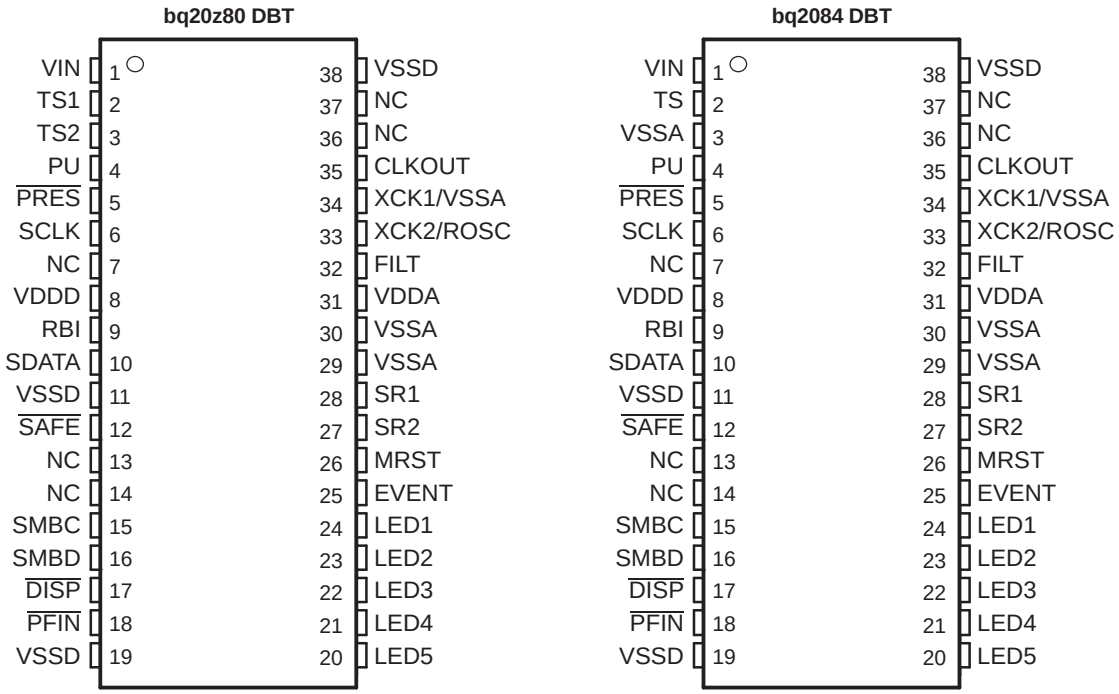
The bq20z80 architecture is based on the bq8024, and uses the bq29312 Analog Front End (AFE) to complete the gas-gauge first-level protection chip set. The differences in the bq8020/bq29312 platform used by the bq2084 are shown in Table 9.

Table 9. BMU Hardware Differences

DEVICE	POR CIRCUIT				XTRA INTERNAL CAP	FLASH MEMORY		RAM
	SLOW	FAST	LOW VDD	DEGLITCH		PROGRAM	DATA	
bq8020	x	x	x			16kx22	1kx8	768x8
bq8024 (1)	x			x	x	24kx22	2kx8	1kx8

(1) The bq8024 platform require a 100 kΩ resistor from MRST to VSSA, and a 0.1 µF capacitor from VDDA to MRST to align the rise of VDDA and the release of MRST.

The pinout is identical except for the optional additional thermistor (Pin 3).



NC − No internal connection

Figure 7. Pinouts for the bq20z80DBT and bq2084DBT

Because the bq20z80 and bq2084 use the same bq29312 AFE, the only difference in the schematic and layout for these two devices is the optional use of the second thermistor. If the TS2 pin (pin 3) is not used, but is grounded, as in a bq2084 schematic, this is no concern. Therefore, testing can be performed on current bq2084-based PCBs and packs simply by replacing the bq2084 with a bq20z80.

3.2 CEDV vs ImpedanceTrack™

What is the Compensated End of Discharge Voltage (CEDV) Algorithm?

The CEDV algorithm mathematically models cell voltage (open-circuit voltage, OCV) as a function of battery state-of-charge (SOC), temperature, and current. It also mathematically models impedance (Z) as a function of SOC and temperature, with a total of seven parameters in the equation.

$$CEDV = OCV - I \times Z$$

This battery-voltage model is used to calibrate full-charge capacity (FCC), and a compensated battery voltage is used for end-of-discharge alarms (Battery Low%, Fully Discharged), and cutoff.

What is ImpedanceTrack?

The ImpedanceTrack (IT) algorithm performs real-time measurements and calculations before recording key battery-chemistry parameters into the on-chip data flash memory.

$OCV = f(SOC)$, $Z = f(SOC, Q_{MAX})$ where Q_{MAX} = battery chemical capacity

The IT algorithm dynamically updates the data flash as it fully characterizes the parameters of each cell, and generates a unique set of data for each battery pack. This data is used to predict how each battery behaves electronically under given current and temperature stimuli by continually updating and reporting *FullChargeCapacity( )*, *RelativeStateofCharge( )*, and *TimeToEmpty( )*.

Algorithm Summary

- CEDV uses a mathematical model to correlate RSOC and voltage near the end-of-discharge state
  - Relies on battery characterization to establish the model
  - Model requires an additional feature to avoid severe inaccuracy as battery ages
  - Requires a full discharge for a single-point FCC update
- ImpedanceTrack measures and records battery-chemistry data, from full to empty states
  - Uses battery data to predict battery response to electronic and thermal stimuli
  - Battery aging of Q_{MAX} and impedance is captured
  - Usable full and available capacity is continually updated

3.2.47.5 Learning Battery Chemical Capacity (Q_{max}) There is a correlation between OCV and SOC (or Depth of Discharge, DOD) that can be understood, and used to model the cell or battery.

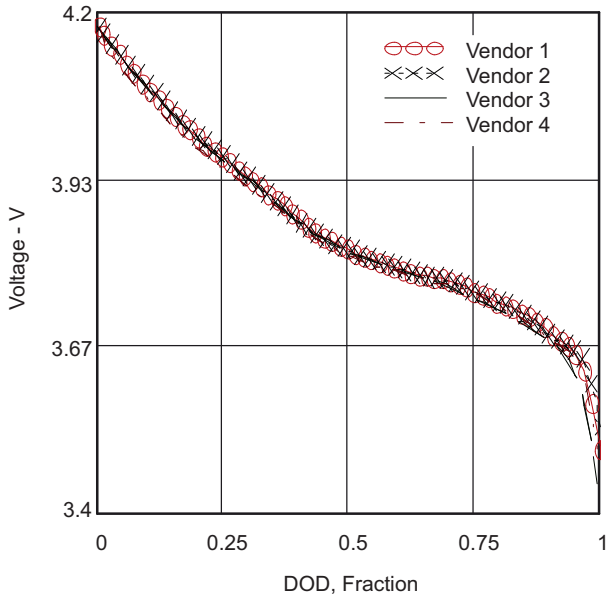


Figure 8. Relationship Between Cell Voltage and DOD for 4 Different Cell Suppliers

Notice the lack of variation between the different cell vendors. This demonstrates that there is no need to uniquely configure the ImpedanceTrack algorithm for different cell suppliers.

The correlation is only valid for the current battery chemistry materials used today. Advances in chemical technology by the use of new or modified materials are yet to be evaluated.

To actually learn a new Q_{MAX}, two OCV measurements are needed, separated by a change in capacity where a valid OCV measurement requires the battery to be at rest. "Rest" in this case is defined at a dv/dt of 0.1 µV/s, which typically takes a maximum time of 1000s.

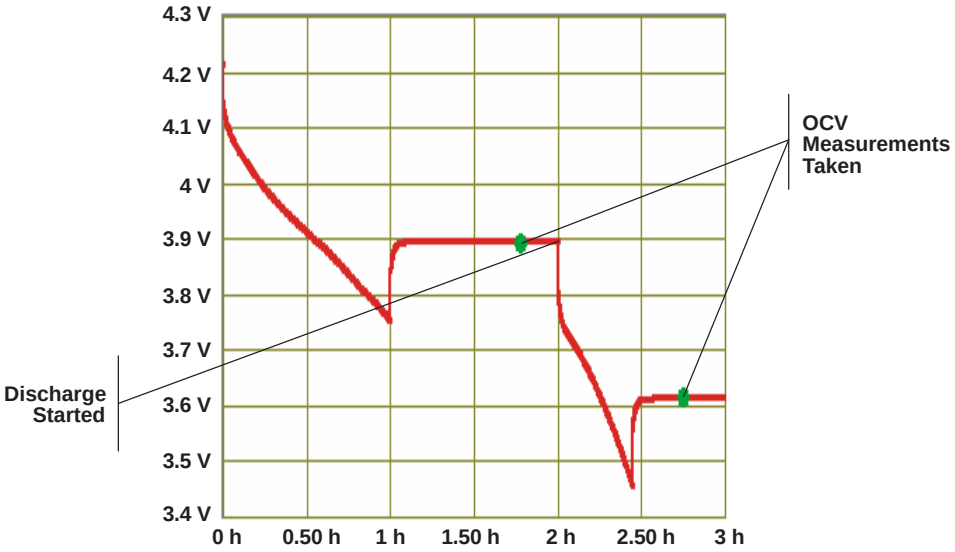


Figure 9. Q_{MAX} Learning Opportunity

Because the voltage profile of the battery correlates to Z and SOC, the aging and self-discharge of a battery are factored into the model. Therefore, no additional factors are needed to compensate for these effects.

3.2.47.6 Impedance Measurement and FCC Calculation The ImpedanceTrack algorithm calculates real-time DC impedance by measuring the voltage drop from the OCV measurement and dividing it by the current. This is sampled at 15 points between full and empty. As this occurs through the life of the battery, the impedance increase due to age is physically measured.

The ImpedanceTrack algorithm uses impedance and OCV data to predict the usable capacity under a given load and temperature using a root-finding approach to converge on usable available capacity.

Both constant current and constant power are applicable and as equally accurate as FCC tracks real time with current and temperature.

3.2.47.7 Pack Development With ImpedanceTrack™ No data collection for each pack design is required as all battery parameters are learned real time by the gas gauge through out the normal operational lifetime of the battery. If a full initialization is desired then it is automatically performed during one discharge cycle and that data can be copied to all packs.

No full discharge is required for capacity learning. Only a charge or discharge for 1000s is necessary for impedance scaling for cell to cell variations.

RemainingStateOfCharge( ) (RSOC) is initialized whenever a rest state is detected which does occur on exit from Ship mode (on power up).

3.2.47.8 Algorithm Comparison Summary

- New battery pack
  - *Cell-to-cell variation effect:* CEDVs are adapted for specific cell impedances, but cell-to-cell variation in impedance of about 15% can cause up to 2% error in EDV2 voltage estimation for Battery Low% (typically set at 7%). This can result in a 2% error in FCC. ImpedanceTrack does not exhibit this error because impedance is measured at each cell in real time.
  - *Transient effects:* In a variable-load environment, after a current change, the cell voltage does not immediately change. However, the CEDV method assumes that voltage strictly correlates with given current and SOC. In a case where current increased immediately before reaching estimated the EDV2 voltage, learned FCC will be overestimated by up to 1%. If the current decreases under similar conditions, learned FCC will be underestimated.
  - *More flexibility in compensating for temperature effects:* IT uses exponential functions for describing impedance-temperature dependence—these are more flexible than CEDV functions. In the IT algorithm, the *false learn* scenario is not possible, but is possible with CEDVs, where unusually low FCC would be learned at low temperature (therefore low temperature learn was disabled) or at a high rate. This low FCC would then be used for all subsequent cycles even at a lower rate, therefore not allowing use of the full capacity of the battery. IT does not have this problem, because FCC is always calculated using model parameters that adapt to present rate and temperature.
  - *Cell-based CEDVs:* If the cell-based CEDV method is used, the lowest cell defines the capacity of the pack. However, this is not exact, because a higher voltage cell keeps the pack operational longer. IT uses the sum of all cell voltages to estimate the whole pack voltage, so this problem is avoided.
  - *Self-discharge estimation:* During periods of inactivity, self-discharge is estimated using a simple, and hence inexact, formula in the CEDV method. IT measures self discharge directly based on OCV. Therefore, SOC information remains correct regardless of the period of inactivity.
- Aged battery pack
  - *Capacity Learning:* The CEDV method requires a full charge-discharge cycle to update the FCC value. IT only requires a 5-minute discharge to update the impedance information, and a 25% discharge (not necessary from fully charged state) to update the chemical-capacity information. Because chemical capacity changes very slowly (typically 3% in 100 cycles), resistance updates are sufficient to keep errors below 1% even without regular chemical-capacity updates. This allows accurate capacity estimation for devices that are never fully discharged, such as uninterruptable power sources (UPS) and other backup systems.

    Because of cell-impedance changes, the EDV2 (7% SOC) voltage calculation used to update FCC in the CEDV method becomes inaccurate with age, since CEDV parameters assume a new-cell impedance value. Cycle-number correction improves this estimate, but because aging depends not only on the number of cycles, but also on inactivity time, temperature, and usage pattern, the possibility remains for a worst-case error of approximately 10% after 300 cycles. Because impedance information is updated by continuous real-time measurements on each cell, IT does not have this problem.
  - *Termination voltage:* This is typically defined as 3 V/cell to prevent cell degradation. This voltage is typically much higher compared to minimal acceptable system-side dc/dc converter voltages (typically 2.2 V/cell). The CEDV method has no way of determining the actual chemical state-of-charge of the cells, therefore a fixed termination voltage is the only way to prevent excessive discharge. However, true end-of-chemical-capacity voltage depends on the rate of discharge and age ($V = V_0 – IR$, and R increase with age), and can move from 2.7 V for new cells down to 2 V for aged cells at the same rate. The IT method has information about the actual chemical capacity of the cell, and reports a 0 SOC at the end of chemical capacity regardless of the voltage. This allows setting the termination voltage to the converter voltage, preventing premature fixed-voltage termination when chemical capacity is still left. This increases run-time by up to 20%.

3.3 ManufacturerAccess( ) Features

The bq2084 has an array of features that use the *SBS ManufacturerAccess( )* command. There are differences between the two devices, as shown in Table 10.

Table 10. ManufacturerAccess( ) Commands

NAME	bq2084	bq20z80	DESCRIPTION
Part Number	0x0001	0x0001	Returns the IC part number
Firmware Version	0x0002	0x0002	Returns Firmware Version
EDV Level	0x0003	NA	Returns the pending CEDV
Hardware Version	NA	0x0003	Returns hardware version
Manufacturer Status	0x0004	0x0006(1)	Returns detailed summary of the battery status
DF_Checksum	NA	0x0004	Instructs the gas gauge to generate a static DF checksum
Qusable Update	NA	0x0005	Instructs the gas gauge to update Q_{USABLE}
Ship	0x0005	0x0010	Causes the bq29312 to enter ship mode
Sleep	NA	0x0011	Causes the bq20z80 to enter sleep mode
Seal	0x062b	0x0030	Instructs the gas gauge to restrict access to that defined by the SBS standard
Calibration Mode	0x0653	0x0040	Instructs the gas gauge to enter calibration mode
Reset	NA	0x0041	Causes the gas gauge to be fully reset
Sleep	NA	0x0011	Instructs the gas gauge to enter Sleep Mode
IT_Enable	NA	0x0021	Instructs the gas gauge to enable Impedance Track™
SAFE_Activation	NA	0x0030	Instructs the gas gauge to drive the $\overline{SAFE}$ output low
SAFE_Clear	NA	0x0031	Instructs the gas gauge to drive the $\overline{SAFE}$ output high
LEDs ON	NA	0x0032	Causes the gas gauge to turn ON all LED's
LEDs OFF	NA	0x0033	Causes the gas gauge to turn OFF all LED's
Display ON	NA	0x0034	Causes the gas gauge to turn on the Display (simulates $\overline{DISP}$ transition)
PFClear	0x2673(2) 0x1712(2)	0x2673(2) 0x1712(2)	Instructs the gas gauge to clear Permanent Failure Mode

(1) Optional configurations available in the bq20z80 (bq2084 is fixed).
(2) Default

Additional security features exist via the *SBS.ManufacturereAccess( )* commands, but are beyond the scope of this report.

Manufacture Status: 0x0004 (bq2084)

This 16 bit word summarizes the battery status, and is formatted differently in the bq20z80 depending on the *DF.OperationConfiguration*, *MAC1* and *MAC2* bits. The bq2084 format is the same as bq20z80 *DF.OperationConfiguration*, *MAC1* = *MAC2* = 0, and is detailed below.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Blt 9	Bit 8
FET1	FET0	PF1	PF0	STATE3	STATE2	STATE1	STATE0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Blt 1	Bit 0
0	0	0	0	1	0	1	0

FET1, FET0

Indicates the state of the charge and discharge FETs

0, 0 **Both charge and discharge FETs are on.**

0, 1 **Charge FET is off, discharge FET is on.**

1, 0 **Both charge and discharge FETs are off.**

1, 1 **Charge FET is on, discharge FET is off.**

PF1, PF0

Indicates the cause of a permanent failure when a permanent failure is indicated by STATE3-STATE0

0, 0 **Fuse is blown**

0, 1 **Cell imbalance failure**

1, 0 **Safety voltage failure**

1, 1 **FET failure**

STATE3, STATE2, STATE1, STATE0

Indicates battery state as defined in the State and Status bit Summary.

Table 11. STATE Code for Manufacture Status

bq2084 STATE	STATE CODE (hex)	CORRESPONDING bq20z80 FLAG
wakeup	0	SBS.OperationStsatus( ) WAKE
precharge	3	SBS.ChargingStatus( ) PCHG
chargesusp	4	SBS.ChargingStatus( ) CHGSUSP
terminatecharge	7	
normalcharge	5	SBS.ChargingStatus( ) FCHG
provisionalcharge	1	SBS.ChargignStatus( ) XCHG
normaldischarge	1	SBS.OperationStatus( ) DSG
depleted	0	SBS.OperationStatus( ) XDSG or XDSGV or XDSGI or XDSGT
depleted_ac		
overheatdischarge		
overheatcharge		
battfail_overcharge		
battfail_lowtemp		
battfail_chargeterminate	8	SBS.ChargingStatus( ) OCHGI or OCHGV
battfail_afe_chg	c	SBS.SafetyStatus( ) SCC
battfail_afe_dsg	c	SBS.SafetyStatus( ) AOCD or SCD
battfail_chg	a	SBS.SafetyStatus( ) OCC or OCC2
battfail_dsg	a	SBS.SafetyStatus( ) OCD or OCD2
removed	f	SBS.OperationStatus( ) PRES
sleep	d	Communication causes exit of Sleep
permanent_failure	9	SBS.SafetyStatus( ) PF

3.4 Extended SBS Commands

The bq20z80 has a selection of Extended SBS Commands in addition to the SBS specified commands. The bq2084 only has one extended SBS command, *SBS.AFEData( )* [0x47].

The extended commands available in the bq20z80, which are primarily available in unsealed mode only, include

- *GetRAMDataBlock( )* [0x43] and *SetRAMBlockNumber( )* [0x44] to enable RAM dumps
- *AFEData( )* [0x45] to retrieve the complete AFE memory map
- *FETControl( )* [0x46] for improved testability at PCB and system level
- *StateOfHealth( )* [0x47] reports the state of health of the battery
- *SafetyAlert( )* [0x50] and *SafetyStatus( )* [0x51] indicate the current status of the primary (first level) safety features
- *PFAlert( )* [0x52] and *PFStatus( )* [0x53] indicate the current status of the secondary (second level) safety features
- *OperationStatus( )* [0x54] and *ChargingStatus( )* [0x55] report the current status of normal operations
- *ResetData( )* [0x57] and *WatchdogResetData( )* [0x58] report the number and type of resets in the life of the bq20z80
- *PackVoltage( )* [0x59] returns the voltage at the PACK pin of the bq29312
- *ManufacturerInfo( )* [0x70] provides scratchpad storage space for the pack manufacturer
- *DataFlashClass( )* [0x77] and *DataFlashSubclass( )* provides access to the integrated data flash space

3.5 LifeTime Data Logging Features

The bq20z80 offers a Lifetime data logging array of where maximum and minimum measurements are stored for warranty and analysis purposes.

The data available includes:

Lifetime Maximum Temperature
Lifetime Minimum Temperature
Lifetime Average Temperature
Lifetime Maximum Discharge Current
Lifetime Maximum Charge Current
Lifetime Maximum Battery Voltage
Lifetime Minimum Battery Voltage
Lifetime Maximum Cell Voltage
Lifetime Minimum Cell Voltage
Lifetime Maximum Power,
Lifetime Maximum Average Power

3.6 Primary (1st Level) Safety Features

The bq2084 and bq20z80 have a similar array of safety features using Voltage, Temperature, Current and system-level data to ensure that the battery remains safe during normal operation.

Table 12. Primary Safety Features

SAFETY FEATURE	bq2084		bq20z80	
	SET	RECOVERY	SET	RECOVERY
VOLTAGE BASED				
Cell Over Voltage	$VCELL_{ANY}$( ) ≥ DF.CellOverVoltage for 0 to 1s or 1 to 2s if VOD is set	$VCELL_{ALL}$( ) < DF.CellOver VoltageReset for 0 to 1s	$VCELL_{ANY}$( ) ≥ DF.CellOverVoltage(1) for DF.CellOverVoltageTime	$VCELL_{ALL}$( ) ≤ DF.CellOverVoltageReset for 0 to 1s
Cell Under Voltage	$VCELL_{ANY}$( ) ≤ DF.CellUnderVoltage for 0 to 1s or 1 to 2s if VOD is set	$VCELL_{ALL}$( ) < DF.CellUnder VoltageReset for 0 to 1s	$VCELL_{ANY}$( ) ≤ DF.CellUnderVoltage for DF.CellUnderVoltageTime	$VCELL_{ALL}$( ) ≥ DF.CellUnderVoltageReset for 0 to 1s
Pack Over Voltage	N/A	N/A	Voltage( ) ≥ DF.PackOverVoltage for DF.PackOverVoltageTime	Voltage( ) ≤ DF.PackOverVoltage Reset for 0 to 1s
Pack Under Voltage	N/A	N/A	Voltage( ) ≤ DF.PackUnderVoltage for DF.PackUnderVoltageTime	Voltage( ) ≥ DF.PackUnderVoltage Reset for 0 to 1s
CURRENT BASED				
DSG Over Current	Current( ) ≥ DF.OverCurrentDSG for DF.OverCurrentDSGTime	AverageCurrent( ) = 0 for 0 to 1s OR Battery Removal	Current( ) ≥ DF.OverCurrentDSG for DF.OverCurrentDSGTime	AverageCurrent( ) ≤ DF.OverCurrentDSGRecovery for DF.CurrentRecoveryTime OR Battery Removal
CHG Over Current	Current( ) ≥ DF.OverCurrentCHG for DF.OverCurrentCHGTime	AverageCurrent( ) = 0 for 0 to 1s OR Battery Removal	Current( ) ≥ DF.OverCurrentCHG for DF.OverCurrentCHGTime	AverageCurrent( ) ≤ DF.OverCurrentCHGRecovery OR DF.CurrentRecoveryTime OR Battery Removal
2nd Tier DSG OC	N/A	N/A	Current( ) ≥ DF.2ndTierOverCurrentDSG for DF.2ndTierOverCurrentDSGTime	AverageCurrent( ) ≤ DF.OverCurrentDSGRecovery OR DF.CurrentRecoveryTime OR Battery Removal
2nd Tier CHG OC	N/A	N/A	Current( ) ≥ DF.2ndTierOverCurrentCHG for DF.2ndTierOverCurrentCHGTime	AverageCurrent( ) ≤ DF.OverCurrentCHGRecovery OR DF.CurrentRecoveryTime OR Battery Removal
3rd Tier DSG OC	V_{RSNS} ≥ AFE.Overload setting for AFE.OLDelay	AverageCurrent( ) < DF.ClearFailCurrent for DF.FaultResetTime OR Battery Removal	V_{RSNS} ≥ AFE.Overload setting for AFE.OLDelay	AverageCurrent( ) ≤ DF.OverCurrentDSGRecovery OR DF.CurrentRecoveryTime OR Battery Removal
Short Circuit in Charge	V_{RSNS} ≥ AFE.SCC setting for AFE.SCCDelay	AverageCurrent( ) < DF.ClearFailCurrent for DF.FaultResetTime OR Battery Removal	V_{RSNS} ≥ AFE.SCC setting for AFE.SCCDelay	AverageCurrent( ) ≤ DF.OverCurrentDSGRecovery OR DF.CurrentRecoveryTime OR Battery Removal
Short Circuit in Discharge	V_{RSNS} ≥ AFE.SCD setting for AFE.SCDDelay	AverageCurrent( ) < DF.ClearFailCurrent for DF.FaultResetTime OR Battery Removal	V_{RSNS} ≥ AFE.SCD setting for AFE.SCDDelay	AverageCurrent( ) ≤ DF.OverCurrentCHGRecovery OR DF.CurrentRecoveryTime OR Battery Removal
TEMPERATURE BASED				
DSG Over Temperature	Temperature( ) ≥ DF.OverTempDSG for DF.OverTempDSGTime	Temperature( ) ≤ DF.OverTempDSGReset for 0 to 1s	Temperature( ) ≥ DF.OverTempDSG for DF.OverTempDSGTime	Temperature( ) ≤ DF.OverTempDSGRecovery for 0 to 1s
CHG Over Temperature	Temperature( ) ≥ DF.OverTempCHG for DF.OverTempCHGTime	Temperature( ) ≤ DF.OverTempCHGReset for 0 to 1s	Temperature( ) ≥ DF.OverTempCHG for DF.OverTempCHGTime	Temperature( ) ≤ DF.OverTempCHGRecovery for 0 to 1s
SYSTEM BASED				
AFE Watchdog	CLKOUT to WDI out of range	CLKOUT to WDI in range	CLKOUT to WDI out of range	CLKOUT to WDI in range *and* AFE Verification passes
Host Watchdog	N/A	N/A	SMBus communications not detected for DF.HostWatchdogTime	SMBus communication detected

(1) The Cell Over Voltage threshold can be programmed to be compensated based on temperature.

3.7 Secondary (2nd Level) Safety Features

Table 13. Secondary Safety Features

SAFETY FEATURE	bq2084	bq20z80
External Input (PFIN)	PFIN input low for DF.PFINTime	PFIN input low for DF.PFINTime
Safety Over Voltage	Voltage( ) ≥ DF.SafetyOverVoltage for 0 to 1s or 1 to 2s if VOD is set	Voltage( ) ≥ DF.SafetyOverVoltage for DF.SafetyOverVoltageTime
Safety Over Current CHG	N/A	Current( ) ≥ DF.SafetyOverCurrentCHG for DF.SafetyOverCurrentCHGTime
Safety Over Current DSG	N/A	Current( ) ≥ DF.SafetyOverCurrentDSG for DF.SafetyOverCurrentDSGTime
Safety Over Temperature CHG	Temperature( ) ≥ DF.SafetyOverTemperatureCHG	Temperature( ) ≥ DF.SafetyOverTemperatureCHG for DF.SafetyOverTemperatureCHGTime
Safety Over Temperature DSG	Current( ) ≥ DF.SafetyOverTemperatureDSG	Current( ) ≥ DF.SafetyOverTemperatureDSG for DF.SafetyOverTemperatureDSGTime
Cell Imbalance	$VCELL_{MAX}$( ) – $VCELL_{MIN}$( ) ≥ DF.CellImbalanceThreshold for DF.CellImablanceTime	$VCELL_{MAX}$( ) – $VCELL_{MIN}$( ) ≥ DF.CellImbalanceThreshold for DF.CellImablanceTim
Charge FET Failure	CHG FET commanded OFF *and* Current( ) ≥ DF.FETFailCHGThreshold for DF>FETFailTime	CHG *and* ZVCHG FET commanded OFF *and* Current( ) ≥ DF.FETFailThreshold for DF>FETFailTime
Discharge FET Failure	CHG FET commanded OFF *and* Current( ) ≥ DF.FETFailDSGThreshold for DF>FETFailTime	DSG FET commanded OFF *and* Current( ) ≥ DF.FETFail Threshold for DF>FETFailTime
AFE Comms Verification	AFE communications incorrect *and* AFE_Fail_Counter ≥ AFE_Fail_Limit	AFE communications incorrect *and* AFE_Fail_Counter ≥ AFE_Fail_Limit
Periodic AFE Verification	Periodic AFE RAM verification fails *and* AFE_Fail_Counter ≥ AFE_Fail_Limit	Periodic AFE RAM verification fails *and* AFE_Periodic_Fail_Counter ≥ AFE_Fail_Limit
Data Flash Verification	N/A	Periodic checksum verification = DF.Checksum

3.8 Charge Control Features

The bq204 and the bq20z80 have the same feature set except for a few additions in the bq20z80.

SBS.ChargingCurrent( ) Temperature Throttling

Under normal fast charge conditions the *SBS.ChargingCurrent( )* can be reduced per the following:

If *DF.Charge Suspend Temperature High (CHGSUSPH)* > *SBS.Temperature( )* ≥ *CHGSUSPH–DF.Delta Temperature (dT)*

Then *SBS.ChargingCurrent( )* = Pre-Charge Current

If *DF.CHGSUSPH –DF.dT* > *SBS.Temperature( )* ≥ *DF.CHGSUSPH*– 2 x *DF.dT*

Then *SBS.ChargingCurrent( )* = (Fast Charge Current - Pre-Charge Current) / 2

If *DF.CHGSUSPH*– 2 x *DF.dT* > *SBS.Temperature( )* ≥ *DF.Pre-Charge Temperature*

Then *SBS.ChargingCurrent( )* = Fast Charge Current

Note 1: If *DF.dT* = 0 then no change in *SBS.ChargingCurrent( )* from Fast Charge occurs.

Note 2: If *SBS.ChargingCurrent( )* is modified per this feature then *TCHG* in *SBS.ChargingStatus( )* is set

Pre-Charge Maximum Timeout

The bq2084 maximum-charge timeout does not differentiate between pre-charge and fast-charge modes. The bq20z80 differentiates between these modes, if the appropriate values are set in *SBS.ChargingCurrent( )*. Status is reported in *SBS.ChargingStatus( )*.

3.9 Data Flash Access

The bq2084 requires individual addressing of each byte of configuration data flash. As a result, new additions to the data-flash-constant array are added to the end of the array to minimize confusion and to enable easier updates. However, this causes problems with keeping data flash constants contiguous when new constants are added to existing features, eg: *Cell Over Voltage* at *DF 0x63,0x64* and *Cell Over Voltage Recovery* at *DF. 0xe0,0xe1* in the bq2084.

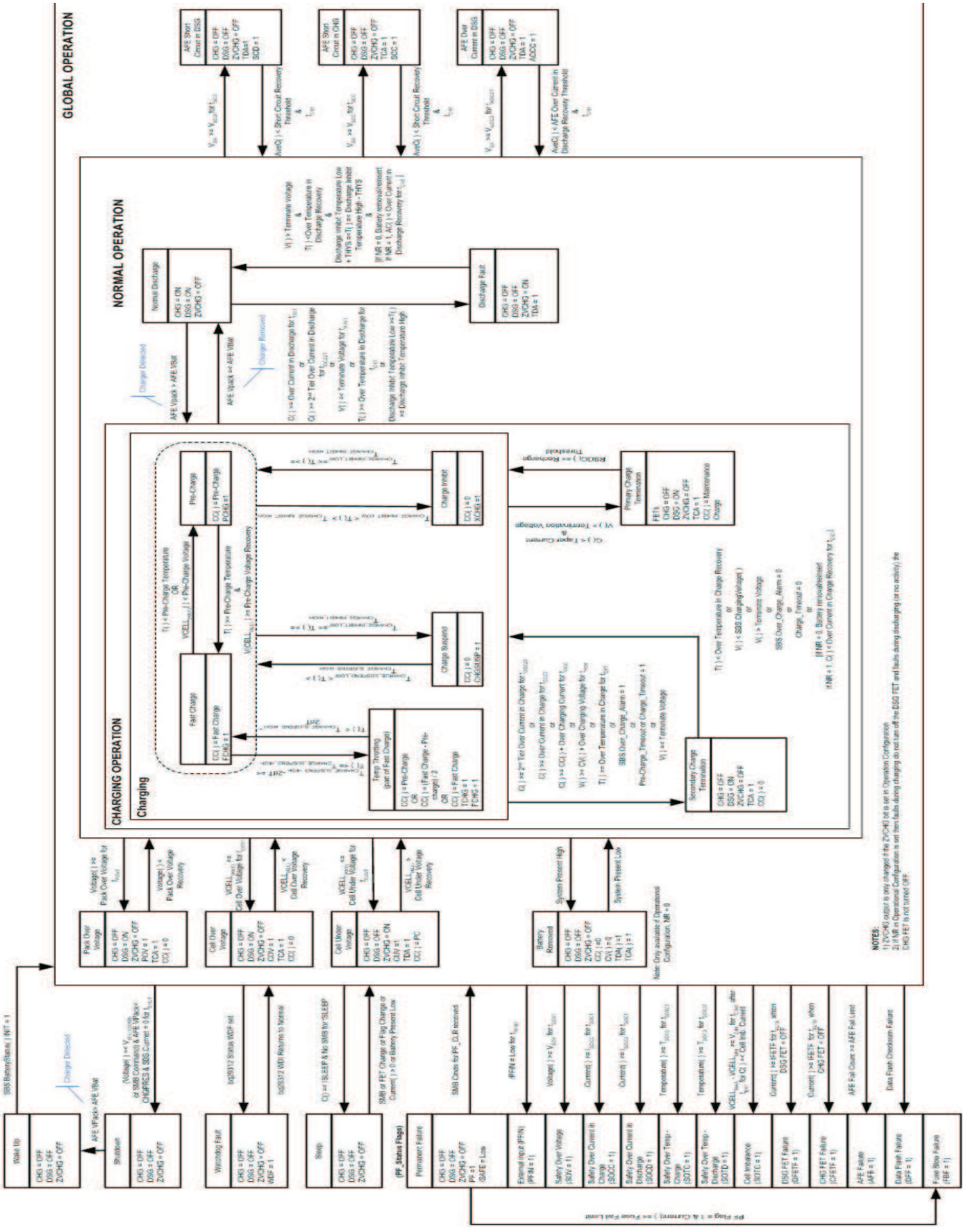
The bq20z80 uses a simpler addressing method where a Class and Subclass offset structure is used to access the data flash space. This allows easy grouping of like constants, and enables the introduction of new constants with the maximum ease to the user.

Eg: *Cell Over Voltage Recovery* is defined as:

Class = 1st Level Safety / Voltage = ID 0 with Subclass Offset = 3

3.10 Device Operational Diagrams

Operational diagrams for the bq2084 and bq20z80 are appended to the end of this application report.


GLOBAL OPERATION
NORMAL OPERATION
Normal Discharge
CHG = ON
DSG = ON
ZVCHG = OFF
Discharge Fault
CHG = OFF
DSG = OFF
ZVCHG = ON
TDA = 1
CHARGING OPERATION
Charging
Pre-Charge
Fast Charge
Charge Inhibit
Charge Suspend
Temp. Throttling (part of Fast Charge)
Primary Charge Termination
Secondary Charge Termination
Charge Detected
Charge Removed
AFE Short Circuit in DSG
AFE Short Circuit in CHG
AFE Over Current in DSG
Peak Over Voltage
Cell Over Voltage
Cell Under Voltage
Battery Removed
Wake Up
Shutdown
Watchdog Fault
Sleep
Permanent Failure
(PF_Status Flags)
NOTES:
1) ZVCHG output is only changed if the ZVCHG bit is set in Operation Configuration
2) If MR in Operational Configuration is set then faults during charging do not turn off the DSG FET and faults during discharging (or no activity) the CHG FET is not turned OFF

Exploring the bq20z80 Impedance Track™ Evaluation Kit

Battery Management

ABSTRACT

The bq20z80 evaluation module (EVM) and its corresponding evaluation software provides a rich and effective environment for examining the bq20z80 – a new, advanced battery gas gauge. This application report covers this EVM and software with an emphasis on how to use it and what to expect. EVM board connections are discussed in detail, and helpful hints are offered. For the evaluation software, components of each major screen are presented along with the various menu options.

4.1 Connecting the EVM

The cell-connection terminal blocks provide screw terminals for connecting 2, 3, or 4 cells to the evaluation module (EVM). The numbering convention for batteries is that Cell 1 is the most negative; so, connect the 1N (N=negative) terminal on the EVM to the most negative point of your battery stack.

If evaluating a 3-cell application, connect both 3P and 4P (P = positive) to the top node of the cell stack. Similarly, for a 2-cell application, connect 2P, 3P, and 4P to the top node.

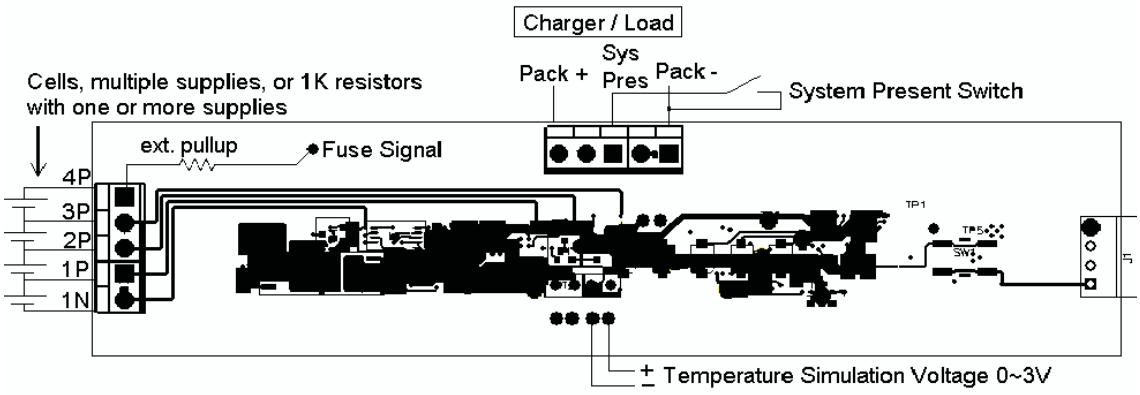


Figure 10. EVM Connections

Cells, Resistors, or Power Supplies?

For quick evaluation of the bq20z80 safety features, using real cells can be a burden. Therefore, substitute a string of 1-kΩ resistors fed with a single laboratory power supply. The supply can be varied quickly to investigate pack voltage protection. An additional floating supply can be connected across one of the resistors to simulate cell over- and undervoltages.

However, be aware that the Impedance Track™ algorithm, which relies on measuring the actual cell impedance, does not operate correctly without real cells.

Where is the Fuse?

The EVM does not include the chemical fuse that is employed in many battery pack applications. This eliminates the need for fuse replacement when running fault tests. Instead, the signal on TP4 shows the control that would blow the fuse. It requires an external pullup resistor to the battery voltage in order to monitor its state on a scope or meter

System Present and Pack Connections

The Pack+ and Pack– connections are used to connect the load and charger. It may be convenient to simultaneously connect a laboratory power supply and an electronic load in parallel. Most electronic loads have a load on/off switch and adjusting the constant current limit control to zero can disable the laboratory power supply.

Simulating Current

If using a string of resistors to simulate cells, it is difficult to apply an actual charge current. The solution is to connect a floating laboratory power supply between Pack– and Battery– (1N). Putting the floating supply in current limit provides a simulated charge current that is forced through the sense resistor. Depending on the laboratory power supplies available, this configuration can be useful for load current by reversing the polarity of the current source connections. Use this configuration to quickly test various overcurrent safety features or to validate coulomb counting accuracy. However, be aware that this method bypasses the protection FETs, and fault conditions will not interrupt the charge or load current.

Simulating Temperature

Because the temperature measurement works by measuring the voltage on the thermistor pin, a temperature chamber for safety evaluation is unnecessary. Just connect a laboratory power supply across the RT1 terminals with the positive output on X3 (see the EVM schematic located at the end of this document). In this case, this power supply does not have to be isolated from the supply used to simulate a charger/load because the return side of the thermistor is the same as Pack–. Forcing 0 V ~ 3 V across the thermistor allows testing the safety features over the full temperature range.

4.2 Scanning the SBS Registers

With the battery connections made, start the evaluation software. When first connected, the circuitry may be in shutdown mode. This normally requires applying a charging source across the Pack+ and Pack– terminals. If a charger voltage is not connected, briefly connect the positive battery voltage to Pack+.

Setting the Scan Interval

By default, the SBS register scanning is off. Put a check in the *Keep Scanning* box to get the scanning started. A periodic update of all the SBS registers should appear. Note the blue progress bar at the bottom. The interval between scans can be set in the Options | Set Scan Interval menu. The program remembers this setting and uses it each time the program is launched.

Adjusting the View

With some screen resolutions, it may not be possible to see all of the register displays simultaneously. In some cases, this can be improved by making the top buttons invisible. Use the View | Display Buttons menu to remove these objects from the screen (see Figure 11).

The Evaluation Software, EVSW, has the flexibility to allow multiple views. Two or three screens can be tiled onto the display at once. After opening any of the SBS, Data Flash, or Pro screens, use the Window menu to tile them either vertically or horizontally. Figure 12 shows a vertically tiled view of all three.

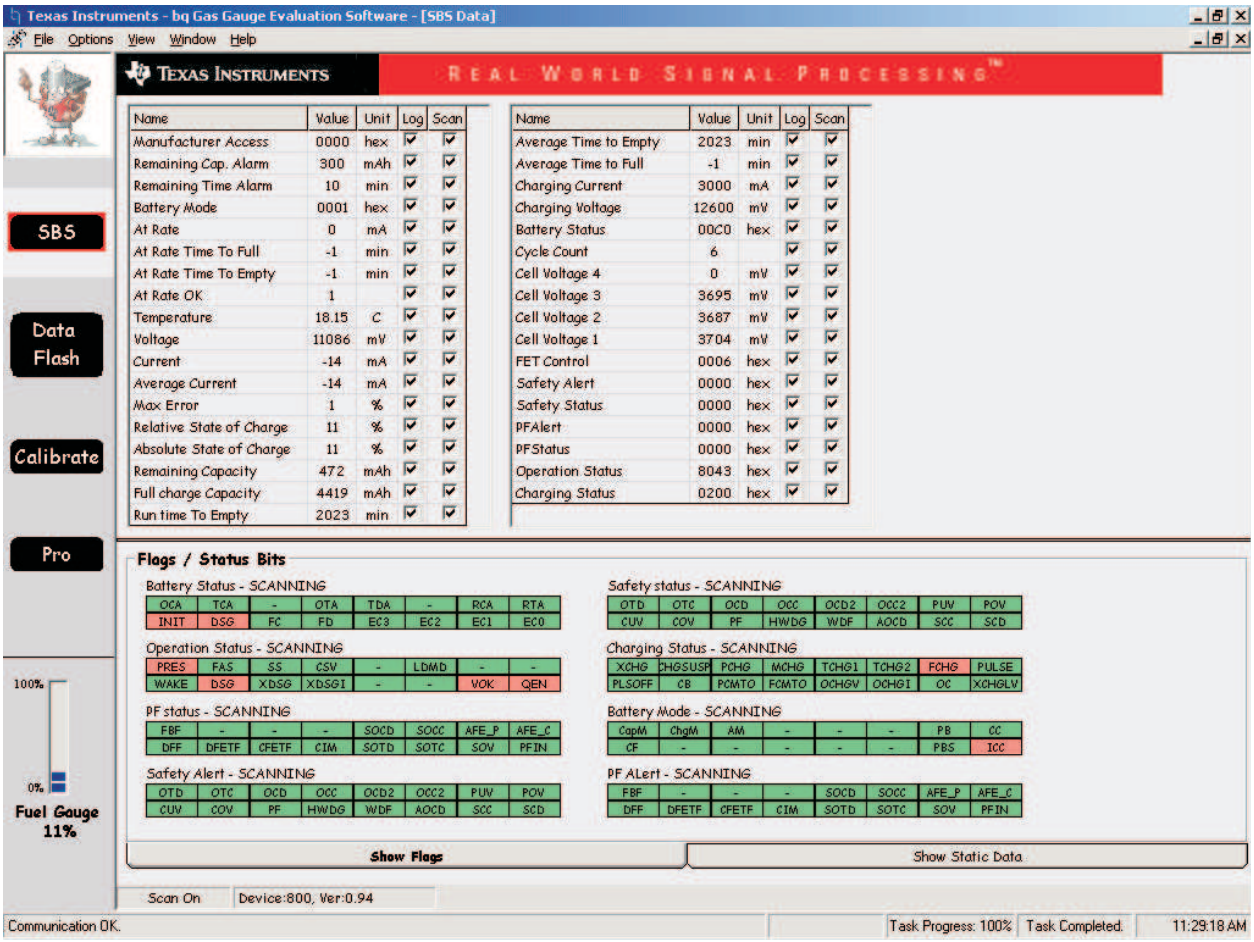


Figure 11. All Flags and Status Bits Are Visible on a 1024x768 Screen if the Top Display Buttons Are Hidden

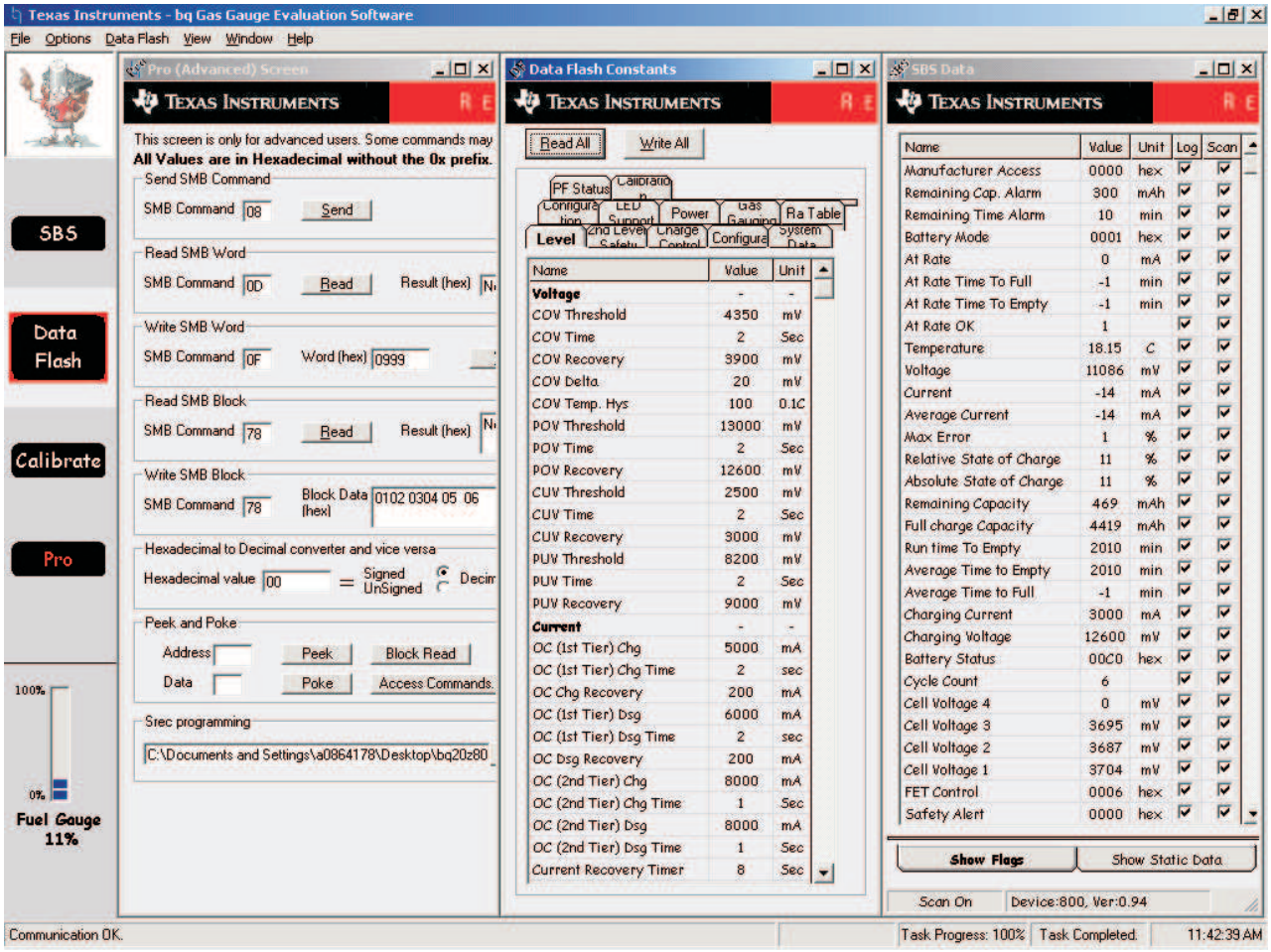


Figure 12. Vertically Tiled View of SBS, Data Flash, and Pro Screen

Flags / Status Bits

The flags and status bit displays are bit expansions of the various status, alert, and battery mode registers. The red bit cells are asserted, whereas the green cells are not. The displayed mnemonics are an improvement compared to decoding hexadecimal digits, but consult the data sheet to learn the full definition for each bit.

4.3 Logging the SBS Registers

Due to the long time associated with battery testing, it is common to data-log complete charge and discharge cycles for later analysis. When evaluating a new cell type, or a new gas gauge device, logs provide a convenient and effective way to understand the process.

Configuring the Log File

The log file can be configured to record any combination of the displayed SBS and extended registers. Simply check or uncheck the items to log. Select or deselect all of them quickly using the Options menu. It is usually a good idea to deselect the registers that are not relevant to the experiment being performed in order to simplify the process of reading the log later and to reduce the size of the log file.

The logging interval is also configured from a dialog box available in the options menu. Consider the purpose for the log when choosing an interval. If you expect to see several events during a short period, or are looking for a transient phenomenon, then a short interval, such as 1000 milliseconds can be used. This produces a huge file when run overnight, so decrease the resolution if it is not really necessary.

Start and stop the logging process with the buttons near the top of the screen. The state of the Start Logging and Stop Logging buttons immediately reveal if the program is logging or not.

Using Excel for Log File Evaluation

The log file is written as records of tab delimited ASCII. This file format can be imported into Microsoft™ Excel without any extra steps. Just right-click on the file name, and select Open With | Microsoft Excel for Windows™. However, one problem that can arise is with columns containing hexadecimal values. If the data contains an "e", Excel interprets this as scientific notation by default. If this situation occurs, use the import function in Excel, and modify the column type for the target column to be "text."

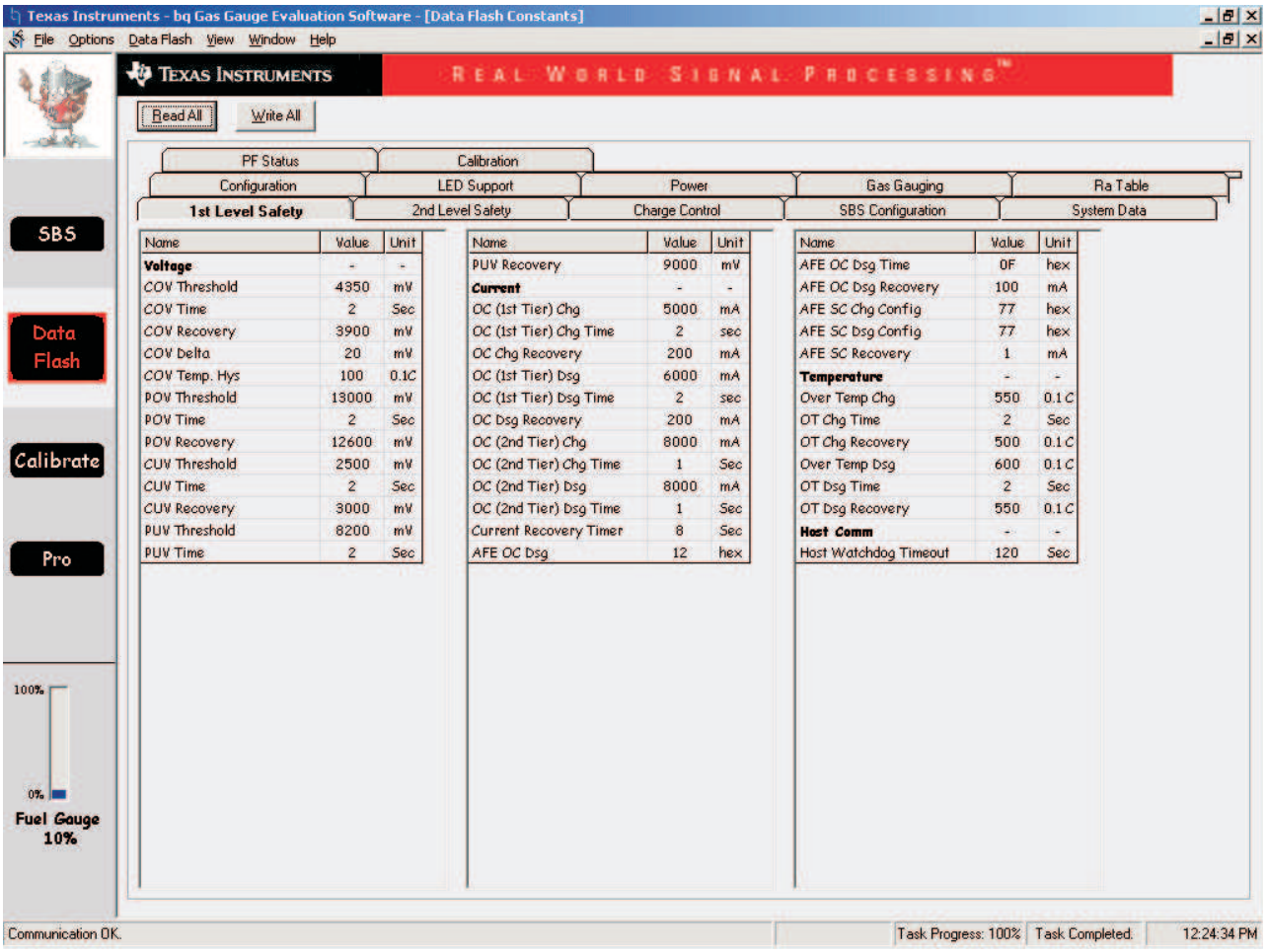
Microsoft Excel has a function in its Window menu called Freeze Panes, which is extremely helpful for reviewing long lists of records. Highlight the first row of data, under the heading row, and choose Freeze Panes from the Window menu. Now you can scroll through the entire log and still see the heading for each column. Sometimes, it is more convenient to delete the header information in lines 1 through 11.

4.4 Editing the Data Flash

The data flash screen displays the classes and subclasses used to categorize the data flash constants. The classes are on the index tabs at the top. Select a tab to activate the display for all the constants within that class. The 12 data flash constant classes are 1st Level Safety, 2nd Level Safety, Charge Control, Gas Gauging, SBS Configuration, Ra Table, Pf Status, Calibration, System Data, Configuration, LED Support, and Power. Each constant is described in the application report *Configuring the bq20z80 Data Flash* (SLUA342).

Navigating the Data Flash – Classes and Subclasses

The classes of constants are selected with the tabs; under each class are also subclass groupings . For example, click on the 1st Level Safety Tab. Shown in the grids are the various data flash constants with subclass indicators in bold type. In this case, the subclasses are Voltage, Current, Temperature, and Host Comm.



Name	Value	Unit
Voltage	-	-
COV Threshold	4350	mV
COV Time	2	Sec
COV Recovery	3900	mV
COV Delta	20	mV
COV Temp. Hys	100	0.1C
POV Threshold	13000	mV
POV Time	2	Sec
POV Recovery	12600	mV
CUV Threshold	2500	mV
CUV Time	2	Sec
CUV Recovery	3000	mV
PUV Threshold	8200	mV
PUV Time	2	Sec

Name	Value	Unit
PUV Recovery	9000	mV
Current	-	-
OC (1st Tier) Chg	5000	mA
OC (1st Tier) Chg Time	2	sec
OC Chg Recovery	200	mA
OC (1st Tier) Dsg	6000	mA
OC (1st Tier) Dsg Time	2	sec
OC Dsg Recovery	200	mA
OC (2nd Tier) Chg	8000	mA
OC (2nd Tier) Chg Time	1	Sec
OC (2nd Tier) Dsg	8000	mA
OC (2nd Tier) Dsg Time	1	Sec
Current Recovery Timer	8	Sec
AFE OC Dsg	12	hex

Name	Value	Unit
AFE OC Dsg Time	0F	hex
AFE OC Dsg Recovery	100	mA
AFE SC Chg Config	77	hex
AFE SC Dsg Config	77	hex
AFE SC Recovery	1	mA
Temperature	-	-
Over Temp Chg	550	0.1 C
OT Chg Time	2	Sec
OT Chg Recovery	500	0.1 C
Over Temp Dsg	600	0.1 C
OT Dsg Time	2	Sec
OT Dsg Recovery	550	0.1 C
Host Comm	-	-
Host Watchdog Timeout	120	Sec

Figure 13. Example of bq20z80 Data Flash Organization. 1st Level Safety Class of Data Flash Constants. Subclasses are Voltage, Current, Temperature, and Host Comm.

Reading and Editing Data Flash

Use the Read All button initially to populate the grids. Make a change to any constant in the value column, and press Enter to write the new value into the device data flash. Note that data cannot be written to the device if it is sealed or in a permanent fail state.

Exporting and Auto Export

A list of all the data flash values may be stored to a text file with a .gg extension. The format of this file includes the class, subclass, name, and value for each data flash location. For example:

- [Voltage(1st Level Safety)]
- COV Threshold = 4350
- COV Time = 2
- COV Recovery = 3900
- COV Delta = 20
- COV Temp. Hys = 100
- POV Threshold = 13000
- POV Time = 2
- POV Recovery = 12600
- CUV Threshold = 2500

- CUV Time = 2
- CUV Recovery = 3000
- PUV Threshold = 8200
- PUV Time = 2
- PUV Recovery = 9000

Note that the constants are grouped under subclass and class which are identified with a line of text in the format: [Subclass(Class)].

These files can be generated automatically at programmed intervals using the AutoExport feature. Use the Options menu to set the interval and the file name. Then, start the feature with the AutoExport menu command. At each programmed interval, a new .gg file is written, with an index number appended to the file name. This feature is useful for tracking data flash values that may change over time, such as the resistance values for each cell in the Ra Table.

Importing and Writing All

The .gg file can be saved and then imported into another device. Use the File | Import menu to select a .gg file. Doing this brings the data into the data flash grids, where it can be reviewed and edited. To transfer all the data into the bq20z80 gas gauge, push the Write All button.

4.5 Calibrating the bq20z80

The calibration screen provides a flexible platform for device calibration of offsets, voltage, current, and temperature. The four common calibration functions and an optional pack voltage calibration and board offset calibration appear on this screen.

CC Offset Calibration

The coulomb current offset calibration is a prerequisite for voltage, temperature, and current gain calibrations, because a gain calibration with an offset present is not accurate. By default, this is a quick version of the offset calibration. A full calibration occurs each time the bq20z80 enters sleep mode. Although the various gain calibrations may be performed independently, the CC offset calibration must be performed at least once prior to use in order to correct for any CC offset error.

Voltage and Temperature Calibration

Enter the known value of voltage and temperature. Select the number of cells in the application. Select the type of temperature sensors used in the application.

Current Calibration

Enter the applied current, which should be approximately 2 A.

Pack Voltage Calibration

Pack voltage calibration is not generally necessary. This is used to calibrate a separate measurement path, which only detects if a charger is present.

Board Offset Calibration

Board offset calibration is not so much a calibration as it is a characterization of the current leakage errors and noise inherent in a given PCB design. The value should be found for a given design and then used for each board produced. For best accuracy, absolutely no current must flow through the sense resistor, including the current used to power the devices. That means that the bq29312 must be powered from the charger and not from the cells. The protection FETs are automatically opened during this procedure to ensure that the AFE is powered only from the pack input. Therefore, device current does not pass through the sense resistor.

4.6 The Pro Screen

The Pro screen can be used to read and write low-level SMBus transactions, peek and poke the RAM of the bq20z80, and reprogram the bq20z80 flash memory. The write operations should not be done without understanding the implications.

SMB Commands, Words, and Blocks

SMBus commands, words, and blocks can be easily read or written on the Pro screen. The most common use of this facility is to send 0x0021 to SMB command 0x00 (Manufacturer Access) in order to start the Impedance Track™ algorithm.

Peek and Poke

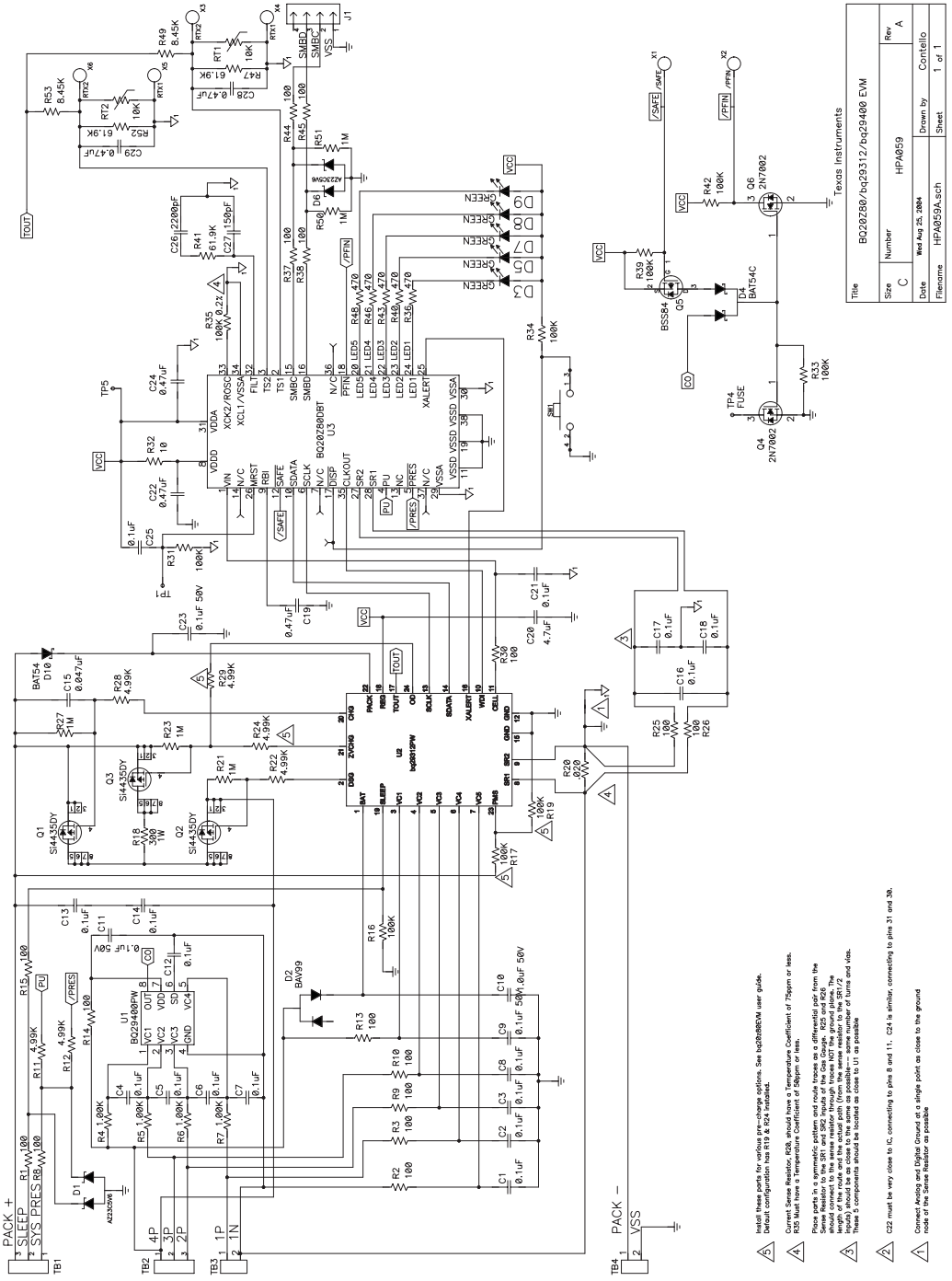
Use this feature only for advanced debugging with the guidance of TI engineers. The peek and poke feature may not be available in some versions of this program.

SREC Programming

Programming or *Re-flashing* the bq20z80 is also an advanced topic, which can be useful in certain circumstances. The object files used to program the device have the extension *.senc* which refers to an encrypted s-record.

4.7 EVM Schematic

The EVM schematic appears on the following page.



Theory and Implementation of Impedance Track™ Battery Fuel-Gauging Algorithm in bq20z8x Product Family

PMP Portable Power

ABSTRACT

In fuel gauge solutions, current integration and voltage correlation algorithms suffer from a decrease in accuracy with battery aging and also require extensive data collection. This application report outlines the theory of Impedance Track™ (IT) technology that overcomes these problems. Implementing the IT algorithm in the Texas Instruments bq20z8x family is reviewed and setting the data flash constants associated with the fuel-gauging algorithm is described in detail.

5.1 Summary of the Algorithm Operation

The Impedance Track™ gas gauge algorithm(1) uses three types of information to calculate remaining capacity (*SBS.RemainingCapacity( )*) and full charge capacity (*SBS.FullChargeCapacity( )*).

1. Chemical: depth of discharge (DOD), and total chemical capacity Q_{max}
2. Electrical: internal battery resistance dependence on DOD
3. External: load, temperature

SBS.FullChargeCapacity( ) is defined as the amount of charge passed from a fully charged state until the voltage defined in *DF:Terminate Voltage* flash constant is reached at a given rate of discharge, after subtracting the reserve capacity (*DF:Reserve Capacity*).

Note that it depends on the rate of discharge and is lower at higher rates and low temperatures because the cell I x R drop causes the Terminate Voltage threshold to be reached earlier.

(1) Impedance Track algorithm is protected by US Patents US6832171, US6789026, and US6892148.

5.2 Detailed Description of Parameters Updated by the Gas Gauge Algorithm

Modes of Algorithm Operation

The algorithm differentiates between *charge*, *discharge*, and *relaxation* modes of operation. During *charge* mode, the SBS.OperationStatus( ) [DSG] bit is cleared, and during *discharge* and *relaxation* mode, it is set. Entry and exit of each mode is controlled by Data Flash (DF) parameters in the subclass Gas Gauging: Current Thresholds section as illustrated in Figure 14. Charge mode is exited, relaxation mode is entered when *SBS.Current( )* goes below *DF:Quit Current* and after a *DF:Chg Relax Time* period. Discharge mode is entered when *SBS.Current( )* goes below *DF:Dsg Current Threshold*. Discharge mode is exited, relaxation mode is entered when *SBS.Current( )* goes above *—DF:Quit Current* threshold and after a *DF:Dsg Relax Time* period. Charge mode is entered when *SBS.Current( )* goes above *DF:Chg Current Threshold*.

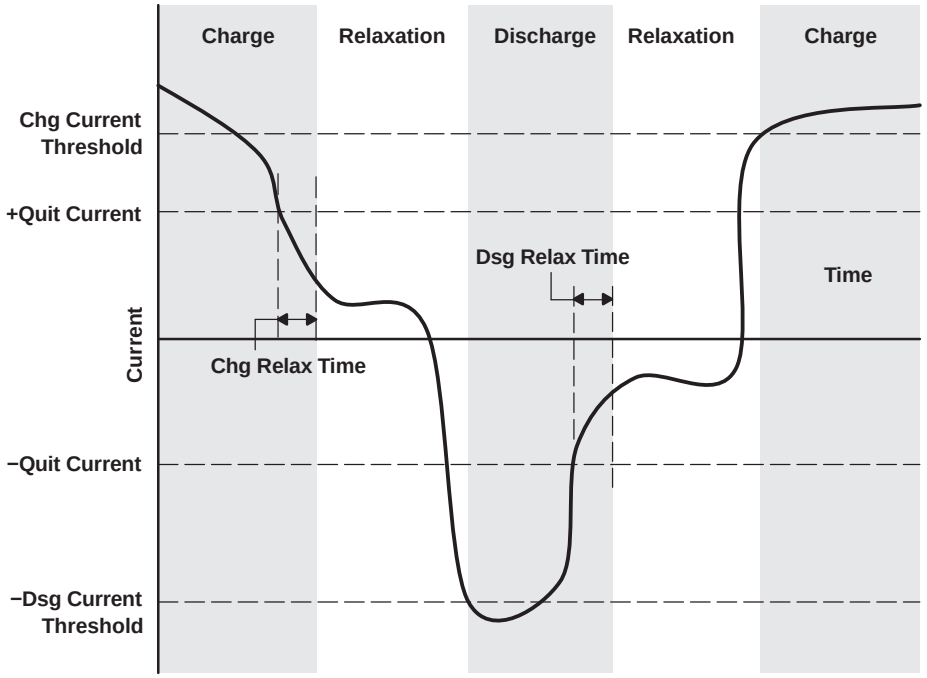


Figure 14. Example of the Algorithm Operation Mode Changes With Varying *SBS.Current( )*

Update of Chemical Depth of Discharge (DOD)

The gas gauge updates information on the chemical depth of discharge (DOD_0) based on open-circuit voltage (OCV) readings when in a relaxed state. This is done for each cell separately. DOD is found by correlating DOD with OCV using a predefined table DOD(OCV,T) stored as reserved data flash parameters. The table is specific for a particular chemistry such as $LiCoO_2$/carbon (default settings), $LiMn_2O_4$/carbon, etc., and can be identified by reading the chemistry ID through sending SBS.ManufacturerAccess( ) command 0008, then reading SBS.ManufacturerAccess().The gas gauge can be set up for a particular chemistry by using the relevant firmware file (*.senc) that can be downloaded from the bq20zXX production folder on power.ti.com. See *Support of Multiple Chemistries* (SLUA384) for more details.

Figure 15 shows the timing of parameter updates during the relaxation mode. First, OCV readings and DOD_0 calculations are taken after a 30-minute relaxation period has passed. Then, OCV readings continue to be taken every 100 seconds. DOD is calculated based on each measured OCV reading using the linear interpolation DOD = f(OCV,T). Integrated PassedCharge is set to zero at each DOD_0 update.

If the current during the OCV reading is non-zero, then an IR correction is done. The first iteration of DOD is found from the uncorrected OCV reading; then the resistance value is found from the R(DOD) table and used to correct the OCV value as OCV′= OCV - I x R. Then, the corrected DOD is found from OCV′. This method achieves the best accuracy if the current during relaxation mode is below the C/20 rate. This is why it is recommended that the DF.Quit Current not exceed C/20.

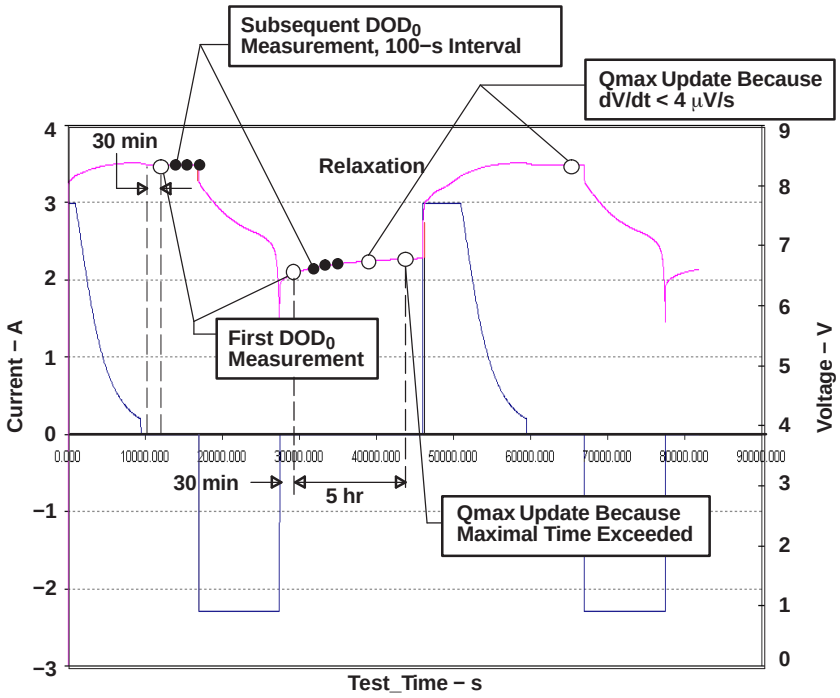


Figure 15. Timing of DOD_0 and Qmax Updates During Relaxation Mode

If no DOD_0 has been measured until the relaxation state is exited, the previous DOD_0 is used along with the PassedCharge integrated since the last DOD reading.

During charge and discharge modes, the *present* DOD is recalculated every second as DOD = DOD_0 + PassedCharge/Qmax. DOD is used for determining when a resistance update needs to occur, as well as the starting point for a Remaining Capacity (and FCC) calculation. Remaining capacity calculations occur immediately after discharge onset, at every resistance update, and after entering relaxation mode.

Update of Qmax

Maximal chemical capacity Q_{max} for each serial cell is stored in Data Flash as *DF:QmaxX*, where X=0, 1, 2, or 3, the cell serial number.

The GG updates Q_{max} based on two DOD readings made before and after charge or discharge, for each serial cell separately. For example, DOD_1 is taken during relaxation, then discharge mode starts, and PassedCharge is integrated. Following this, another relaxation mode is entered, and DOD_2 is taken.

DOD1 and DOD2 are calculated from OCV readings in a well-relaxed state, as exemplified in Figure 15. A well-relaxed state is detected if dV/dt < 4 μV/s or maximal waiting time of 5 hours is exceeded. The first condition is satisfied in typical batteries after about 1 hour if DOD is between 0% and 80%, and 3–4 hours if DOD is above 80%. At a low temperature, relaxation takes a longer time.

In order to ensure high accuracy of DOD measurement, Qmax calculation do not occur if the temperature is above 40°C or below 10°C. It also does not occur if at least one of voltage measurements for DOD_1 or DOD_2 was taken in the cell voltage range between 3737 mV and 3800 mV because of flat OCV(DOD) dependence in this range. These limits are chemistry dependent and will be specified separately for different chemistries.

Qmax is calculated as Qmax = PassedCharge / (DOD_2– DOD_1).

The data flash constant *DF.Update Status* increments by 1 when the first Qmax update takes place (e.g., from 4 to 5 if no resistance updates were made, or from 5 to 6 if a resistance update was made). *SBS.Max Error( )* becomes 5% in the first case and 1% in the second case

PassedCharge has to be more than 37% of *DF:Design Capacity* for an update to occur. For the first cycle (with *DF:Update Status* = 4), 90% of *DF:Design Capacity* is required because this cycle takes place in the factory settings and Qmax is learned for the first time.

In order to prevent Qmax fluctuations, a first-order smoothing filter is applied to all Qmax readings except in the first cycle. Readings with lower PassedCharge are assigned lower weights in the smoothing.

Update of Resistance

Resistance is updated during discharge, as summarized in Figure 16. The first resistance update happens after 500 seconds, to prevent distortion from transients after load onset.

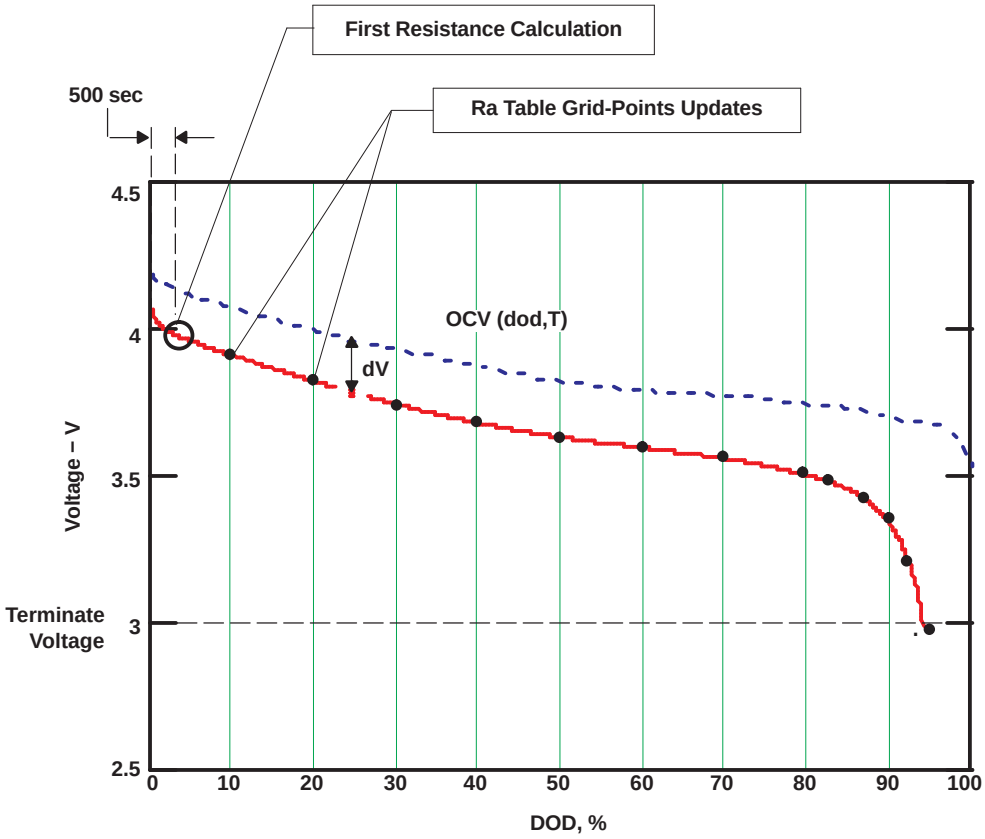


Figure 16. Impedance Updates

Calculation is performed by comparing the measured voltage with the OCV value at the same DOD, that is taken from the OCV(DOD,T) table:

dV = V – OCV(DOD,T)

R(DOD) = dV/I

Resistance measurements are taken continuously and stored in RAM.

Resistance is updated in the Data Flash (in *DF:Ra Table*) after each 11.1% of DOD charge (1/9th increment) is exceeded (DOD charge is PassedCharge/Qmax). When DOD reaches 77.7%, resistance is updated after each 3.2%. The final resistance update is made after discharge is terminated.

The constant *DF.Update Status* increments by 1 when the first grid-point resistance update takes place (e.g., from 4 to 5 if no Qmax updates were made before, or from 5 to 6 if Qmax updates were made before).

Before storage to Data Flash, resistance values are normalized to 0°C as Ra[dod] = R[dod]/exp(Rb[dod] x T) where R is the measured resistance value at a given DOD, Rb[DOD] is the value of temperature coefficient of impedance change at a given DOD stored as a reserved data-flash table, and T is temperature in °C. Note that values of resistance normalized to 0°C are somewhat larger than values at room temperature and so cannot be directly compared with R=dV/I values.

Resistance values for the grid points with a higher DOD than presently updated are scaled by the same factor as the present grid-point change, e.g., by factor Ra_new/Ra_old. In this way, faster convergence of the resistance profile is achieved.

Values in *DF.Ra Table* are stored in mΩ units, in the format CellX Ra N where X is a cell serial number from 0 to 3, and N is grid-point number from 0 to 14 that corresponds to 10% increments of DOD until 80%, and then 3.3% increments of DOD. The CellX flag and xCellX flag are used for interchanging the data-flash column usage for reducing the number of DF writes. A flag value of 55 indicates the presently used data column; 00 indicates the presently unused data column.

If during resistance update, the DOD exceeds 100%, or resistance appears negative, which are both indications of a too-small DF.QmaxX initial guess, DF.QmaxX increments by 10% and all resistances are recalculated. This is normal behavior during the first *learning* cycle. However, if the initial guess of DF.QmaxX was too far from the correct value, the second cycle might be needed to achieve full resistance accuracy. To avoid this, set DF.QmaxX to a value specified by the cell manufacturer, multiplied by the number of parallel cells.

Update of Temperature Model

Because temperature changes significantly during the course of a discharge, the algorithm needs to be able to predict the future temperature. This is needed for temperature correction of battery impedance R = Ra x exp(Rb x T)) during voltage simulation near the end of a discharge. To achieve this, the algorithm collects T(t)-dependence data during discharge. It is used to update parameters of a simple thermal model including a heat exchange coefficient and a thermal time constant. These parameters are updated at the same time as resistances. The algorithm also records the outside temperature (T_out) during relaxation periods. These parameters are used to define a function T(t, T_start) that calculates a temperature profile starting from present temperature, T_start, and continuing until the end of discharge.

Update of Remaining Capacity (RM) and Full Charge Capacity (FCC)

Update of RM and FCC takes place after each resistance grid-point update, at the end of discharge, and at the exit of relaxation mode.

FCC consists of 3 parts:

$$SBS.FullChargeCapacity( ) = Q_{start} + PassedCharge + RM$$

Components of FCC are indicated in an example in Figure 17.

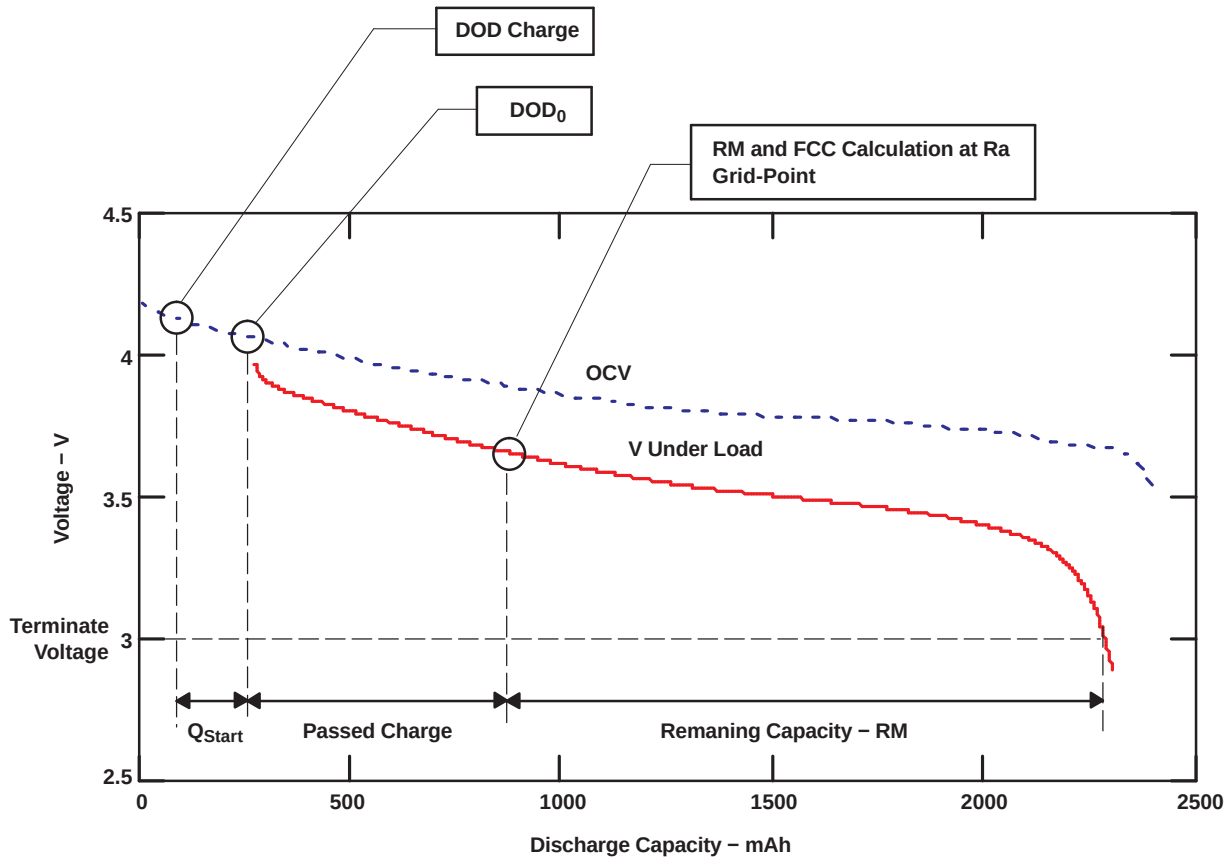


Figure 17. Components of SBS.FullChargeCapacity( ) Value

1. Q_{start} is the charge that would have passed to make DOD = DOD_0 from a fully charged state (DODcharge). For a fully charged battery, Q_{start}= 0. Q_{start} is recalculated at the exit of the relaxation mode. In the case of constant current, it is simply $Q_{start} = Q_{max} \times$ (DOD0 – DODcharge), but for the constant power case a voltage simulation is run. DODcharge is assigned equal to DOD_0 at first DOD_0 update, after charge termination by taper current. Note that DODcharge is somewhat higher than 0 because chargers typically do not charge a battery to full.
2. PassedCharge is the coulomb count integrated during the present discharge or charge, and set to zero at every DOD_0 update.
3. Remaining capacity is calculated after each resistance grid-point update and at the end of discharge.

SBS.RemainingCapacity( ) (RM) is calculated using a voltage simulation. The GG starts a simulation at the present DODstart = DOD_0 + PassedCharge/Qmax and continue calculating voltage V(DODx,T) = OCV(DODx,T) + I x R(DODx,T) by incrementing DOD with dDOD increment of 4%. DOD[i]=DODstart + dDOD x I. This incrementing is continued until the simulated voltage V(DOD[i]) becomes less than *DF.Terminate Voltage*. Once that happens, the final DOD *SBS.RemainingCapacity( )* = (DODfin-DODstart) x Q_{max} is detected. Note that Q_{max} for the lowest capacity cell is used.

Current that is used in the simulation is the average current during the present discharge (several types of averaging can be selected using *DF:Load Select* data flash constant). A simulation can run in constant current mode (*DF:Load Mode* = 0) or constant power mode (*DF:Load Mode* = 1).

Update of SBS.Remaining Capacity( ) and SBS.RemainingStateOfCharge( ) Values

Although *SBS.FullChargeCapacity( )* is only updated at a few points during a discharge as previously described, the *SBS.RemainingCapacity( )* is updated continuously (every 1 second) based on the integrated charge. *SBS.RemainingCapacity( )* = RM – Q_integrated where Q_integrated is charge passed since the last RM calculation. The value of *SBS.RemainingCapacity( )* is also used to update *SBS.RelativeStateOfCharge( )* every second as *SBS.RelativeStateOfCharge( )* = *SBS.RemainingCapacity( )* x 100/*SBS.FullChargeCapacity( )*.

The same value is used to calculate the run-time to empty as *SBS.RunTimeToEmpty( )* = *SBS.RemainingCapacity( )* / *SBS.AverageCurrent( )*.

Note that even if a simulation of RM is run in constant power mode (*DF:Load Mode* = 1), the reporting of *SBS.RemainingCapacity( )* and *SBS.RemainingRunTime( )* can be done either based on mAh or in 10mWh values. The mAh or mWh reporting depends on the setting of *SBS.BatteryMode( ) [CAPACITY_MODE]* bit (0=mAh, 1=10mWh). In case of a second setting, the run-time-to-empty is calculated as SBS.RunTimeToEmpty( ) = SBS.RemainingEnergy( ) / SBS.AveragePower( ) and is generally more accurate for most devices because of increased power consumption at low voltages.

Update of SBS.Max Error()

SBS.Max Error() is an estimate of maximal error of SBS.RSOC. Initially, it is set to 100% because the fuel gauge has no information about the battery. After Qmax is learned, or resistance is learned (as indicated by DF.Update Status = 5), SBS.Max Error changes to 5%. After the second part of the database (resistance or Qmax) is learned (Update Status = 6), SBS.Max Error changes to 1%. SBS.Max Error( ) is increased to reflect the number of cycles since the last Qmax. This is achieved by storing the cycle number when Qmax was last updated in an internal variable Qmax_cycle. SBS.Max Error is then calculated as Max Error + (SBS.Cycle Count() – Qmax_cycle) x 0.05. This means that SBS.Max Error increases by 1% in 20 cycles, e.g., only occasionally is a Qmax update needed to maintain high accuracy.

bq20z80 EVM Data Flash Settings for Number of Serial Cells and Pack Capacity

PMP Portable Power

ABSTRACT

This application report describes the configuration changes in the data flash constants in the Texas Instruments bq20z80 Gas Gauging Evaluation Software required for a variety of battery-pack configurations.

The factors affecting the settings include the number of cells in series and the pack capacity. The pack capacity is determined by the cell capacity and the number of cells are in parallel.

Configurations are described (for example) as 3s2p, which stands for 3 cells in series and 2 in parallel. All changes must be done before enabling the Impedance Track™ feature in the bq20z80.

Section 1 describes the changes required when changing series-cell count, and Section 2 explains settings for varying the pack capacity. Illustrations are provided showing the specific locations in the data flash screens of the evaluation software.

6.1 Changes to Default 4 Series Cell Configuration

The following changes from the default settings must be made to enable a 2-series or 3-series cell pack before enabling the Impedance Track™ feature in the EVM. If a 4-series cell pack is connected, the EVM can be used in the default setting.

In addition to the serial configuration, the design capacity of the cells must be considered. This information is found on the cell-manufacturer data sheet and must be set in the data flash. This is described in Section 2 of this application note.

Table 14. First Level Safety

Setting	2-Cell	3-Cell	4-Cell (Default)
POV Threshold	8700	13000	17500
POV Recovery	8400	12600	16000
PUV Threshold	5400	8100	11000
PUV Recovery	5700	8500	12000

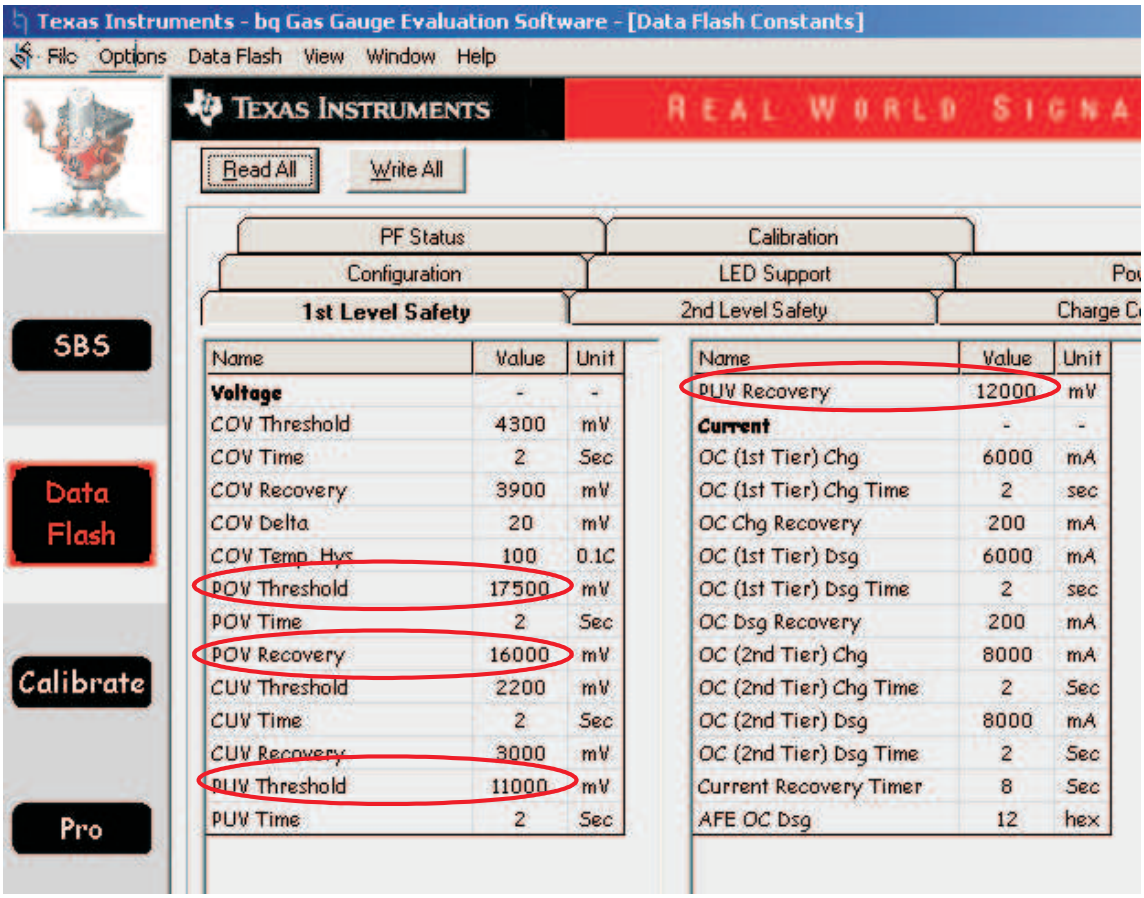


Table 15. Second Level Safety

Setting	2-Cell	3-Cell	4-Cell (Default)
SOV Threshold	9000	13500	18000

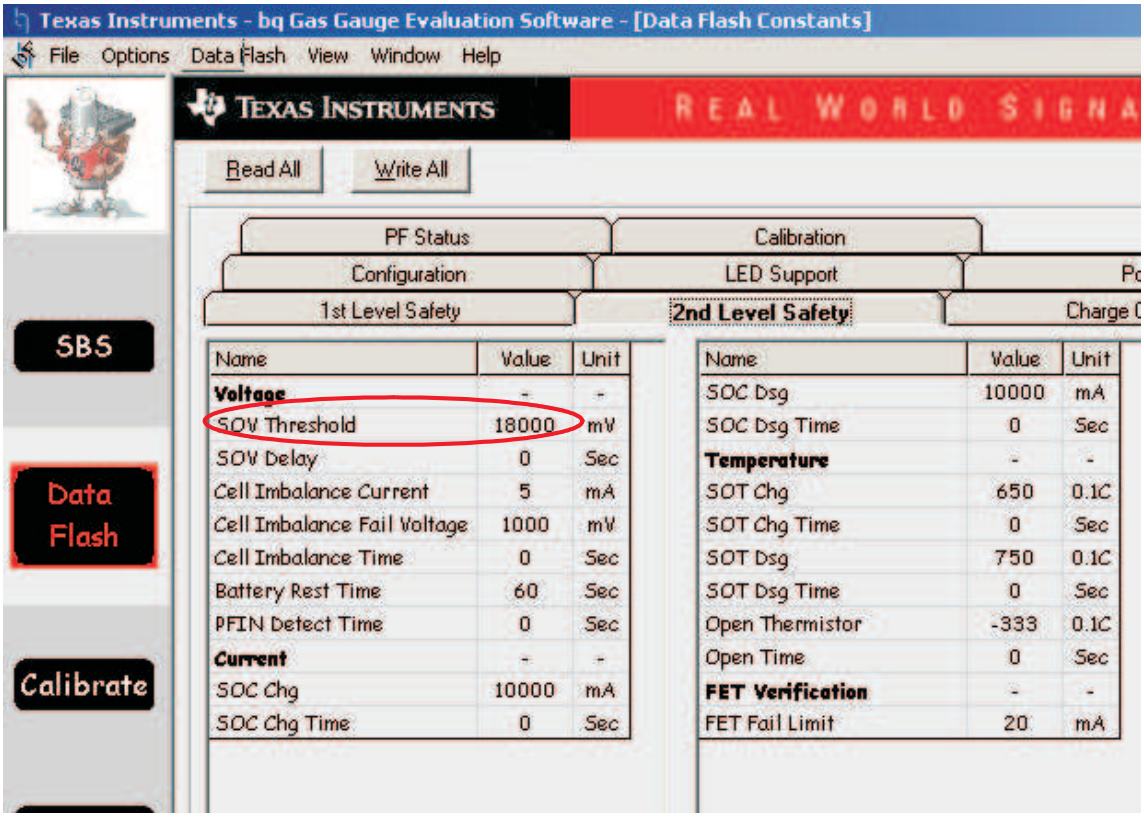


Table 16. Charge Control

Setting	2-Cell	3-Cell	4-Cell (Default)
Charging Voltage	8400	12600	16800

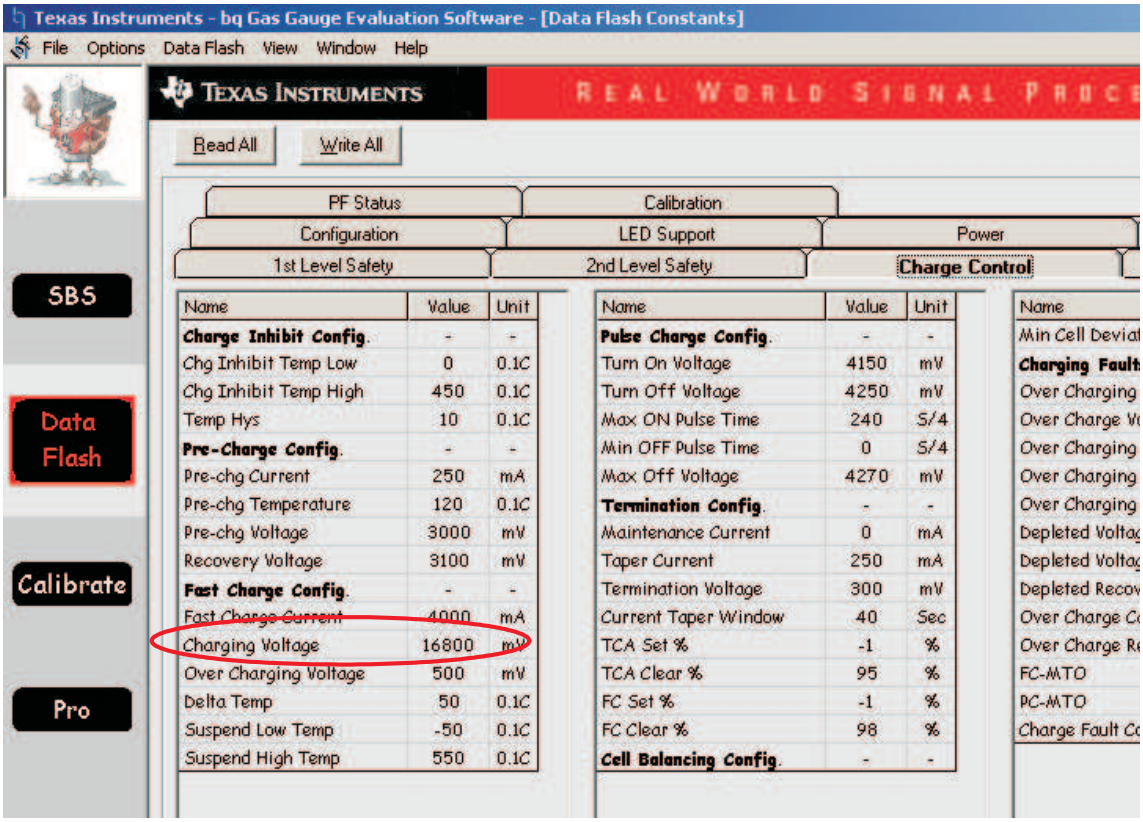


Table 17. SBS Configuration

Setting	2-Cell	3-Cell	4-Cell (Default)
Design voltage	7200	10800	14400

Also see the description of the Design Energy setting in Section 2.

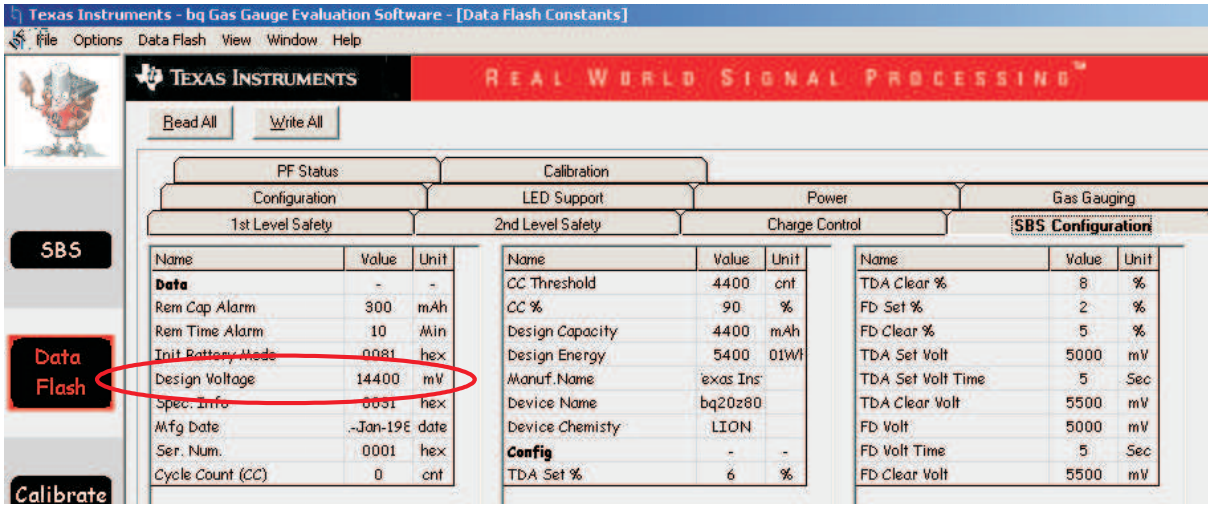


Table 18. Configuration

Setting	2-Cell	3-Cell	4-Cell (Default)
Operation CfgA	2d29	2e29	2f29

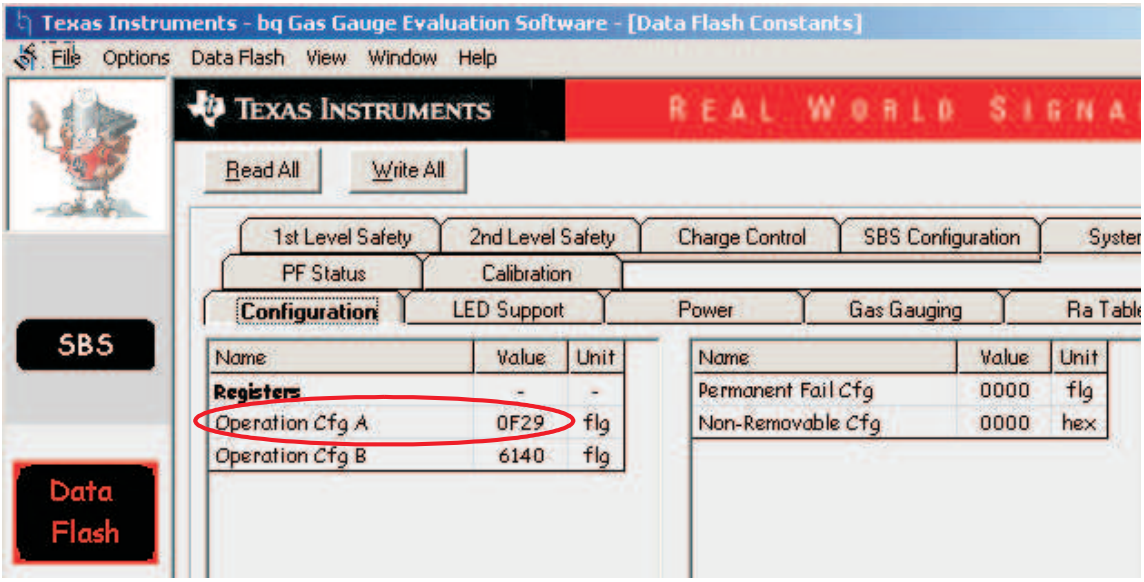


Table 19. Power

Setting	2-Cell	3-Cell	4-Cell (Default)
Flash Update OK Voltage	6000	7500	7500
Charger Present Threshold	2500	2500	2500
Shut Down Voltage	5000	7000	7000

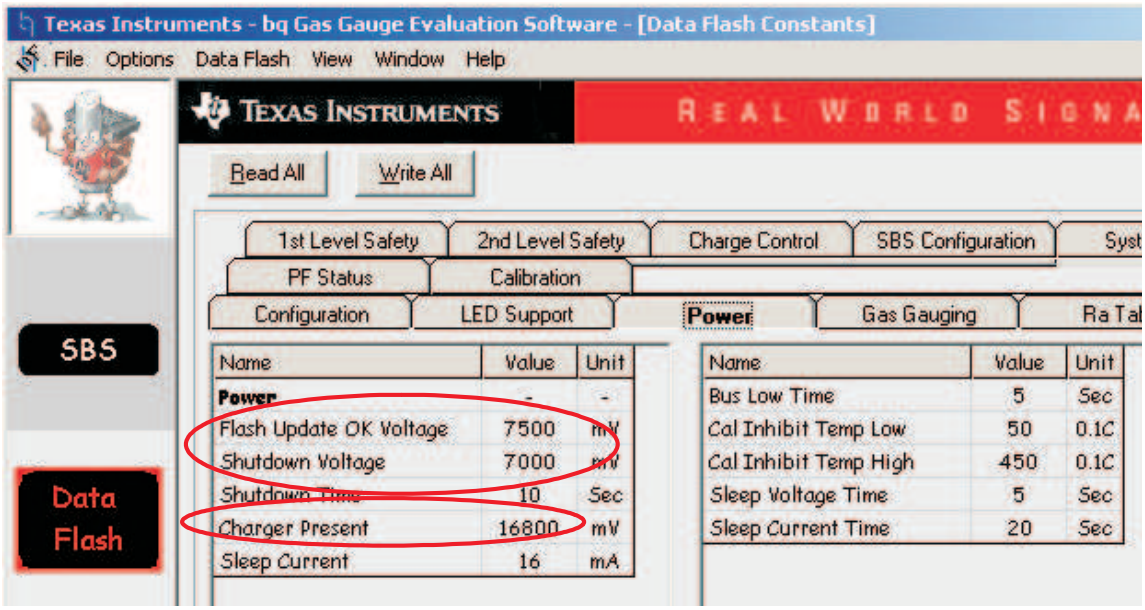
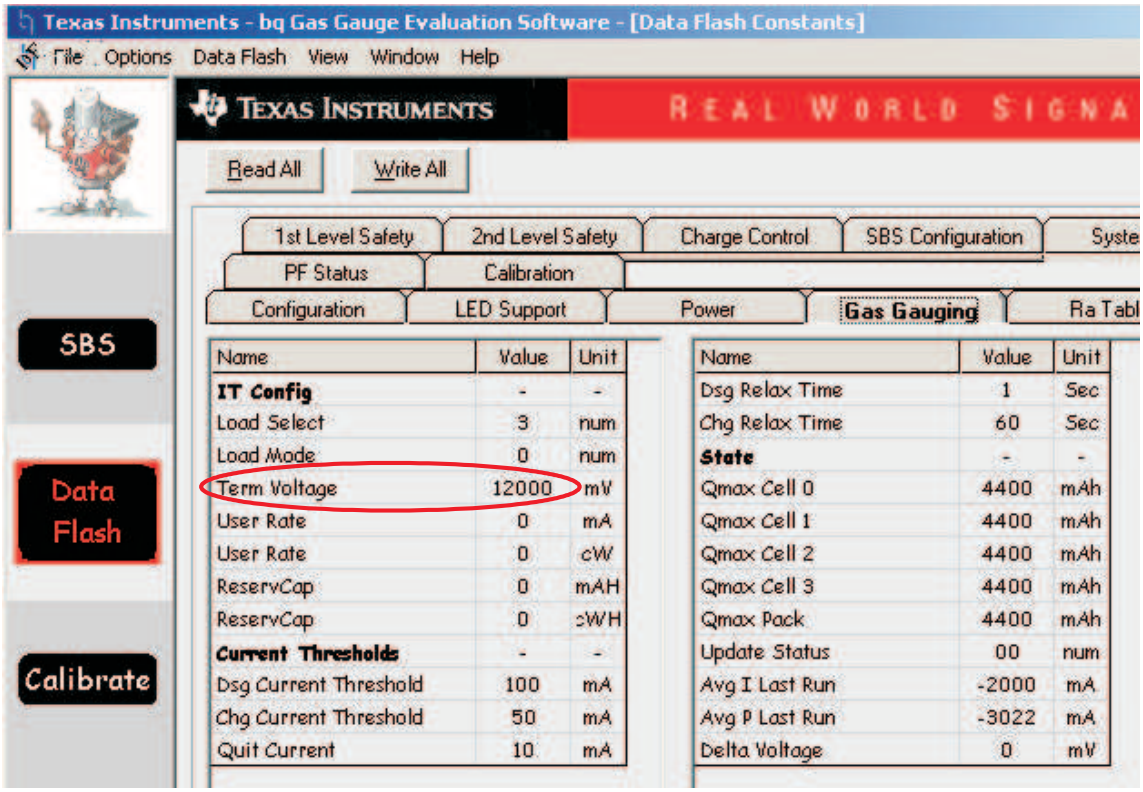


Table 20. Gas Gauging

Setting	2-Cell	3-Cell	4-Cell (Default)
Term Voltage	6000	9000	12000



6.2 Changes to Capacity settings

The pack capacity depends on the individual cell capacity and on the number of parallel cells. The cell-capacity value found in the cell-manufacturer data sheet is used only as an initial estimate for the gas-gauging algorithm, and is updated during operation.

Gas Gauging

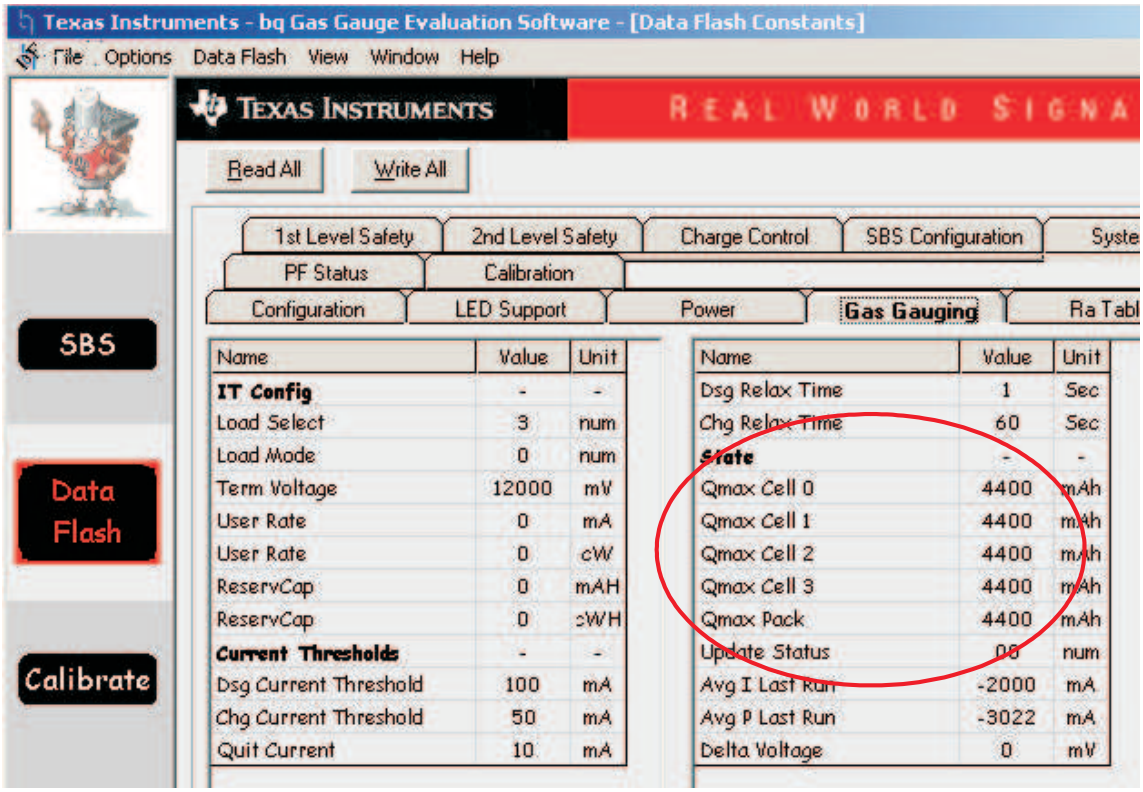
The Qmax of all serial cells (Qmax Cell 0 to 3) is set initially to equal values. The same value is assigned to Qmax Pack. The value to be assigned is calculated as

Qmax = Data sheet Cell Capacity × Number_parallel_cells.

Example: The default assumes 2200-mAh cells Following are the required changes to the 4s2p default values if 2400-mAh cells are actually used..

Table 21. Gas Gauging

Setting	1p with 2400 mAh	2p with 2200 mAH (Default)	3p with 2400 mAH
Qmax Cell 0	2400	4400	7200
Qmax Cell 1	2400	4400	7200
Qmax Cell 2	2400	4400	7200
Qmax Cell 3	2400	4400	7200
Qmax Pack	2400	4400	7200



SBS Configuration

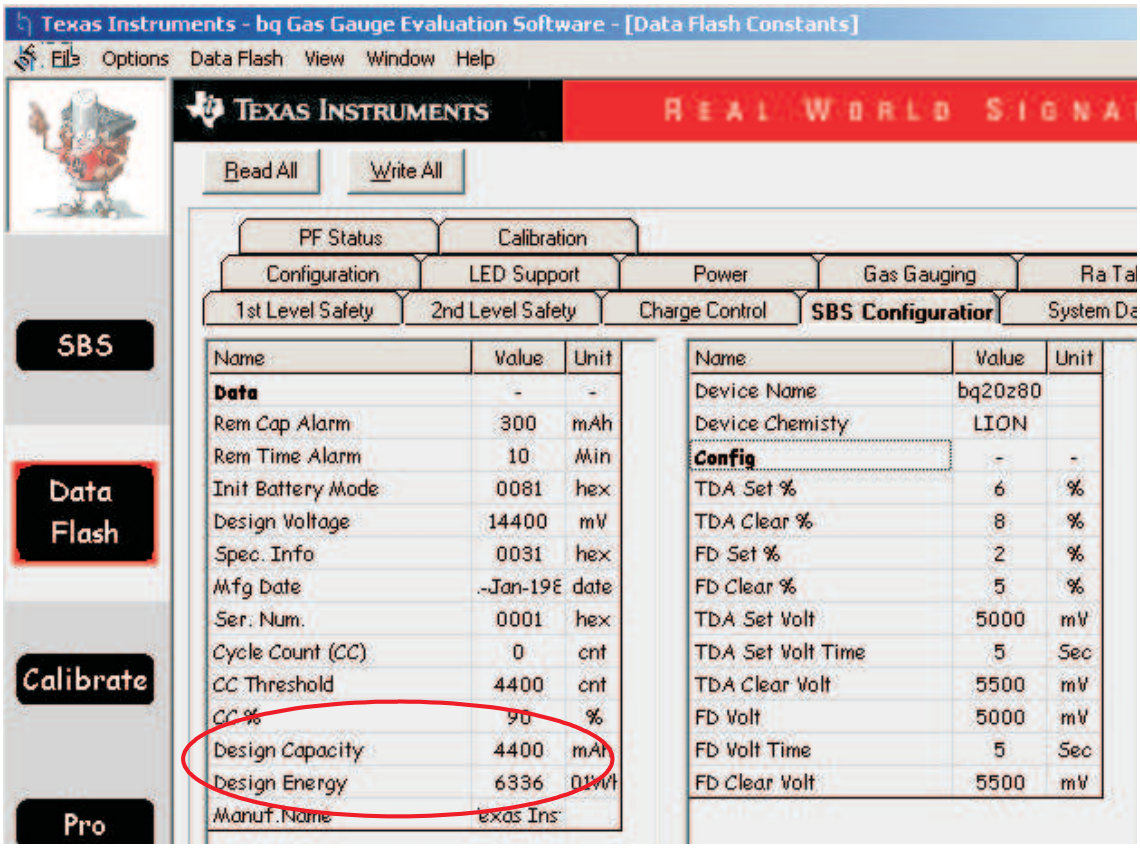
Design Capacity is set to the same number as Qmax. Design energy (centi-Watt) is calculated as

Design Energy = Design Capacity × Number_Serial_Cells × 3.6 V ÷ 10

Example: The default assumes 2200-mAh cells. Following are the required changes to the 4s2p default if 2400-mAh cells are actually used.

Table 22. Gas Gauging

Setting	1p with 2400 mAh	2p with 2200 mAH (Default)	3p with 2400 mAH
Design Capacity	2400	4400	7200
Design Energy	3456	6336	10368



Design Capacity and Design Energy are not used in the gas-gauging algorithm, except for reporting absolute state of charge (ASOC) and state of health, so they do not influence gas-gauging accuracy. Actual capacity depends on the rate of discharge. If a more-accurate setting of design capacity and energy is desired, it should be measured at a discharge rate typical for the target application. The learned FCC value from gas-gauging of a new battery pack at a typical rate can be used as a good estimate of design capacity.

Data Flash Programming Using the EV Software

This document applies to users that require a small quantity of battery packs for evaluation. For mass production methods, see *Using the BQTester Software* (SLUA352) and *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* (SLUA355).

Values of data-flash parameters are determined based on bq20z80 data sheet (SLUS625). In most cases, the default settings are sufficient, while the most commonly changed values are described in *bq20z80 EVM Data Flash Settings for Num of Serial Cells/Pack Cap* (SLVA208).

7.1 Manually changing a value of data-flash constant

1. Apply voltage of about 16 V between Pack+ and Pack- pins to power up the PCB.
2. Connect the EV2300 board, and start the EV Software.
3. Go to the "Data flash" screen.
4. Find the class containing the required data-flash parameter, for example "1st Level Safety".
5. Find the required parameter in the class, for example “POV Threshold”.
6. Type the new value directly into the table, and press enter.
7. Repeat with other constants if needed.

7.2 Saving the data-flash for use with other packs

1. While in the data-flash screen, use the File-→ Export menu to save the data-flash to a (*.gg) file

7.3 Loading previously saved data-flash constants from a file

1. While in the data-flash screen, use File-→ Import menu to load the data-flash from a (*.gg) file into program memory.
2. Push the “write all” button to write all values into the bq20z80 data-flash.
3. If existing calibration values in bq20z80 are to be preserved rather than overwritten with the values from the file, use the “Write All, Preserve”→ Calibration button instead.
4. Go to the “SBS Screen” and send the “Reset” command (Manufacturer Access 0041) to be sure that all settings go into effect.

Calibration Using EV Software

This document applies to users that require a small quantity of battery packs for evaluation. For mass production methods, see *Using the BQTester Software* (SLUA352) and *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* (SLUA355).

The procedure for calibration is different for PCBs and PCBs with cells attached. Calibration before cells are attached is recommended because this method is much faster. When cell are attached, long relaxation periods between the steps are needed to avoid errors with gas-gauging.

8.1 Calibration of the board if cells are not attached

Before calibration:

- Make all the necessary data flash settings to configure the pack. Send the “Reset” command (Manufacturer Access 0041).
- Do NOT send the “IT enable” command 0021 before the calibration, because it starts the gas-gauging algorithm with an uncalibrated pack.

1. Connect 1N (lowest cell (-)), 1P, 2P, 3P and 4P (highest cell (+)) terminals with 470 Ω, 1% resistors to emulate the cells. Apply voltage in the 16 V range between 1N and 4P.
2. Momentary short 4P and Pack+ pins to wake-up the gas-gauge from shut-down mode. Connect the EV2300 to the board and start the EV Software.
3. Current Offset Calibration
   - Enter the “Calibrate” screen.
   - Check the “CC Offset calibration” (uncheck all other boxes).
   - Push the “Calibrate part as indicated below” button.
   - Note that when SMB lines are disconnected, current offset is auto-calibrated to a more accurate value.
4. Voltage Calibration
   - Use a digital volt meter with better than 1-mV accuracy to measure voltage between the 1N and 4P pins. Do not rely on the accuracy of the applied voltage, accurate measurement of the "actual_voltage" is critical.
   - Enter the measured value into the “Enter actual voltage” text-box in the Voltage Calibration section of the “Calibrate” screen.
   - Enter the correct serial cell count (for example 3)
   - Check the “Voltage calibration” check box (uncheck all other boxes)
   - Check the “FET Control”→ OFF radio-button.
   - Push the “Calibrate part as indicated below” button.
   - Note that due to digital filter settling time, full accuracy of reported voltage are reached 5 minutes after calibration. Only after passing this time, comparisons between requested and reported voltage should be done to evaluate calibration accuracy.
5. Pack Voltage calibration
   - This step is optional. The default pack voltage calibration accuracy is sufficient for the purposes of raw pack voltage estimation.
   - Push the “Pack Voltage Calibration” button.
6. Temperature Calibration
   - Measure the temperature using an external temperature measurement means.
   - Enter the measured value into the “Enter actual temperature” text box.

- Check the “Temperature calibration” check box (uncheck all other boxes).
- Push the “Calibrate part as indicated below” button.

7. Current Gain Calibration
   - Connect a power supply in series with a digital ammeter with better than 1-mA accuracy between the 1N and Pack- (e.g. across the sense resistor). Set the voltage so that current is 2 A.
   - Take the actual current reading from the ammeter.
   - Enter the actual current reading into “Enter actual current” text box.
   - Check the “Pack current calibration” check box (uncheck all other boxes).
   - Make sure that in the “FET Control” selection group, “OFF (bypassed)” is selected.
   - Push the “Calibrate part as indicated below” button.
   - Note that after calibration is finished, FETs turn OFF
8. CC Board Offset calibration

   Board offset calibration has a marginal effect on current measurement accuracy. It is critical only if performing the CC Offset calibration current is not reported as zero in no-load conditions. Board offset calibration should not be done at every pack during production because of long required time to achieve accurate results, but instead used for lab characterization of several packs. After which, the average value is used as the fixed data-flash value in all production boards

   To achieve the best value of the board offset calibration, the following steps are needed:

   a. Power-up the PCB through Pack+ and Pack- terminals. There should be no current flowing through sense resistor, e.g. FETs should be off.
   b. Connect the SMB lines, using EV Software read data-flash to get an initial reading of all calibration constants.
   c. Cause the gas-gauge to perform the CC offset auto-calibration by disconnecting SMB-lines for 30 seconds or longer.
   d. After reconnecting the SMB-lines, read the data-flash again, check that the calibration has taken place by observing changes of the CC offset value in the "Calibration" section of the data flash.
   e. To obtain the first estimate of board offset calibration value, enter the "calibration" screen, and push the "CC Board offset calibration" button.
   f. To observe accuracy of calibration, set the "Deadband" value in the "Calibration" section of the data-flash to zero, and observe the reported SBS current. If it reports 0 or -1 (or fluctuates between the two), calibration is sufficiently accurate.
   g. If the reported value is higher or lower, fine-tune the "Board offset" value by manually changing it until SBS current reports 0.
   h. Reset the "Deadband" value to 3.
   i. After repeating steps 1-8 for 5-10 boards, take the average value and use it as a fixed data-flash constant to program into all the boards of the same layout during production.

8.2 Calibration if cells are attached

Making calibrations after cells are attached is not recommended because it is more complex and requires a longer time for providing sufficient cell relaxation after disturbance by current. However, if it cannot be avoided, calibration on assembled pack is done as follows:

1. Before calibration
   - Make all the necessary data flash settings to configure the pack. Send the “Reset” command (Manufacturer Access 0041).
   - Do NOT send the “IT enable” command 0021 before the calibration, because it starts the gas-gauging algorithm with uncalibrated pack.
2. Remove any external power.

   Remove any external power connected to Pack+ and Pack-. There should be no charge or discharge current flow to battery for at least 30 minutes prior to calibration because the cell voltage has a long relaxation period after such events. For the same reason, the Current Gain calibration should be done as the last calibration step.
3. Current Offset Calibration
   - Enter the “Calibrate” screen.
   - Check the “CC Offset calibration” (uncheck all other boxes).
   - Push the “Calibrate part as indicated below” button.
   - Note that when the SMB lines are disconnected, the current offset is recalibrated.

4. Voltage Calibration
   - If there is physical access to the Cell+ and Cell- terminals, turn ON the FETs to make voltage measurements. If physical access is available, skip this step

     To enable charge and discharge FETs, in the “Pro” screen, use the “Write SMB Word”, command 46, Word: 0006.
   - Use a volt meter with better than 1-mV accuracy to measure voltage between Pack+ and Pack- terminal.
   - Enter the measured value into “Enter actual voltage” text-box in the Voltage Calibration section.
   - Enter the correct serial cell count (for example 3).
   - Check the “Voltage calibration” check box (uncheck all other boxes).
   - Push the “Calibrate part as indicated below” button.
   - Note that due to digital filter settling time, full accuracy of reported voltage is reached 5 minutes after calibration. Only after passing this time, comparisons between requested and reported voltage should be done to evaluate the calibration accuracy.
5. Pack Voltage calibration
   - This step is optional. The default pack voltage calibration accuracy is sufficient for the purposes of raw pack voltage estimation.
   - Push the “Pack Voltage Calibration” button.
6. Temperature Calibration
   - Measure the temperature using an external temperature measurement means.
   - Enter the measured value into “Enter actual temperature” text box.
   - Check the “Temperature calibration” check box (uncheck all other boxes).
   - Push the “Calibrate part as indicated below” button.
7. Current Gain Calibration
   - Enter the “Pro” screen in the EV Software, enable charge and discharge FETs using the “Write SMB Word”, command 46, Word: 0006
   - Use electronic load to apply discharge current of 2 A through the 1-mA accurate amperometer attached in series between Pack+ and Pack-.
   - Take the actual current reading from the amperometer.
   - Enter the actual current reading into the “Enter actual current” text box.
   - Enter the actual current reading into the “Enter actual current” text box.
   - Check the “Pack current calibration” check box (uncheck all other boxes).
   - Make sure that in the “FET Control” selection group, the “ON (External Load) is selected.
   - Push the “Calibrate part as indicated below” button.
   - Note that after calibration is finished, FETs turn OFF
8. CC Board Offset calibration

   This calibration should not be done at every pack during production because of long required time, but used for lab characterization of several packs. After which, the average value is used as the fixed data-flash value in all production boards. If cells are attached, it is preferable to use the previously defined on-board-level board offset value.
9. Calibration is complete

   Wait 30 minutes to let cells relax after being disturbed by the current during “Current Gain Calibration” and send the Manufacturer Access Command 0021 to enable the gas-gauging and turn-on FETs

Basic Pack Assembly Using an EVM or User-Made PCB

1. It is assumed that the PCBs have been preprogrammed with the correct data-flash values, and calibrated as described in this document.
2. Connect the lowest (-) of the serially connected 4-cell battery stack to 1N PIN of TB3 – TB2 connector.
3. Connect the second lowest cell (+) to 1P.
4. Connect the third lowest cell (+) to 2P.
5. Connect the forth lowest cell (+) to 3P.
6. Connect the highest (+) of the battery stack to 4P.
7. Connect the external power (from 6 V to 16.8 V) to the Pack+ and Pack- terminals on TB1 and TB4 connector to wake up the EVM from shut-down mode
8. Connect the SMBus connector (J1) to the EV2300 adapter, start the EV Software.
9. Fuel-gauging. Go to the “Pro screen” in the EV Software. Make sure that the “Write SMB Word” section reads: SMB Command: 00 Word (hex): 0021, and push the “Write” button
10. Go to the SMB Screen and check that the IT is enabled. Look inthe “Flags/Status bits” of the “Operation Status”. The QEN bit should be set (red). Also, the “Relative State of Charge” value is now updated to the correct value that corresponds to the state of charge of the cells.
11. Pack is ready. Emulate insertion into system by shorting the “Sys. pres” (System Present) and “VSS” pins on the TB1 – TB4 connector. Discharge and charge FETs that are ON (as indicated by value of 0006 in the “FET Status” field in SMB Screen of EV Software), and start the charge/discharge tests.
12. Step 11 not required if the “non-removable” configuration is chosen by setting NR=1 in the Op.Config B. In this example, the system is always considered present.
13. In production, the data-flash constants used should be optimized (Update Status = 6), so no learning is needed.
14. For evaluation that uses the default data-flash constants, correct self-learning of all model parameters is recommended for the first cycle as follows: Charge to full, let it rest for 2 hours, discharge to empty, let rest for 5 hours. During this first cycle, the model of your cells is created by the gas-gauge and is self-updated during normal operation. Two cycles are recommended for full accuracy. See more details on acquiring optimized parameters in (SLUA334).

Preparing Optimized Default Flash Constants for Specific Battery Types

PMP Portable Power

ABSTRACT

Impedance Track™ gas gauge technology allows bq20z80 gas gauge ICs to automatically acquire and maintain parameters for battery modeling needed for continuous gas-gauge accuracy, regardless of battery model or manufacturer. This application report discusses how to prepare optimized default flash constants for specific battery types.

10.1 Introduction

Impedance Track™ gas gauge technology allows bq20z80 gas gauge ICs to automatically acquire and maintain parameters for battery modeling needed for continuous gas-gauge accuracy, regardless of battery model or manufacturer. These ICs are pre-programmed with default values for these parameters. During daily use (charged, discharged, or unused), new parameters specific for a given battery are collected by the algorithm.

The default parameters that are used for gas gauging prior to discharge activity provide a high level of gas gauge accuracy. However, to maximize the accuracy and reach a 99% or better level, a full update of parameters is required. Therefore, before the first discharge cycle, the accuracy of the gas gauge is less than the 99% accuracy that is achieved after parameter acquisition. A full set of parameters is acquired when the battery completes one full discharge cycle and subsequent relaxation takes place.

In order to ensure maximum accuracy in new battery packs before any discharge activity occurs, make a discharge cycle on one battery pack (let it acquire optimized parameters), save the configuration file with optimized parameters, and then program it into all new battery packs whose cells came from the same supplier. The following sections describe how to create a configuration file with optimized parameters and program them into battery packs during production.

10.2 Creating Pre-Learned Defaults

- Assemble a battery pack with a bq20z80 solution (see application report *Pack Assembly and the bq20z80*, literature number SLUA335). Set the appropriate Data-Flash constants, calibrate, and assemble the pack as described in this document.
- Charge the pack to full.
- Let it relax for 2 hours.
- Discharge the pack to minimal device acceptable voltage (also set as *Term Voltage* flash constant), at a typical rate for the target application. The exact rate is not critical.
- Let it relax for 5 hours.
- Repeat steps 1 - 5 one more time to achieve the best resistance accuracy.
- Start EV Software for bq20z80.
- Enter *Data Flash* window, and push *Read Flash* button.
- Check in *Gas Gauging* tab that *Update Status* shows *06* which means that the pack has acquired all parameters. If not, repeat the cycle.
- In *File* menu, click *Export*, and chose a (*.gg) file name for saving the pre-learned defaults, for example, (optimized.gg).
- Open the saved file in a text editor such as Notepad, and change the value of *Update Status* from 06 to 02, which indicates that the parameters are learned but the Impedance Track™ feature is disabled (as it should be in a new pack before calibration). Also, the cycle number in SBS Configuration is changed to 0.
- The new defaults are now ready.

10.3 Production Flow With New Defaults

Use of the bqTester (or user supplied software derived from the open-source bqTester code) is recommended for a fast production process. See *Using the BQTester Software* (SLUA352) for details on how to use the generated (.gg) file for production. Alternatively, user supplied software can be used as described in chapter *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* (SLUA355).

If using the EV Software for making a limited number of packs for evaluation, follow this procedure:

- If using a chemistry different from the default, program firmware specific for your chemistry.
- At the step where flash constants are set:
  - Open the EV Software, and go to the *Data Flash* window.
  - Use the menu File→Import and select the optimized.gg file.
  - Push the *Write All* button to write constants to flash memory.

  - In the SBS window, send *reset* (manufacturer access command 0041)
- Perform CC Offset, temperature voltage, and current calibration as described in the *Calibration Using EV Software* (SLUA386).
- Connect battery cells to PCB.
- Enable the Impedance Track™ technology by going to *Pro screen* in EV Software. Make sure that *Write SMB Word* section reads:
  - SMB Command: 00 Word (hex): 0021 – and push *Write* button.
- Now the pack is configured and ready for further evaluation / testing.

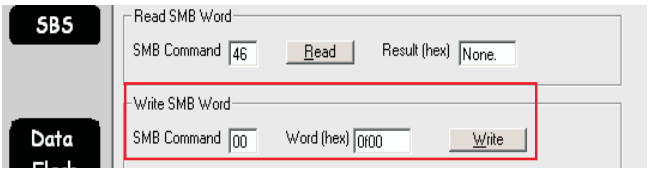
Updating Firmware With The bq20z80 and EVM

Garry Elder *Battery Management*

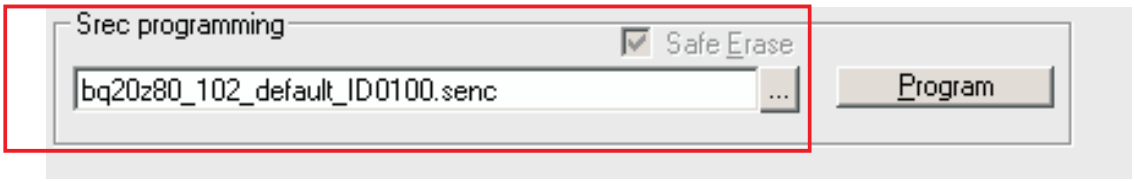
The following the steps are used to update the bq20z80 firmware in the EVM:

1. Power up the EVM by applying 16 V between Pack+ and Pack-. This step is not necessary if the cells are already attached.
2. Start the EV Software. Ignore the wrong-version warning about (press OK)

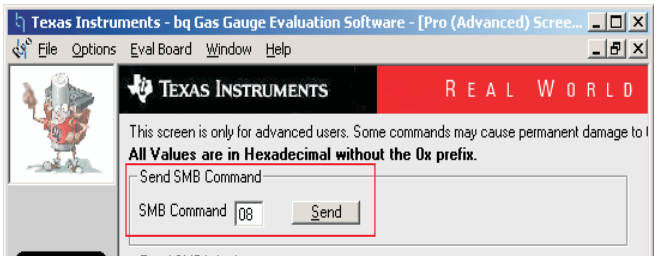
3. Navigate to the *Pro* screen.
4. Enter ROM mode by setting the *Write SMB Word* section to read: "SMB Command: 00 Word (hex): 0f00", and click the *Write* button.



5. In the *Srec programming* screen enter the path and file name for the new firmware file (*.senc). If needed, click the (…) button to browse for the file location.



6. Click the *Program* button to program the firmware. All flash-constants information including calibration will be lost, so it should be exported beforehand into a (*.gg) file.
7. Once programming is finished, execute the program by sending SMB command 08. Navigate to the *Send SMB command* screen, enter 08 in the *SMB Command* box, and push the Send button.



8. Restart the EV Software so the new version of firmware is recognized.

Using SHA-1 in bq20zxx Family of Gas Gauges

Travis Neely *PMP Portable Power*

ABSTRACT

The bq20zxx Impedance Track™ family of gas gauge ICs includes a highly sophisticated authentication algorithm, known as SHA-1, which requires little setup and development time and provides an effective, secure battery design.

12.1 Introduction

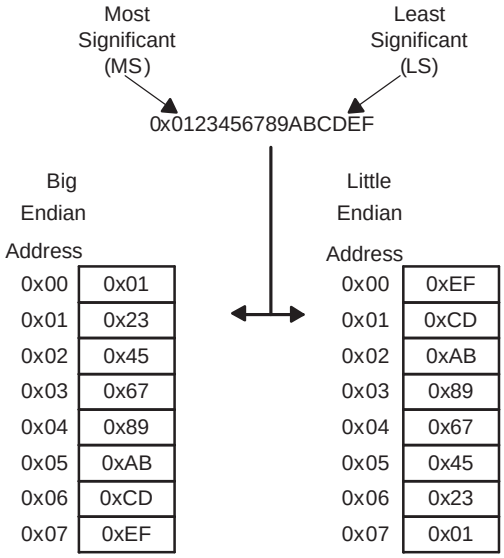
Battery counterfeiting is a major problem confronting original equipment manufacturers (OEM) today. One of the most effective methods to counter this issue is with the use of SHA-1 authentication routines in battery designs. Using this approach ensures that the OEM can track the suppliers for battery replacements. With this anti-counterfeiting algorithm, only battery packs manufactured by authorized subcontractors using the bq20zxx Impedance Track™ gas gauge IC with the SHA-1 can be integrated into OEM system designs. The SHA-1 authentication key in the bq20zxx can be regulated and tracked by the OEM. Multiple subcontractors can be supplied with different authentication keys for even greater security and regulation

12.2 Explaining Little Endian

The SHA-1 features of the bq20zxx use SMBus string reads and writes. Because SMBus communications is based on the Little Endian scheme of byte ordering, an understanding of Little Endian can reduce the complexity of the development process.

Two, byte-ordering schemes are used when storing multibyte data in memory: Little Endian and Big Endian. In Big Endian ordering, the most significant byte (MSB) is stored at the lowest possible memory address. This ordering method is most routinely used in Motorola processors.

In Little Endian ordering, the least significant byte (LSB) is stored first in memory at the lowest address. Little Endian is used in Intel processors. It is also used by the SMBus data transfer method for multibyte data transfers. In other words, SMBus always transfers the LSB first.



What is SHA-1?

This document describes the SHA-1 functions only as they are used with the bq20zxx gas gauge IC. More complete explanations of the SHA-1 algorithm are available in many articles and books. For example, see www.faqs.org/rfcs/rfc3174.html for an excellent description of the SHA-1 algorithm and some C-code examples of how to implement it.

Three primary bq20zxx functions are used to implement the SHA-1 security feature in a system design. The first function is the SHA-1 challenge. The challenge is a 20-byte (160-bit) string sent to the bq20zxx by the host. The SHA-1 algorithm in the bq20zxx then is required to send back a response. The 20-byte challenge, located at SMBus command 0x2f is a 20-byte SMBus string write. As with the rest of the SHA-1 function, this challenge string is Little Endian.

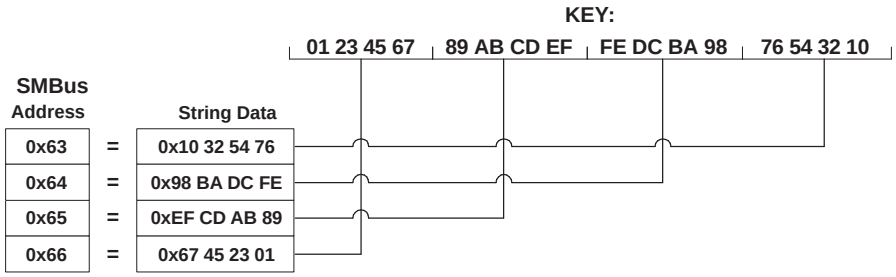
The second bq20zxx function used to implement the SHA-1 feature is the SHA-1 response. The response is a 20-byte string read. Once a challenge is given and the bq20zxx is given time to compute the response, it is available in the same SMBus command as the challenge (command 0x2f).

The third function is the SHA-1 authentication key. The authentication key is the primary function of the SHA-1 algorithm. The key is input during production only by using the *Gold Data Flash File* methodology explained in a later section entitled *How to Set Up for Production*. Once the key is written and the part sealed, it is completely inaccessible. It must be kept secret. With the key unknown, it is virtually impossible for the challenge/response pattern to be decoded. If the key is compromised, the authentication is no longer effective.

How to Use SHA-1 in the bq20zxx

The following two steps are used to implement the SHA-1 algorithm in the bq20zxx.

1. **Create a unique authentication key, and write it to the part during assembly: The authentication key resides in the SMBus addresses 0x63-0x66 in 4-byte strings. The four strings are read/write accessible until the bq20zxx is sealed. When written using an SMBus string write command, they are retained permanently in flash memory and can only be changed when the bq20zxx is unsealed. They are stored in Little Endian format as shown in the following diagram. The SHA-1 authentication key defaults to *0123456789abcdeffedcba9876543210* in the bq20zxx. This is a default and is not intended for production. It should be changed to a unique key prior to production to ensure that security is not compromised.**



2. **Implement SHA-1 in the OEM host system.**
   a. **The host has to know the SHA-1 authentication key:**
   The host must know the key defined in step 1. This key is used in the host system to determine what the response should be.
   b. **The host has to issue a random challenge:**
   The host sends a challenge using a 20-byte string write to SMBus command 0x2f in Little Endian format. It is important that the challenge be random every time to ensure security. Here is an example of a challenge and writing it in Little Endian:

   Using the example of:

0x20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 3E 2F 30 31 32 33

   Must be written in Little Endian as follows:

0x33 32 31 30 2F 2E 2D 2C 2B 2A 29 28 27 26 25 24 23 22 21 20

   c. **The host computes the response:**
   With the known SHA-1 authentication key and random challenge, the host computes the anticipated response from the bq20zxx.

d. **Bq20zxx computes the response:**
The bq20zxx computes the response at the same time that the host is computing it. The bq20zxx should be given greater than 100 ms to compute the response and put it into memory for retrieval.

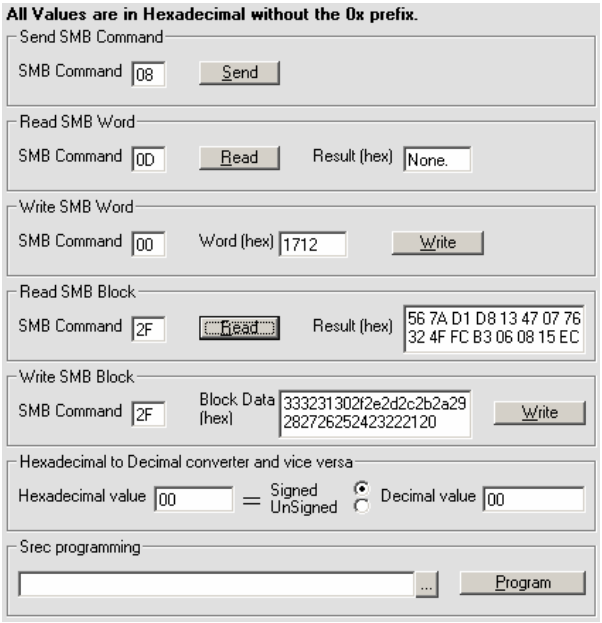
e. **The host has to read the response:**
The host reads a response from the same command (0x2f) to which the challenge was written. The response is a 20-byte string read in Little Endian format.

f. **The host must validate the response:**
The host must compare the response read from command 0x2f in the bq20zxx to what was computed in step *2c*.

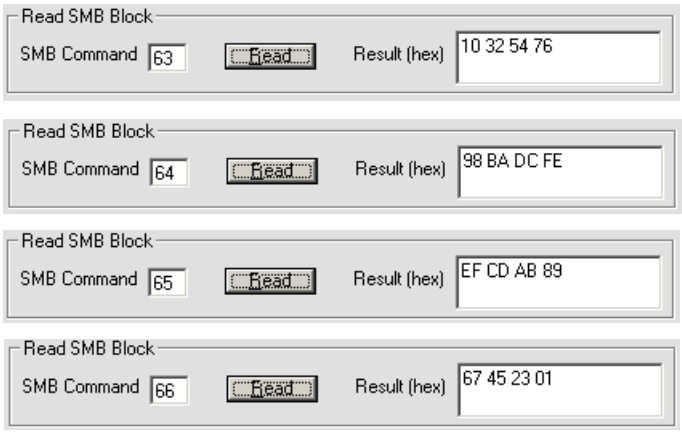
g. **If the response is validated, then the battery is authorized. Otherwise, the host can reject the battery pack.**

Experimenting With the bq20zxx Evaluation Software:

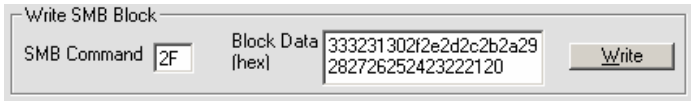
The PRO screen of the bq20zxx Evaluation software can be used to experiment with the SHA-1 features. This screen includes the SMBus read and write block functions that are required for SHA-1. Use the procedure described in the preceding section entitled *How to Use SHA-1 in the bq20zxx* with the following functions:



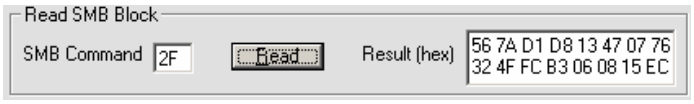
1. **Use the Read SMB Block frame to verify that the key is written to the desired value using the four reads to SMBus commands 0x63-66. They should read as follows by default. Notice that they report in Little Endian.**



2. **If the authentication key needs to be changed, it can be modified with an SMBus write to the same SMBus commands 0x63-66 in Little Endian.**
3. **Now, write the challenge in Little Endian to the bq20zxx using the Write SMB Block Frame:**



4. **Then, use the Read SMB Block Frame to read the Response from the bq20zxx:**



5. **Notice that only 16 bytes fit in the Read SMB Block Frame. The entire response is in the Result window but not wholly visible. Select and highlight the Result data and paste it into a text editor to see the entire result as follows:**

56 7A D1 D8 13 47 07 76 32 4F FC B3 06 08 15 EC 23 5C AB FE

How to Set Up for Production:

Setting up the SHA-1 for production assembly is simple using the BqTester *Gold Data Flash File* methodology for testing production modules. See *Using the bqTester Software* (SLUA352) application report or *bqMulti-Site Tester* user guide at www.ti.com for more information.

Using the bq20zxx EV software, set up the module as required for the application. Many of the TI documents in the corresponding bq20zxx IC product folder at www.ti.com can assist the user in setting up the module. As an example, for the bq20z80, these include:

- *Preparing Optimized Default Flash Constants For Specific Battery Types* application report (SLUA334)
- *bq20z80 EVM Data Flash Settings for Number of Serial Cells and Pack Capacity* application report (SLVA208)
- *Pack Assembly and the bq20z80* application report (SLUA335)
- *Exploring the bq20z80 Impedance Track Evaluation Kit* application report (SLUA351)
- *Pack Assembly and the bq20z80* application report (SLUA335)

Once a module is configured as required for the particular application, the desired SHA-1 authentication key needs to be saved into the bq20zxx module as explained in the previous section *How to Use SHA-1 in the bq20zxx*. With this completed, the SHA-1 key is stored, and the data flash meets the requirements for the *Gold Data Flash File*.

As explained in *Using the bqTester Software* application report or the *bqMulti-Site Tester* user guide, create the *Gold Data Flash File*. Use this file with bqTester or bqMulti-Site Tester Software for module testing in production. Be sure to seal the bq20zxx as explained in the corresponding bq20zxx data sheet. All modules produced with this *Gold Data Flash File* and bqTester or bqMulti-Site Tester will have the same hidden SHA-1 key and be ready for use.

bq20z80 to bq20z80-V101 Change List

Garry Elder *Battery Management*

ABSTRACT

This document describes the design considerations required to change a bq20z80 design to a bq20z80-V101 solution. The latest ordering information, data sheet, and application reports can be found on the World Wide Web at:http://power.ti.com.

13.1 Introduction

The bq20x80-V101 firmware upgrade has been released to enable several feature additions and corrections. New orderable part numbers have been released to support this firmware upgraded device:

– bq20z80DBT-V101

– bq20z80DBTR-V101

To be able to read and write all the data flash configuration locations, the latest version of the evaluation software is required.

13.2 Change Details

CHANGE	bq20z80	bq20z80-V101	COMMENTS
Added authentication (optional SBS command 0x2f)	Command 0x2f has no function and is not acknowledged.	Command 0x2f is the *SBS.Authenticate( )* command to the bq20z80 to begin the SHA1 authentication.	Additional feature to enable host to authenticate the battery
Added Cell Balancing	Cell balancing not available	Added State of Charge cell balancing algorithm	Additional feature to enable longer lifetime of battery
Added charge fault FET Enable register	When charge faults occur, FET action is taken.	When charge faults occur, FET action is taken if enabled in *DF:FET Enable* register.	Adds flexibility to system interaction
Added pulse compensation for end of discharge	Applications with pulsed current loads and minimum voltage requirements can have less RemainingCapacity than reported.	The voltage pulses caused by pulsed current loads are measured and used to better estimate RemainingCapacity.	Added additional feature to improve capacity prediction
Added *SBS.BatteryStatus( ) [TDA, FD]* voltage thresholds	*SBS.BatteryStatus( ) [TDA, FD]* are only set on SBS.RSOC, detection of charge termination or faults	*SBS.BatteryStatus( ) [TDA, FD]* are now set and cleared based on *SBS.Voltage( )*	Adds flexibility to system interaction
Added option for LEDs in series with current source	LED display is only in parallel.	LED display is available in series (with current source) or parallel.	Adds capability for higher brightness LED's
Configured pin 7 as active high fuse blow	Pin 7 is not connected.	Pin 7 is now an active high reflection of $\overline{\text{SAFE}}$ (pin 12).	Adds flexibility to choose different circuits driven by the permanent failure signal
Added State of Health calculation (command 0x4f)	Command 0x4f has no function and is not acknowledged.	Command 0x4f is the *SBS.StateOfHealth( )* command where SOH is the ratio of *SBS.DesignCapacity( )* to *SBS.FullChargeCapacity( ).*	Additional feature to allow host to easily determine health of the battery
Added Synchronization of *SBS.RemainingCapacity( )* to *SBS.FullChargeCapcity( )* at charge taper termination.	*SBS.RemainingCapacity( )* is not affected and could be < 100% at charge termination.	If DF:Operation Cfg [RMFCC] is set then *SBS.RemainingCapacity( )* is updated to the value of *SBS.FullChargeCapcity( )* at charge termination.	Adds option to enable charge synchronization in order to display RelativeStateOfCharge as 100% at charge termination

CHANGE	bq20z80	bq20z80-V101	COMMENTS
Improved thermal model	A preliminary thermal mode was used.	An updated thermal model is used.	Improved thermal compensation of Impedance Track™ algorithm
Improved cell capacity measurement by limiting valid temperature ranges	Valid voltage measurements for cell capacity estimation can occur at any temperature.	Valid voltage measurements for cell capacity estimation must occur within a defined temperature range.	Improves capacity estimation
Improved cell capacity measurement	After a full reset, it may take several minutes for voltage reading to settle to the most accurate reading.	Settling time of voltage measurements after a full reset is reduced.	Improves initial voltage reading accuracy
Improved default resistance tables	A preliminary default resistance mode was used.	An updated default resistance mode is used.	Improved thermal accuracy of Impedance Track™ algorithm
Prevented lifetime updates until IT is enabled	Data flash lifetime data is updated under all conditions.	Data flash lifetime data is not updated until Impedance Track™ is enabled.	Improves suitability of lifetime data
Aligned SBS.RemainingCapacity( ) with *DF:Terminate Voltage*	*SBS.RemainingCapacity( )* could be above zero when *SBS.Voltage( )* reaches *DF:Terminate Voltage.*	Forces *SBS.RemainingCapacity( )* to zero when *SBS.Voltage( )* is below terminate voltage	Improves alignment between reporting and system status
Disabled LEDs for undervoltage conditions	When *SBS.OperationStatus( )* [CUV or PUV] is set, then the LED display could be activated.	When *SBS.OperationStatus( )* [CUV or PUV] is set, the LED display is disabled.	Reduces risk of deeply discharging the battery
Clear *SBS.BatteryStatus( ) [RCA]* when not *SBS.BatteryStatus( ) [DSG]*	*SBS.BatteryStatus( ) [RCA]* is not cleared when *SBS.BatteryStatus( ) [DSG]* is cleared.	*SBS.BatteryStatus( ) [RCA]* is now cleared when *SBS.BatteryStatus( ) [DSG]* is cleared.	Corrected to meet SBS specification
Allowed sleep mode for undervoltage conditions	When *SBS.OperationStatus( )* [CUV or PUV] is set, then entry to sleep mode is disabled.	When *SBS.OperationStatus( )* [CUV or PUV] is set, then entry to sleep mode is allowed.	Reduces risk of deeply discharging the battery
Improvements made to Lifetime data	Does not save maximum and minimum lifetime AverageCurrent or AveragePower. Only saves lifetime data when new values exceed old values by defined delta values	Saves maximum and minimum lifetime AverageCurrent and AveragePower. Lifetime data is saved after a defined period of time even if new values do not exceed old values by defined delta values	Improves lifetime data
Changes made to pulse charging	Voltages for pulse charging are sampled once a second.	Voltages for pulse charging are sampled 4 times a second.	Improves pulse charging
Changes made to charging timeouts	The precharge timeout timer runs when the charging current is below a defined threshold; so, it is possible that the precharge timer will run during charging taper current and cause an undesired precharge timeout during charging taper.	The fast charge and precharge timeout timers only run when precharging or charging, as indicated by FCHG and PCHG bits in ChargingStatus.	Improves operation of fast charge and precharge timeout timers
Changes made to discharge faults	Discharging fault is indicated whenever BatteryStatus [TDA] is set. Current discharging fault is not indicated for current faults detect by AFE. Separate discharging faults are indicated for voltage and temperature.	Discharging fault is indicated for any safety condition resulting in turning off the discharge FET. Current discharging fault is indicated for all detected overcurrent conditions, including overcurrent detected by AFE. Temperature and voltage discharge faults are not indicated separately.	Improves indication of discharging fault conditions
Improvements made to calibration functions	Voltage calibration functions may cause error in voltage calibration of several millivolts.	Voltage calibration functions are capable of accuracy within 1 millivolt.	Improved voltage calibration accuracy
Protect against simultaneous writes to data flash	A SMBus-initiated data flash write may occur at the same time as a data flash write initiated by the AGG, which my cause a data flash write error.	A SMBus-initiated data flash write cannot occur at the same time as any other data flash write.	Increased robustness of data flash writes
Corrected *SBS.ManufacturerAccess( )* access of silicon revision	*SBS.ManufacturerAccess( )* access of silicon revision is not functional.	*SBS.ManufacturerAccess( )* access of silicon revision is functional.	Allows host to determine bq20z80 silicon revision

CHANGE	bq20z80	bq20z80-V101	COMMENTS
Corrected data flash checksum operation	The data flash checksum includes non-accessible portions of the data flash that change when writing the data flash checksum, invalidating the checksum.	The data flash checksum only includes data flash that does not change when writing an updated data flash checksum.	Data flash checksum operation works correctly.
Corrections made to LED display	Fixed LED thresholds cannot be selected.	Fixed LED thresholds can be selected.	Correct operation of LED threshold settings
Erroneous readings are corrected that occurred after offset calibration when sleep mode is not entered.	Erroneous SBS voltage, current, and temperature readings occur after current offset calibration if sleep mode is not entered, corrupting the lifetime data.	No erroneous SBS voltage, current, and temperature readings occur after current offset calibration if sleep mode is not entered.	Improve reliability of lifetime data
Corrected the length of *SBS.ManufacturerData( )* command	*SBS.ManufactureData( )* returned additional data not specified in the data sheet.	Only returns the appropriate data	Correct data set made available to host
Changed DF:Charger Present default voltage to 12000 mV	*DF:Charger Present* default was 16800 mV.	Default changed to 12000 mV.	More realistic default for most applications
Corrected LED display lock-up fault when exiting sleep with LEDs on	LED display locks up if LEDs are ON as the bq20z80 exits sleep mode.	LED display operates normally regardless of power state transitions.	Correct operation of the LED display under all conditions
Added report of any inability to write DFF as flash write error in calibration mode	If writing the data flash is not allowed either due to a permanent failure or low voltage, then no indication is given when attempting to write data flash in calibration mode.	The inability to write data flash in calibration mode is reported as a flash write error.	Improved calibration system interaction
Corrected issue of improperly clearing AFE faults	AFE faults were detected and the pack protected but the fault would be cleared up to three times at an interval of 250 milliseconds before the defined recovery requirements would apply.	AFE faults are correctly handled, including the flags.	Improved system interaction when faults occur
Modified code to save open-circuit voltage (OCV) data on IT enable only, not a full reset	OCV data was saved after a full reset which could have disturbed the OCV measurements if the battery was not in a completely relaxed state.	OCV tables are only updated when IT enabled, or the IT enable command is resent.	Improved OCV data reliability under all system conditions
Corrected range check for calibration of analog-to-digital converter (ADC) offset	In calibration mode, if the measurement ADC offset was out of range, no error would be reported.	In calibration mode, if the measurement ADC offset is out of range, an error is reported.	Improved calibration system interaction
Implemented a validation time for DOD0	There is a possibility of erroneous DOD0 measurement if charge or discharge current occurs at the same time.	DOD0 measurement is not saved unless the battery remains in the relaxed state for a defined time after the DOD0 measurement is made.	More reliable SBS.FullChargeCapacity( ) and SBS.RemainingCapacity under all system conditions
Implemented a bounds limit to a QMAX change	QMAX changes are not limited to filter-bad readings.	QMAX changes are bounds limited to filter-bad readings.	More reliable SBS.FullChargeCapacity( ) and SBS.RemainingCapacity under all system conditions
Implemented a double hit for dv/dt detection for QMAX qualification	The dv/dt qualification for QMAX update requires only one sample to be valid.	The dv/dt qualification for QMAX update requires two samples to be valid.	More reliable SBS.FullChargeCapacity( ) and SBS.RemainingCapacity( ) under all system conditions
Corrected parameter update issue caused by exiting sleep mode during current measurement	If bq20z80 exits sleep during a current measurement, the SBS parameters do not update again until the pack enters and exits sleep mode again.	SBS parameter updates operate normally regardless of power state transitions.	Improved system interaction for sleep mode transitions
Implemented an option to leave charge FET on for a nonremovable pack in sleep mode, enabled by DF:Operation Cfg B [NRCHG].	When DF:Operation Cfg B [NR] is set, then the CHG is turned off at entry to sleep mode.	When DF:Operation Cfg B [NR, NRCHG] are set, then the CHG remains on at entry to sleep mode.	Improved system interaction options

CHANGE	bq20z80	bq20z80-V101	COMMENTS
Modified code such that if QMAX has not been updated, old valid OCV readings are discarded when a new valid OCV reading is detected and the conditions for QMAX update do not exist.	Valid OCV is only discarded when all conditions for QMAX update are satisfied, but the accumulated error in the measured capacity exceeds 1% (default value).	If QMAX has been updated, the same conditions for discarding an OCV reading are the same as for the bq20z80. Otherwise, old OCV readings are discarded and new OCV readings are used when the conditions for a valid OCV reading exist, but the conditions for QMAX update do not exist.	Enables QMAX measurement for full charge or discharge for the first QMAX update, even if initial OCV measurement is made when battery is only partially charged.
Modified code such that if QMAX has not been updated, then for QMAX update to occur, the measured capacity must be greater than or equal to 90% (default value) of design capacity.	The measured capacity must be greater than 20% (default value) or a value as determined from the QMAX update filter constant for a QMAX update to occur.	For the first QMAX, the measured capacity must be greater than 90% (default value) for a QMAX update to occur. If QMAX update has occurred the conditions for measured capacity are the same as for the bq20z80.	Improved QMAX data reliability for the first update of QMAX
Default minimum passed charge for QMAX update has been changed from 20% to 37%	Internal flash value of Min Passed Charge is 20%. The default setting for the QMAX update filter constant of 64 means actual Min Passed Charge for QMAX update is 25%.	Internal flash value of Min Passed Charge is 37%. This 37% is consistent with the QMAX update filter constant of 96.	Improved QMAX data reliability under all system conditions.
Default QMAX update filter constant has been changed from 64 to 94.	Internal flash value of QMAX update filter is 64.	Internal flash value of QMAX update filter is 94.	Improved QMAX data reliability under all system conditions.
QMAX values for nonexistent cells will be updated to Design Capacity.	*DF:Qmax Cell 2..4* written with random values if not used when QMAX is updated	*DF:Qmax Cell 2..4* are updated to = *DF:Design Capacity* if not used when QMAX is updated.	Ensure all QMAX values are reasonable, even if not used

13.3 Summary

The significant changes are to improve system interaction stability and reliability under all system conditions.

bq20z80-V101 to bq20z80-V102 CHANGE LIST

Kalpana Mahesh *PMP - Battery Mangement*

ABSTRACT

This document describes the design considerations required to change a bq20z80-V101 design to a bq20z80-V102 solution. Find the latest ordering information and data sheet on the TI Web site at http://www.power.ti.com.

14.1 INTRODUCTION

The bq20z80-V102 firmware upgrade has been released to enable several feature additions and corrections.

The following new orderable part numbers have been released to support this firmware-upgraded device.

- bq20z80DBT-V102
- bq20z80DBTR-V102

The latest version of the evaluation software is required to be able to read and write all the data flash configuration locations.

To upgrade a previous version of the bq20z80, use the evaluation software available on power.ti.com and find the latest encrypted program in the Web folders. For details on how to update the firmware, see the TI application report SLUA336.

Table 1. CHANGE DETAILS

CHANGE	bq0z80-V102	bq20z80-V101	COMMENTS
Corrected to allow display to turn off when charging and button pushed.	LED display operates correctly during charging.	LED display would stay on until charging terminated after the button was pushed. Only occurs when LED display not configured to be always on during charging.	Correct operation of the LED display under all conditions
Allow negative LED thresholds to permit LED alarms to be disabled	Configuring negative LED alarm threshold disables LED alarm functionality.	Feature not available	Allow better customization
Allow zero values for ALARM and CHARGING LED blink rates to disable them	Configuring zero value for the LED blink rates disables them.	Feature not available	Allow better customization
Restore initialization of dodcharge in relaxed state so that the correct dodcharge value is used in capacity estimation	dodcharge initialized to the correct value	dodcharge value set to zero	Improved gauging accuracy with correct initialization of dodcharge value.
Only clear offset calibration flag when SMBus lines go high.	Prevents offset calibration occurring just because a safety condition occurs and then clears when the SMBus lines are low.	Offset calibration occurs multiple times if safety condition occurs when SMBus lines are low.	More appropriate period between offset calibrations when SMBus lines are low.
Change so that setting AFE Fail Limit to zero disables PF_AFE_C	Configurable option to allow disabling PF_AFE_C trigger	Feature not available.	Allow better customization

Table 1. CHANGE DETAILS (continued)

CHANGE	bq0z80-V102	bq20z80-V101	COMMENTS
Enable LED display to turn off after charge termination and if SMBus lines are detected low and LEDs enabled during charging.	LED display turns off after charge termination.	LED display stays on when charging terminates after SMBus lines are detected low.	Correct operation of the LED display under all conditions
Set charge FET state immediately when entering sleep	Charge FET state set correctly, immediately after entering sleep	The CHG FET would not get set to the correct state for sleep until the first voltage measurement.	Quicker transition of FET to the correct state in sleep
Change *DF:Operation Cfg B [CCT = 0]*, so that *SBS.CycleCount( )* threshold is in mAH, not in % of FCC	Data flash default bases *SBS.CycleCount( )* calculation on mAh and not % of FCC	*DF:Operation Cfg B [CCT = 1]*, making the default *SBS.CycleCount( )* calculation to be based on % of FCC	Data flash default changed to reflect common customer usage
When *DF:Operation Cfg B [CCT = 1]*, so that *SBS.CycleCount( )* threshold is % of FCC, then *DF:CC Threshold* is used as a minimum for the *SBS.CycleCount( )* threshold	Use *DF:CC Threshold* as the minimum to prevent rapid incrementing of the *SBS.Cyclecount( )*, damaging the data flash	Small or negative *SBS.Full Charge Capacity( )* values (should not occur under normal operation) from causing the *SBS.CycleCount( )* incrementing rapidly, potentially damaging the data flash	Improved system reliability
When exiting the relaxed state to sleep, the initial charge capacity is correctly calculated	Corrected initial charge capacity calculation to be accurate when exiting relaxed state to sleep	If the relaxed state was exited to sleep after a valid DOD measurement (30-minute default value), then the initial charge capacity would not be recalculated and would result in an incorrect FCC value if the sleep state was exited before another valid DOD measurement (30-minute default value)	More reliable *SBS:FullChargeCapacity( )* calculation under all system conditions
Correct update of Remcap in relaxed state to use passed charge	Charge or discharge current accumulated in a relaxed state used to update Remcap	If the relaxed state was exited after the accumulation of significant charge or discharge current (over at most 100 seconds with default values), the RemCap and FCC would be in error by this charge. This is only significant if the relaxed state can exist with significant current as determined by application settings.	More reliable *SBS:FullChargeCapacity( )* *SBS:RemainingCapacity( )* calculation under all system conditions
Implement disable of resistance update based on accumulative scale. If the product of 15 consecutive (default value) resistance scale factors is less than 0.5 or more than 1.5, then resistance update is disabled until the next valid soc measurement. Sets bit 2 of Operation Status to indicate resistance update disabled.	Prevent invalid soc values from causing incorrect resistance updates	Incorrect resistance updates that could result from invalid soc values	More reliable resistance updates under all system conditions
Implement disable of resistance update based on estimated capacity error. Sets bit 2 of Operation Status to indicate resistance update disabled.	Prevent invalid soc values from causing incorrect resistance updates	Incorrect resistance updates that could result from invalid soc values	More reliable resistance updates under all system conditions
Disable Qmax increment if due to Grid 14 and exit of discharge	Prevent unnecessary Qmax increments	Qmax increments can occur due to Grid 14 and exit of discharge	Improved Qmax data reliability under all system conditions.
Drive all unused pins low	Provides better ESD immunity	Not all unused pins driven low	Improved ESD immunity

Table 1. CHANGE DETAILS (continued)

CHANGE	bq0z80-V102	bq20z80-V101	COMMENTS
Initial charge capacity calculation when dod0 is measured in the overdischarged state is corrected	Overdischarged state does not affect the accuracy of FCC calculations	An incorrect initial charge capacity affects FCC that is calculated during discharge or a Qmax update. If FCC is not changed by a Qmax update, then reported RemainingCapacity could be negative after 5 hours of relaxation	More reliable *SBS:FullChargeCapacity( )* *SBS:RemainingCapacity( )* calculation under all system conditions
Correct calculation of FCC and RemCap when dod0 is taken when the battery is overdischarged or overcharged. This allows RemCap to go negative, or greater than FCC (though is only reported from 0 - FCC).	Overcharged/Overdischarged does not affect the accuracy of FCC and RemCap calculations	The RemainingCapacity will increment (or decrement) during charging (discharging) even when the battery is in an overdischarged (overcharged) state.	More reliable *SBS:FullChargeCapacity( )* *SBS:RemainingCapacity( )* calculation under all system conditions
Change cell imbalance *DF:Battery Rest Time* from 1 byte to 2 bytes and set the default value to 1800 seconds	New feature providing improved customization	Feature not available	Improved customization for Cell Imbalance detection
Use upper and lower limit for resistance accumulative scale. Set default values to 300% and 30%.			More reliable resistance updates under all system conditions
Add *DF:CF MaxError limit* for setting *SBS.BatteryMode( ) [CONDITION FLAG]*. Set default value to 100%.	New feature providing improved customization	Feature not available	Improved customization
Use *SBS.AtRate( )*, UserRate and C/5 rate for relaxed capacity calculation, respectively, if set by Load Select; otherwise, use previous rate.			More reliable *SBS:FullChargeCapacity( )* *SBS:RemainingCapacity( )* calculation under all system conditions
Correct Host Watchdog from being reset by broadcasts	Host Watchdog functionality not affected by alarm or charger broadcasts	Host Watchdog reset by alarm or charger broadcasts	Reliable Host Watchdog functionality under all system conditions
The voltage table chemistry ID can be read by writing 0x0008 to ManufacturerAccess and then reading from ManufacturerAccess. The default chemistry ID is 0x0100	New feature providing more information	Feature not available	Improved information access
SBS.BatteryMode( ) is initialized on high transition of the SMBus lines to *DF:Init BatteryMode*, instead of always clearing *SBS.BatteryMode( )* defined bits on high transition of the SMBus lines.	Customization allows for preserving *SBS.BatteryMode( )* settings through SMBus line transitions	Feature not available	Improved customization
Broadcast timers are set correctly on high transition of SMBus lines. The timers are set to 10 seconds on high transition of SMBus lines.	Broadcast timer accurate regardless of CC offset calibration or entry to sleep	Broadcast timer accuracy required a CC offset calibration and entry to sleep.	Improved broadcast timing accuracy to meet Smart Battery Data spec

14.2 SUMMARY

These significant changes improve system interaction stability and reliability under all system conditions.

- Recommended configuration file changes for existing applications include:
- Configuring the new *DF:Battery Rest Time* feature
- Configuring the new *DF:Init Battery Mode* feature
- Configuring the new *DF:CF MaxError Limit*
- Configuring the new *DF:AFE Fail Limit* feature
- Configuring the new *DF:LED Flash Rate* and *DF: LED Blink Rate* feature
- Configuring the new *DF:Chg Flash Alarm* and *DF:Dsg Flash Alarm* feature

bq20z80-V101 and bq2080-V102 Gas Gauge Circuit Design

Battery Management

ABSTRACT

Each component in the bq20z80-V101 and bq2080-V102 chipset reference designs is explained in this application report. Design tradeoffs and alternative circuits are provided, where appropriate.

15.1 Introduction

The bq20z80-V101 and bq2080-V102 advanced gas gauge chipsets have approximately 90 components in the reference design for a 4-cell application. For clarity, these components are grouped into the following classifications: High Current Path, Gas Gauge Circuit, AFE/Secondary Current Protection, and Secondary Voltage Protection.

The discussion is based on the 4-cell reference design for the bq20z80 chipset. The complete schematic is available at the end of this document.

15.2 High Current Path

The high current path begins at the Pack+ terminal of the battery pack. As charge current travels through the pack, it passes through protection FETs, a chemical fuse, the lithium-ion cell connections, the sense resistor, then returns to the Pack– terminal. In addition, some components are placed across the Pack+ and Pack– terminals to reduce effects from electrostatic discharge (ESD).

Protection FETs

The P-channel Charge, Precharge, and Discharge FETs should be selected for a given application. Most portable battery applications are a good match for the Si4435DY device or equivalent. The Precharge FET could usually be implemented with a less expensive device, but often the same device is used in order to reduce the number of unique components.

The Vishay Si4435DY is an 8.8-A, 30-V device with Rds(on) ranging from 20 mΩ to 35 mΩ depending on the gate drive voltage.

If a Precharge FET is used, R26 is calculated to limit the precharge current to the desired rate. Be sure to account for the power dissipation of the series resistors. The precharge current is limited to (Vcharger – Vbat) / R26 and maximum power dissipation is (Vcharger – Vbat)2 / R26. The gates of all p-channel protection FETs are pulled up to the source with a high value resistor to ensure they are turned off when the gate drive is open.

Depending on the charger type, C22 is used in Figure 1 to slow down the operation of the charge FET. This capacitor can be deleted if there is no concern about excessive inrush current when the charger turns on. The capacitor may not be ideal if pulse charging is used.

C13 and C18 help to protect the FETs during an ESD event. The use of two devices ensures normal operation if one of them becomes shorted. In order to have any effect, the copper trace inductance of the capacitor leads must be designed to be as short and wide as possible. Ensure that the voltage rating of both C13 and C18 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.

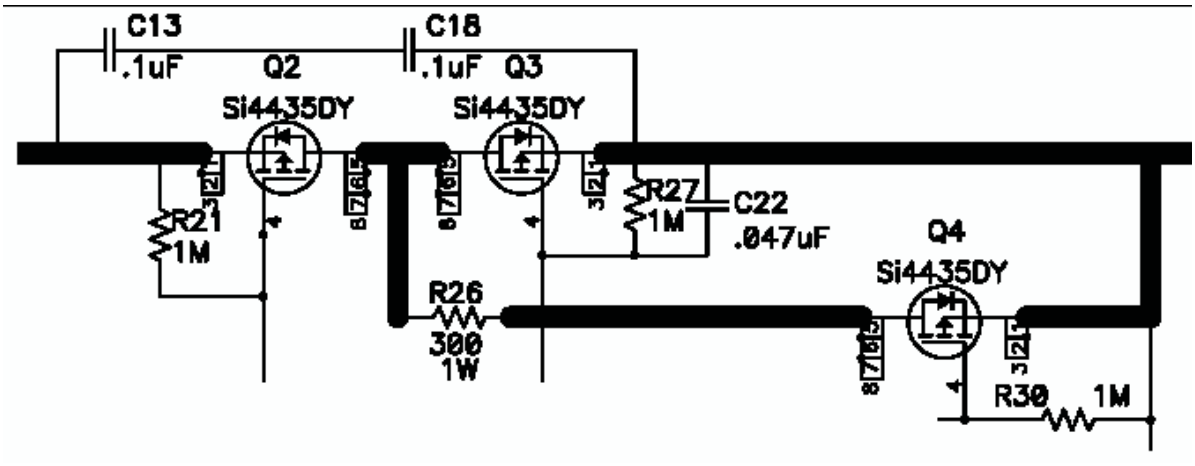


Figure 1. Protection FETs

Chemical Fuse

The chemical fuse (Sony Chemical, Uchihashi, etc.) is blown under command from either the bq29400 secondary voltage protection IC or from the SAFE pin of the gas gauge device. Either of these events applies a positive voltage to the gate of Q1 in Figure 2, which then sinks current from the third terminal of the fuse causing it to ignite and open permanently.

It is important to carefully review the fuse specifications and match the required ignition current to that available from the N-channel FET. Ensure that the proper voltage, current, and $R_{ds(on)}$ ratings are used for this device.

Optionally, a blocking diode can be inserted in series with the fuse terminal 3 to prevent false fuse ignition in the event of a reverse connection of charger or cells. In this case, current flows through the body diode of Q1 and operates the fuse without any command from the integrated circuits.

Because the gate pulldown resistor (R14) does not consume any power under normal operation, it is made relatively low to reduce the possibility of false gate activation due to PC board contamination.

The jumper, JP1, may be used to remove the possibility of false fuse activation during cell connection or debug operations. Alternately, a removable jumper could be placed between the gate of Q1 and ground.

D3 is used to sense that the fuse has blown. This is discussed in this document under the heading *Safe Circuitry*.

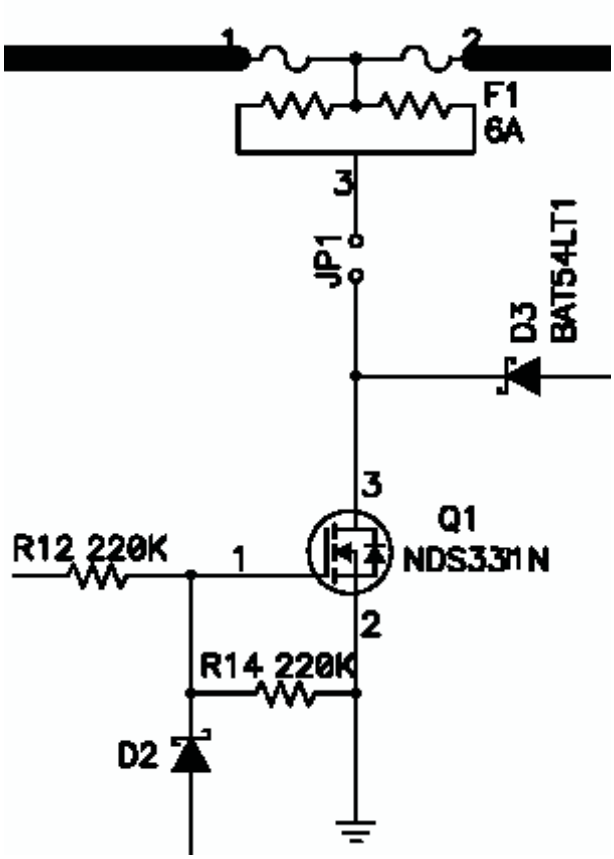


Figure 2. Chemical Fuse

Lithium-Ion Cell Connections

The important thing to remember about the cell connections is that high current flows through the top and bottom connection and, therefore, the sense leads at these points must be made with a Kelvin connection to avoid any errors due to drop in the high current copper trace. Some designs have even extended the Batt+ and Batt– sense connections all the way to the cells themselves with additional wires or a flex circuit.

The circled location 1 in Figure 3 indicates the Kelvin connection of the most positive battery node. Circled locations 2 and 3 are equally important. Note that the ground symbol at location 3 is only associated with UI, the secondary overvoltage protection device.

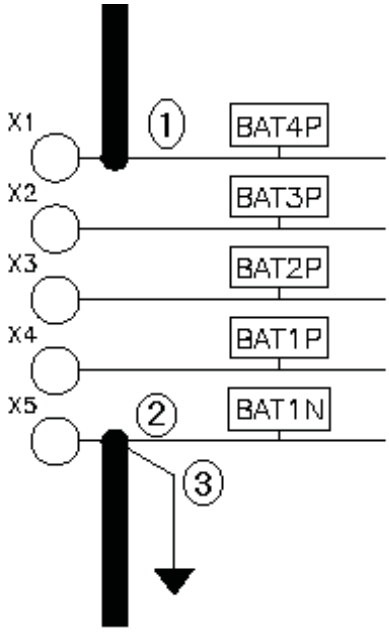


Figure 3. Lithium-Ion Cell Connections

Sense Resistor

As with the cell connections, the qualities of the Kelvin connections at the sense resistor are critical. Not only the sense lines, but the connection of low current digital ground and low current analog ground systems must be made in a careful manner.

The sense resistor should have a temperature coefficient no greater than 75 ppm in order to minimize current measurement drift with temperature. The value of the sense resistor should be chosen to correspond to the available overcurrent and short-circuit ranges of the bq29312. (See the tables in SLUS546). Parallel resistors can be used as long as care is used to ensure good Kelvin sensing.

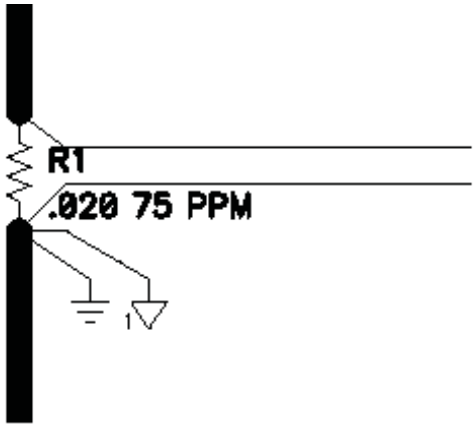


Figure 4. Sense Resistor

ESD Mitigation

A pair of series 0.1-µF capacitors is placed across the Pack+ and Pack– terminals to help in the mitigation of external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors should become shorted.

Optionally, a tranzorb such as the SMBJ2A may be placed across the terminals to further improve ESD immunity.

15.3 Gas Gauge Circuit

The gas gauge circuit includes the bq20z80-V101/bq2080-V102 and all of its peripheral components. These components are divided into the following groups: LEDs, oscillator and phase-locked loop filter, differential low pass filter, power supply decoupling / RBI / master reset, system present, SMBus communication, and SAFE circuit.

LEDs

The LEDs are associated with current limiting resistors R33 through R37. It is better to place the resistors on the IC side as they offer some ESD protection to the gauge in the event of ESD entry from human contact near the LEDs.

The display switch just yanks the bq20z80-V101/bq2080-V102 pin 17 to ground to generate an interrupt. It is pulled up to 3.3 V with a 100-kΩ resistor. If your packaging is arranged to permit an ESD hit to the switch, you may want to insert a clamping diode, and/or RC damping here also.

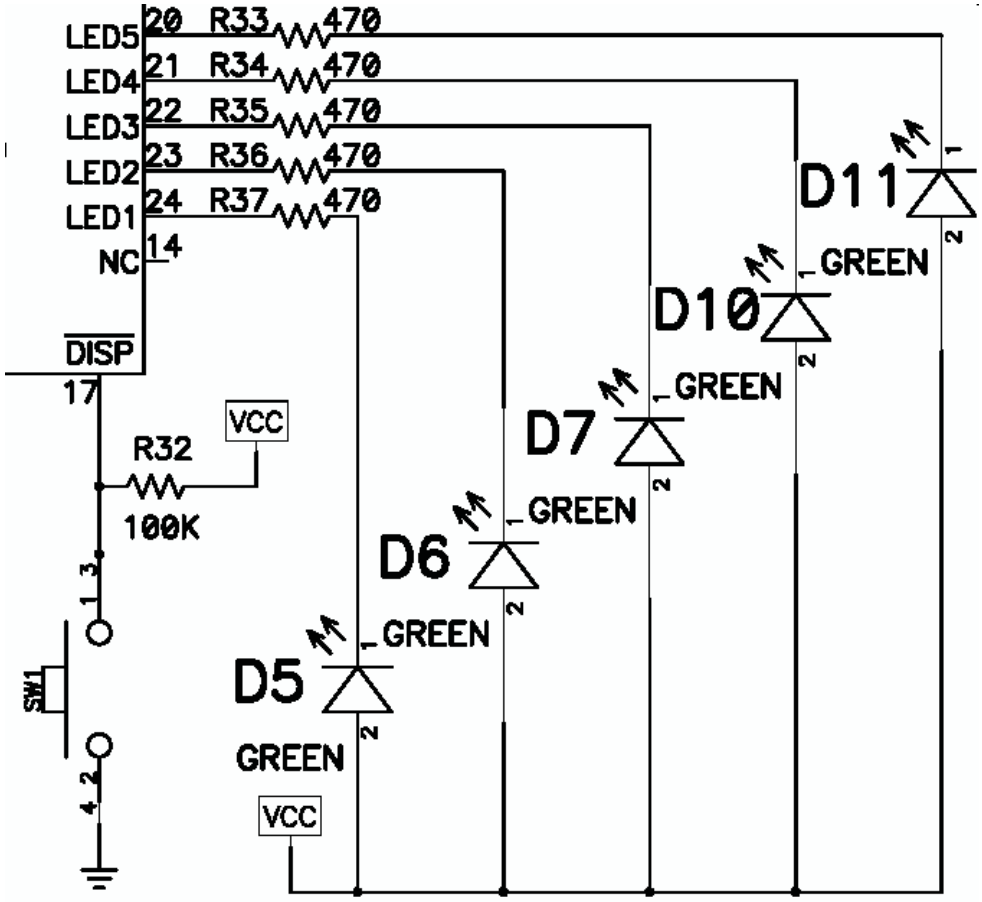


Figure 5. LEDs and Display Switch

Oscillator and Phase-Locked Loop Filter

The 100-kΩ resistor R38 sets the 32.768-kHz clock frequency for the gas gauge. The accuracy of this clock is important, as it directly affects the accuracy of the coulomb counter as it integrates measured current over time. For this reason, the accuracy of the 100-kΩ oscillator resistor should be at least 0.2% with temperature coefficient of 75 ppm or better.

The gas gauge uses an internal phase-locked loop to multiply the 32.768-kHz time base to a much higher frequency for the microcontroller clock. The VCO input of the PLL requires a low pass filter, which is implemented by R42, C27, and C28. The use of a 1% resistor and 5% capacitors is recommended. Do not change the value of these components.

Each of these four components requires attention to layout and should be located near its respective IC pins.

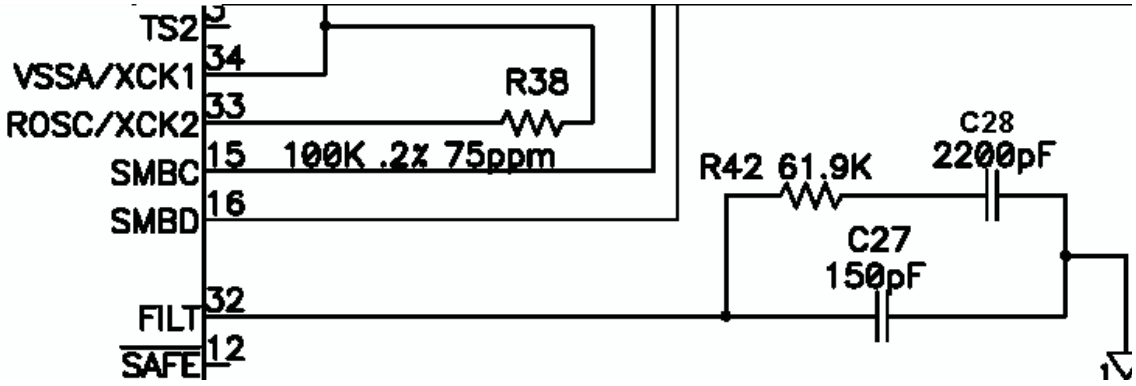


Figure 6. Oscillator Resistor and Phase Lock Loop Filter

Differential Low Pass Filter

A differential filter as shown in Figure 7 should precede the current sense inputs of the gas gauge. This filter eliminates the effect of unwanted digital noise, which could cause offset in the measured current. Even the best differential amplifier has less common-mode rejection at high frequencies. The amplifier input stage may rectify a strong RF signal, which then may appear as a dc offset error.

Five percent tolerance of the components is adequate because capacitor C19 shunts C14/C15 and reduces AC common-mode rejection arising from component mismatch. It is important to locate C19 close to the gas gauge pins 27 and 28. The other components should also be relatively close to the IC. The ground connection of C14 and C15 should be close to the IC.

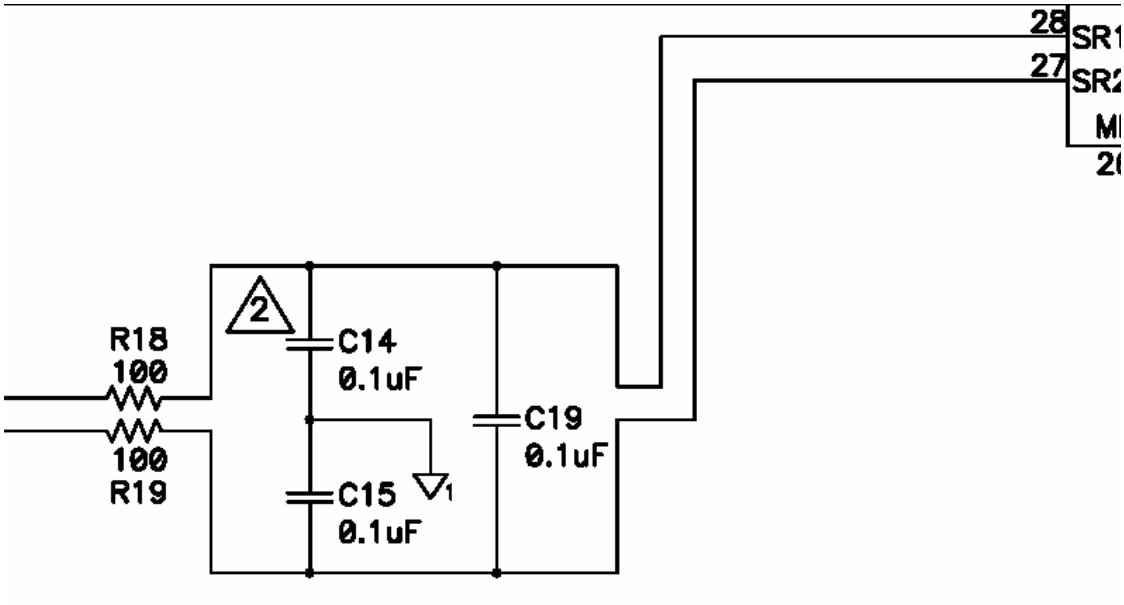


Figure 7. Differential Filter

Power Supply Decoupling, RBI, and Master Reset

Power supply decoupling is important for optimal operation of the bq20z80 and bq2084 advanced gas gauges. As shown in Figure 8, two decoupling capacitors are recommended. Note, however, that the 0.47-µF capacitors do not prevent partial resets of the gas gauge during severe ESD events. These partial resets are not harmful, because all required information is backed up and is restored by a recovery routine after the reset.

However, some reliability groups are not satisfied with this approach, preferring to prevent the partial resets from occurring. An ESD event is quite brief with the equivalent frequency approaching 1 GHz. The 0.47-µF capacitors, which are required for lower frequency decoupling, are not effective at UHF frequencies and beyond. Standard 68-µF to 100-pF ceramic capacitors are effective, however, and can prevent partial resets if placed in parallel with the 0.47-µF devices. They must be located as close as possible to the respective power input pins.

The 10-Ω resistor further helps to isolate digital noise from the analog measurement system. Also, because the input to the Power On Reset (POR) circuit is connected to VDDA, it is important to make it more sensitive to power disruption than the VDDD pin.

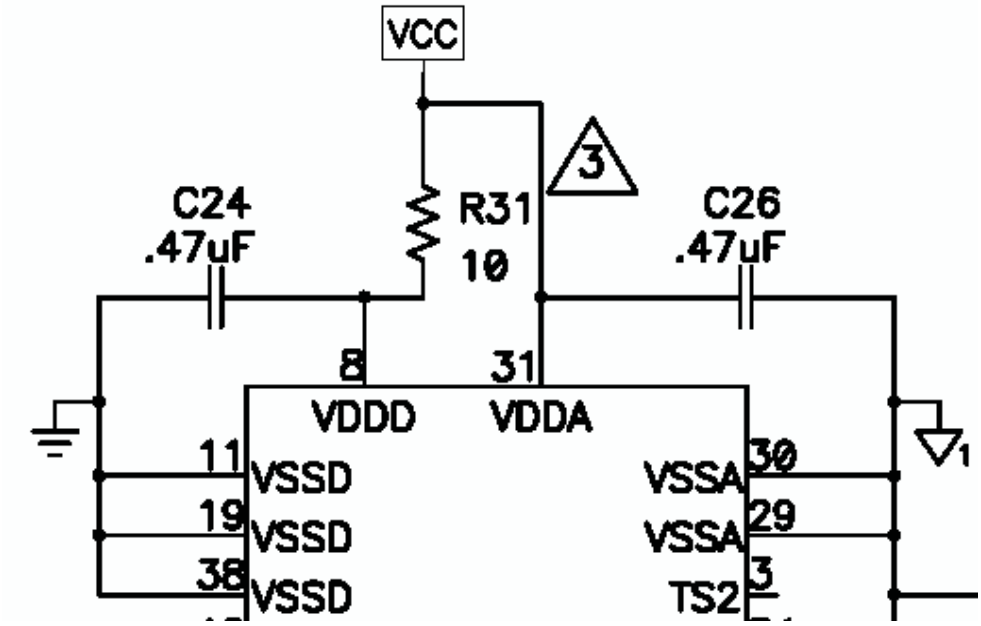
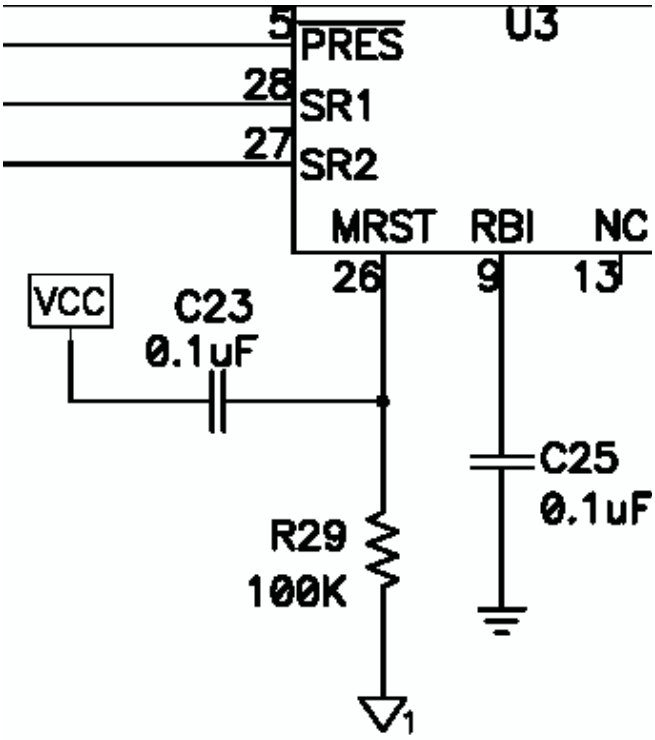


Figure 8. Power Supply Decoupling

The RBI pin is used to supply backup RAM voltage during brief, transient power outages. The partial reset mechanism just referred to uses the RAM to restore the critical CPU registers following a temporary loss of power. A standard 0.1-µF ceramic capacitor is connected from pin 9 to digital ground as in Figure 9.

C23 and R29 form an RC network, which holds the MRST pin high for the time constant during power-on-reset. While this network is required for the bq20z80, it is **NOT** required for the bq2084. In the latter case, MRST may be tied directly to ground or to ground through a low value resistor.



NOTE: C23 and R29 not required for bq2084

Figure 9. RBI Capacitor and Master Reset

System Present

The System Present signal is used to inform the gas gauge whether the pack is installed into or removed from the system. In the host system, this signal is grounded. The $\overline{\text{PRES}}$ pin of the bq20z80-V101/bq2080-V102 is occasionally sampled to test for System Present. To save power, a 5-kΩ pullup resistor is powered by the PU output on pin 4 only during a brief 4-µs sampling pulse once per second.

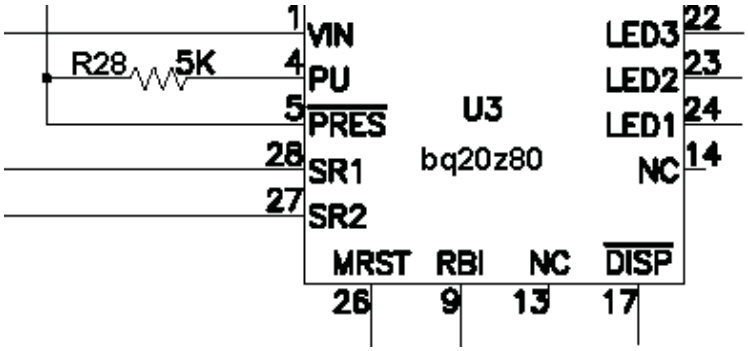


Figure 10. System Present Pull-Up

Because the System Present signal is part of the pack connector interface to the outside world, it must be protected from external ESD hits. R45 and the 5.6 V D8 provide protection for positive pulses, while R39 limits the current that would flow out of the IC in parallel with the current through D8 for negative pulses. Observe the voltage rating of D8 in order to maintain signal integrity and avoid electrical stress to the IC. When the system present function is not used, it should be connected to ground.

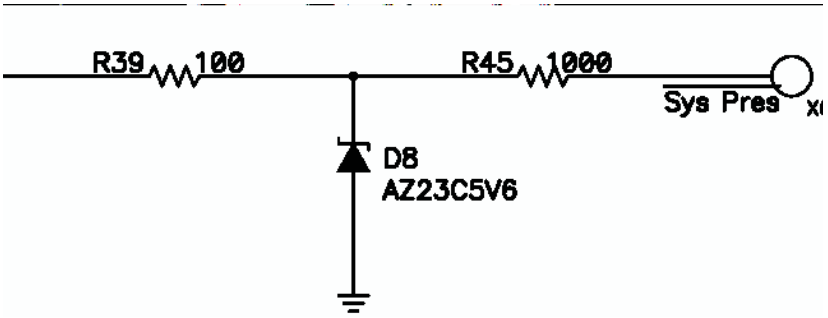


Figure 11. System Present ESD Protection

SMBus Communication

As with the System Present pin, the SMBus clock and data signals interface to the outside world on the pack connector. Each signal employs an ESD protection scheme similar to that used in Figure 11 for System Present. It should be noted, however, that the 5.6-V zener diode must have nominal capacitance less than 100 pF in order to meet the SMBus specifications. The AZ23C5V6 is a recommended device. Also, the resistor on the pack side is only 100 Ω to maintain signal integrity. Note that the zener will not survive a long-term short to a high voltage.

R46 and R47 provide pulldown for the communication lines. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto offset calibration and then goes into sleep mode to conserve power.

ESD protection operates as with the System Present network shown in Figure 11. For the SMB clock signal R43 and part of D9 provide clamping for positive ESD pulses, whereas R40 limits the current from the IC in parallel with D9 for negative ESD pulses. For the best ESD protection, the anode of the zeners (D8 and D9) should return to PACK- rather than be connected to the low current digital ground system.

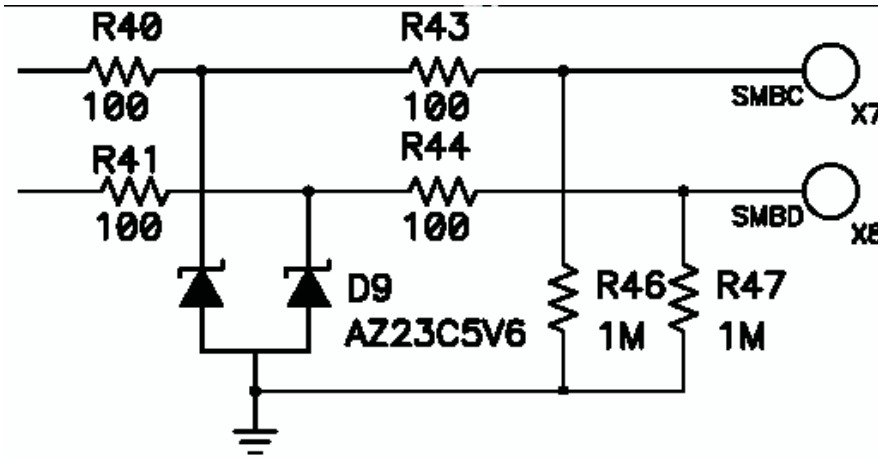


Figure 12. SMB Communication

SAFE Circuitry

The SAFE output (pin 7) of the bq20z80 is designed to blow the chemical fuse if various safety criteria are violated. The PFIN input (pin 18) is used to monitor the state of the secondary voltage protection IC.

Q1 ignites the chemical fuse when its gate is high. R12, R14, and D2 form a logical OR gate which enables the Q1 gate if either the SAFE signal or the output of the bq29400 device go to the high state. The 7-V output of the bq29400 is divided in half by R12 and R14 which provides adequate gate drive for Q1 while guarding against excessive back current from D2.

Many circuit designers prefer to add a capacitor to ground from the gate of Q1. Although this is generally good practice, especially for RFI immunity, note that the chemical fuse is a comparatively slow device and is not affected by any sub-microsecond glitches that may come from the SAFE output during the cell connection process.

When the fuse is commanded to ignite, D3 becomes forward-biased, which notifies the gas gauge of the situation. In this manner, the output of U1 can be recorded for future fault analysis.

The bq2084 requires a slightly more complex circuit, because SAFE is not implemented on pin 7. Both devices have the low-active $\overline{\text{SAFE}}$ signal available on pin 12. The use of $\overline{\text{SAFE}}$ requires an additional FET to invert the signal and ensure proper operation.

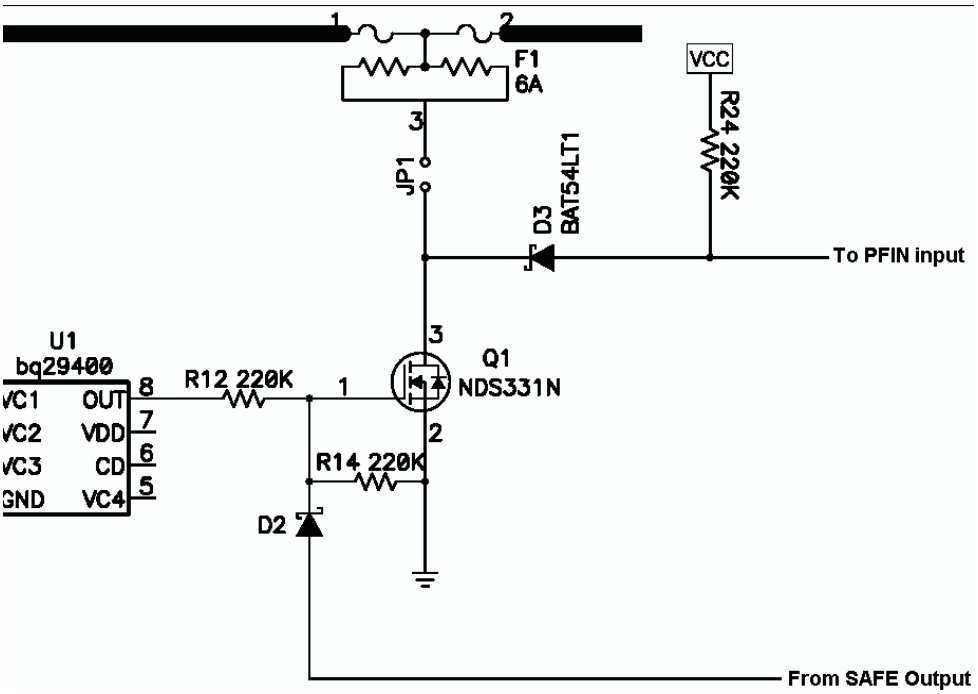


Figure 13. bq20z80 SAFE Circuit

15.4 AFE/Secondary Current Protection

The bq29312 analog front end (AFE) provides secondary overcurrent and short-circuit protection, cell balancing, cell voltage multiplexing, voltage translation, and the low dropout 3.3-V regulator for the gas gauge. The following discussion covers cell and battery inputs, pack input, sleep and PMS inputs, FET control output, regulator output, temperature output, and cell voltage output.

Cell and Battery Inputs

Each cell input is conditioned with a simple RC filter with a time constant of at least 10 μs. This filter provides ESD protection during cell connect and acts to filter unwanted voltage transients. The resistor value allows some tradeoff for cell balancing versus safety protection.

Internal FETs in the bq29312 provide an approximate 400-Ω resistance, which can be used to bypass charge current in individual cells that may be overcharged with respect to the others. (Of course, this is not done during the low duty cycle voltage measurement phase.) If the filter is built with 1-kΩ resistors and 0.01-μF capacitors, the cell-balancing feature is not effective because the total bypass resistance across a cell is 1000 + 1000 + 400 = 2400 Ω. As the reference design indicates, 100-Ω resistors and 0-μF capacitors are recommended. Values between 200 Ω and 470 Ω can provide limited cell-balancing functionality.

The BAT input (pin 1) uses a diode (D1) and 1-μF capacitor (C11) to isolate and decouple it from the cells in the event of a transient dip in voltage caused by a short-circuit event.

Also, as described previously in the High Current Path section, the top and bottom nodes of the cells must be sensed at the battery connections with a Kelvin connection to prevent voltage-sensing errors caused by a drop in the high current PCB copper.

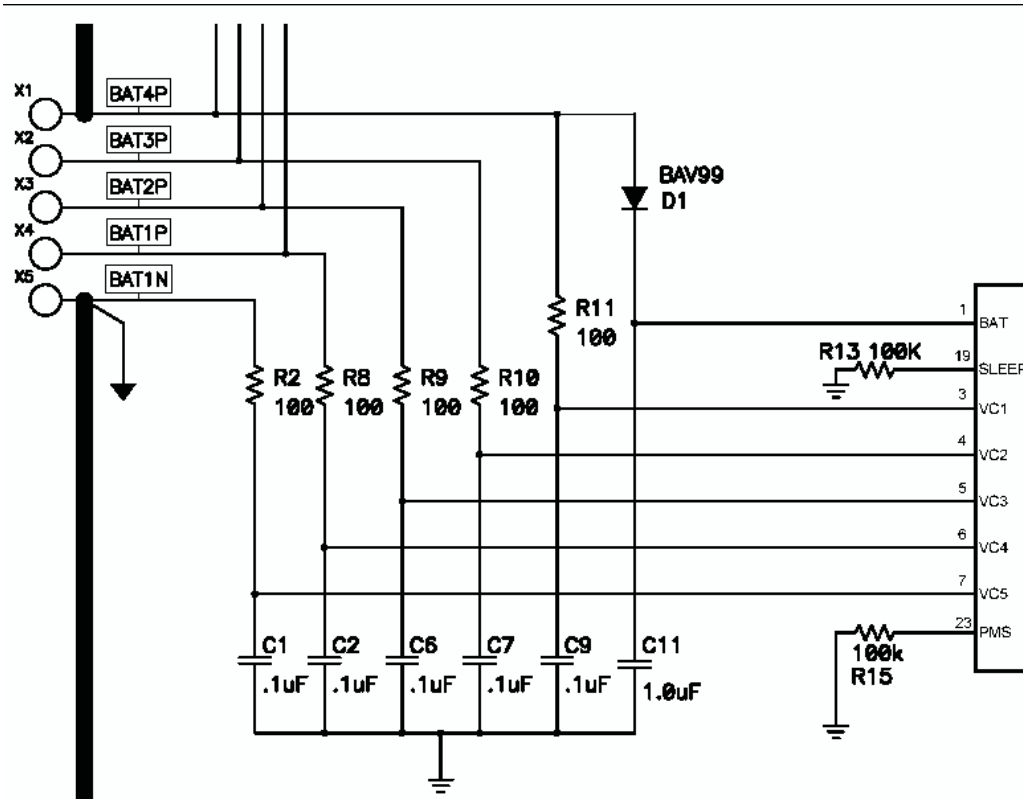


Figure 14. Cell and BAT Inputs

PACK Input

The PACK input provides power to the AFE from the charger. This way, the device continues to function normally even if the cell voltage is depleted. The PACK input uses a diode (D4) and 0.47-µF capacitor (C17) to isolate and decouple it from the Pack+ input. This guards against input transients and prevents mis-operation of the gate driver in the event of a reverse charger connection. Ensure that the voltage ratings of D4 and C17 are adequate to withstand the full system voltage.

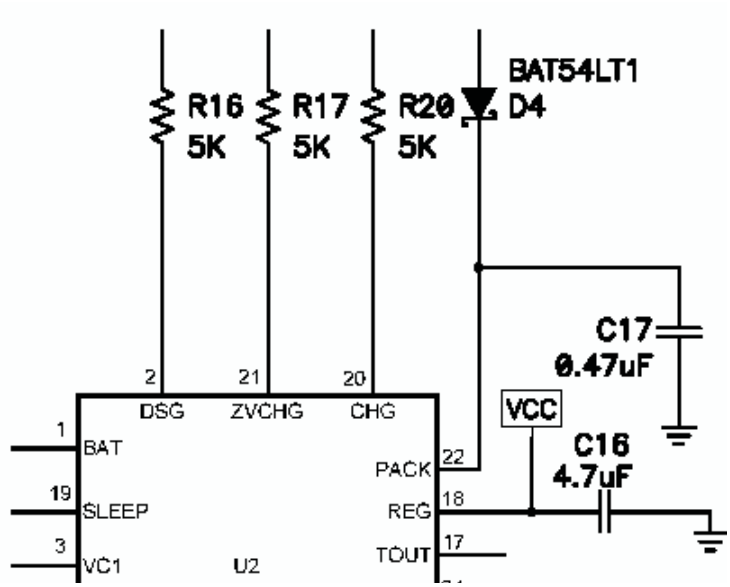


Figure 15. PACK Input

Sleep and PMS Inputs

The sleep pin is generally not used, but should be grounded through a 100-kΩ resistor. The PMS pin, depending on the desired operating mode, should also be tied to ground or PACK through a 100-kΩ resistor. The resistor for the sleep pin is to improve ESD susceptibility and can be eliminated only if a short path can be used to connect it directly to pins 12 and 15.

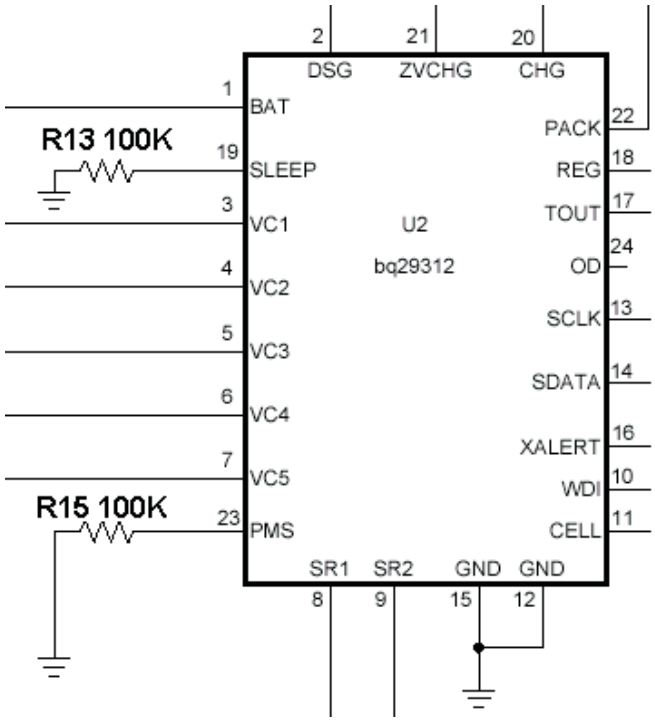


Figure 16. SLEEP and PMS Inputs

FET Control Outputs

The three FET control outputs are simply coupled to the gates of the protection FETs with 5-kΩ resistors. These resistors, with the gate-source capacitance, determine the switching time of the FETs. As mentioned in the Protection FETs discussion of High Current Path section of this document, the charge FET often uses an additional *slow-down* capacitor from its gate to source to limit di/dt when the charger is first applied.

Regulator Output

The low dropout regulator within the bq29312 requires capacitive compensation on its output. In order to guarantee the integrity of the compensation, the 4.7-µF capacitor should be placed close to the REG output (pin 18).

Temperature Output

TOUT (pin 17) provides thermistor drive under program control. R22 and R25 are specific 1% resistors for optimization of the recommended Semitec NTC103AT, or equivalent thermistor. Because this thermistor is normally external to the board, C21 is provided for ESD protection.

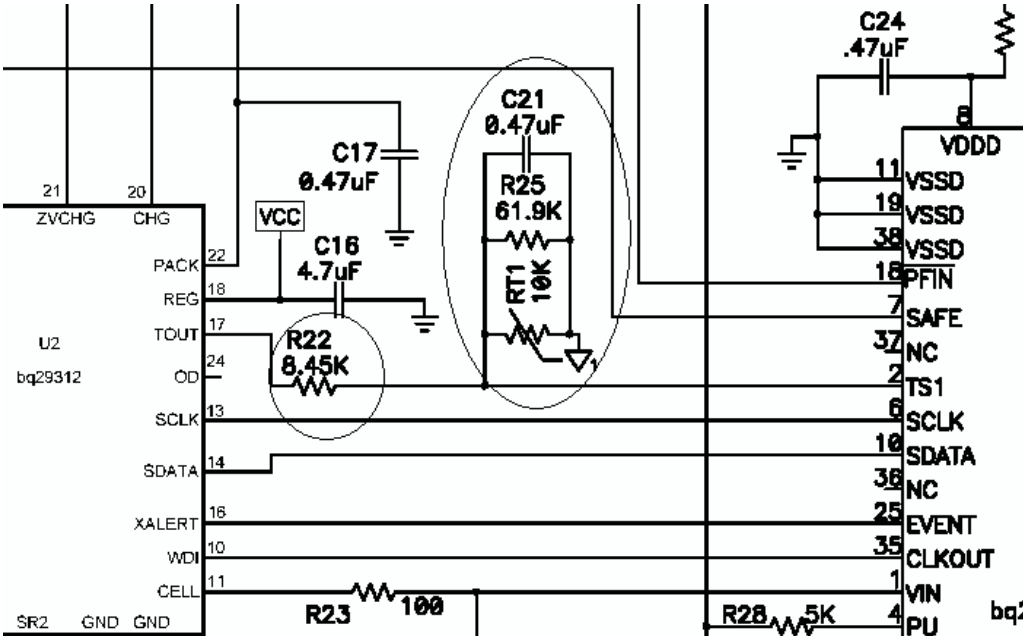


Figure 17. Thermistor Drive Output

Cell Voltage Output

The CELL output requires an RC filter composed of a 100-Ω resistor and 0.1-µF capacitor. This filter stabilizes the output amplifier in the bq29312 and provides the required filtering for the input of the gas gauge A/D converter.

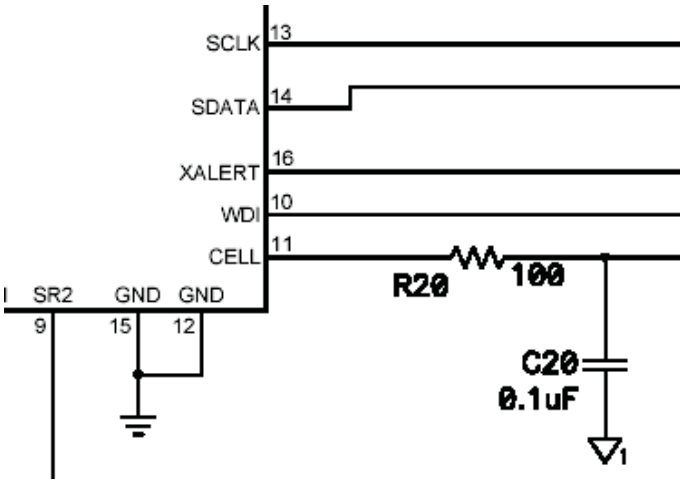


Figure 18. CELL Output

15.5 Secondary Voltage Protection

The bq29400 provides secondary overvoltage protection and commands the chemical fuse to blow if any cell exceeds the internally referenced threshold. The peripheral components are cell input filters and a time delay capacitor.

Cell Inputs

An input filter is provided for each cell input. This filter comprises resistors R4, R5, R6, and R7 along with capacitors C3, C4, C5, and C8. Note that this input network is completely independent of the filter network used as input to the bq29312. To ensure independent safety functionality, the two devices must have separate input filters.

Note that because the filter capacitors are implemented differentially, a low voltage device can be used in each case.

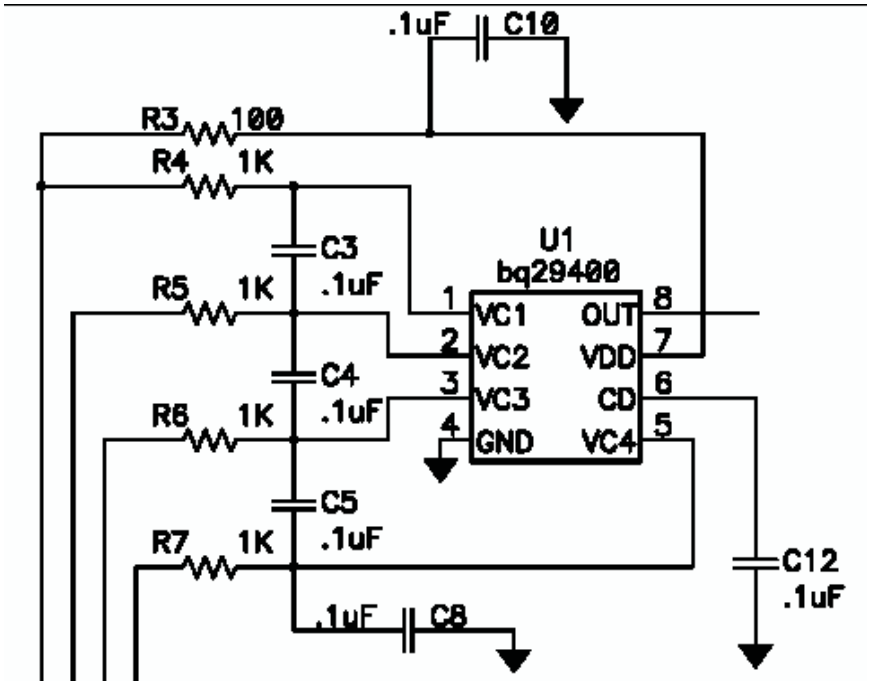


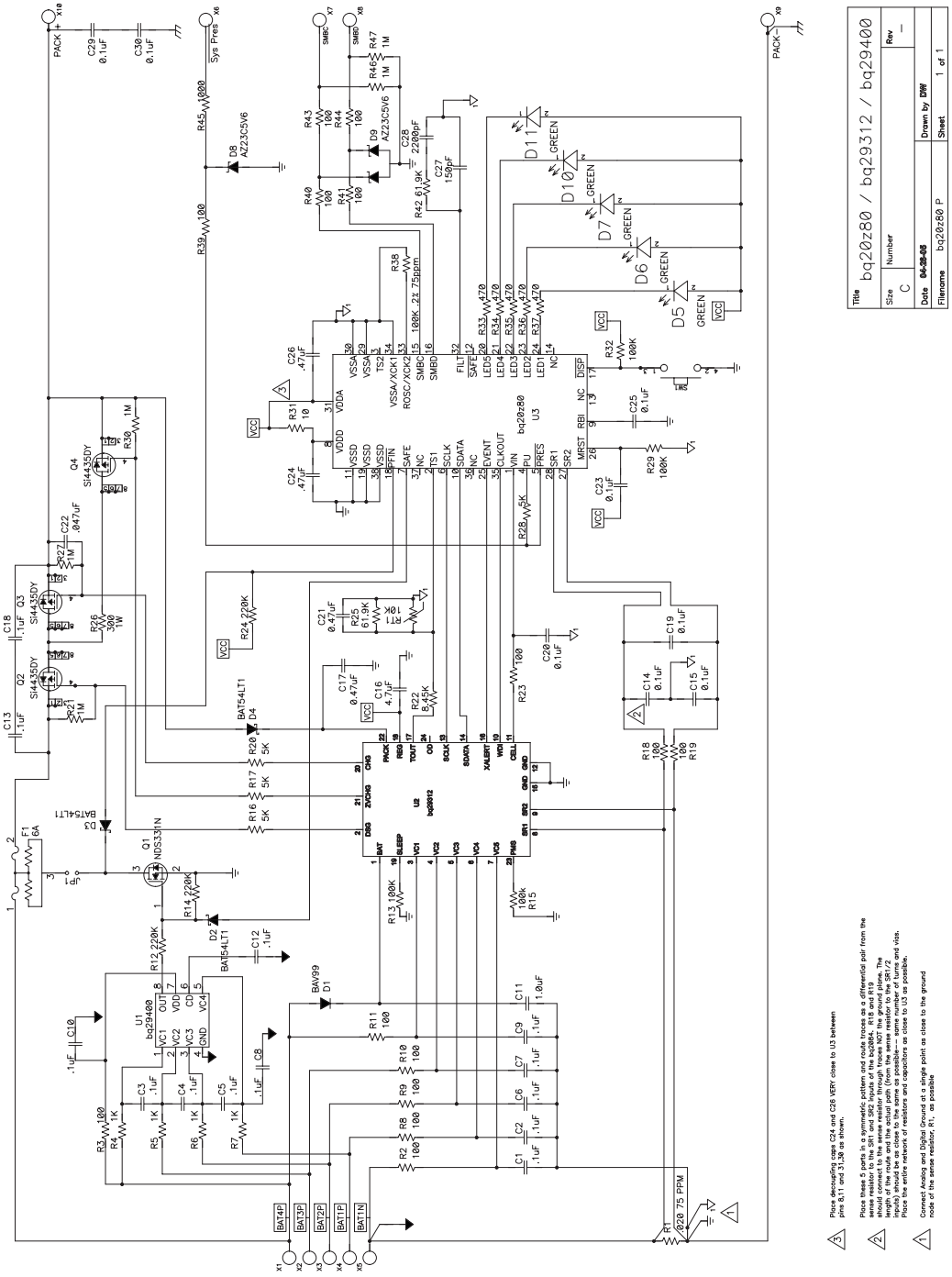
Figure 19. bq29400 Cell Inputs and Time Delay Capacitor

Time Delay Capacitor

C12 sets the time delay for activation of the output after any cell exceeds the threshold voltage. The time delay is calculated as td = 1.2 V × DelayCap(μF) / 0.18 μA.

15.6 Reference Design Schematic

The reference design schematic appears on the following page.



Avoiding ESD and EMI Problems in bq20zxx Battery Pack Electronics

Doug Williams *Battery Management*

ABSTRACT

In an increasingly wireless world, electrostatic discharge and electromagnetic interference are both potential issues for portable battery packs. This application report discusses the causes of ESD and EMI issues in battery pack designs and offers solutions for mitigation.

16.1 Introduction

Electrostatic discharge (ESD) and electromagnetic interference (EMI) are both potential issues for portable battery packs in an increasingly wireless world. The bq20zxx Impedance Track™ advanced gas gauge family chipsets are based on a low-power microcontroller, which must be protected from severe outside disturbances. For a robust design, careful PCB layout and various mitigation techniques are necessary considerations.

16.2 Watery Grave

In the June 23, 2005 edition of EDN magazine, Howard Johnson, Ph.D., wrote an article entitled *Watery Grave*. In the article, he presented the scenario of a person on a lake, in an aluminum canoe, as a terrible thunderstorm was approaching. Given the following three choices, the reader was asked to select the one that would afford the best chance for survival (assuming there would not be a direct hit, which would be fatal in any case).

1. Stay in the canoe
2. Swim to shore
3. Invert the canoe and dive under it for protection (it becomes a Faraday shield)

The correct answer, of course, is to stay in the canoe because the hull of the boat would divert the current around the person. The same strategy could be used to protect integrated circuits inside a battery pack from the miniature lightning of an ESD hit. If the pack could be fitted with a metal case, the solution would be clear. Although the solution with the standard plastic case is not quite so obvious, the method is still the same — the current must be diverted around the unit to be protected.

For an EMI attack, the analogy holds also. RF energy can arrive by either radiation or conduction. Using shielding or bypass techniques, the energy must be diverted around the vulnerable semiconductor structures which can rectify the RF into lower frequency signals able to interfere with system operation.

16.3 Follow The Electrons

Figure 1 represents the general model for battery pack cells, electronics, and the pack connector. The BMU, or *battery management unit*, is comprised of various integrated circuits and peripheral components in the fuel gauge and safety circuitry design. This model is used to trace the flow of current during an ESD hit and an attack by heavy RF field intensity.

The Li-ion cells, protection FETs, sense resistor, and the pack connector surround the BMU. The single RC filter to the left of the BMU represents one of several connections, which monitor the voltage of each cell. The connections below the BMU represent various connections from the electronics to the common ground point, which is usually located on the PACK— side of the sense resistor. The resistors and zener diode to the right of the BMU represent the typical protection network for one of the communication lines.

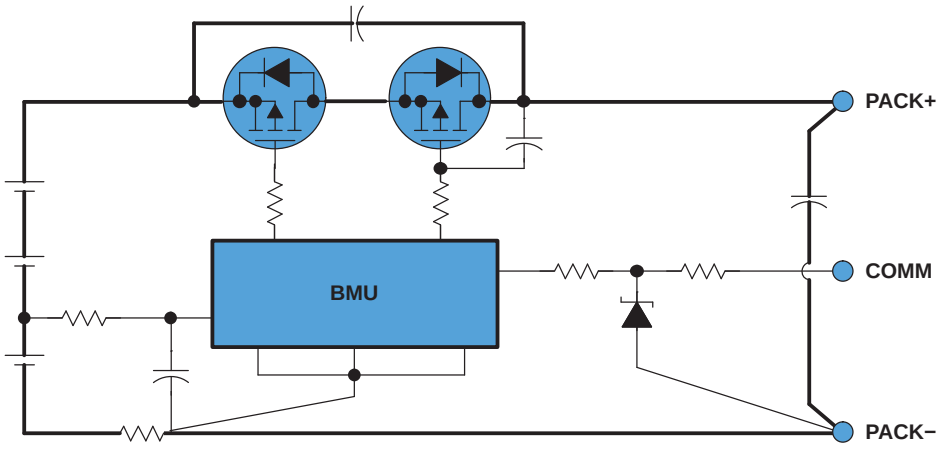


Figure 1. Basic Battery Pack Block Diagram

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During an electrostatic discharge from a human body onto the battery pack connector, the current from the charged source tends to flow into the largest available capacitance, which is that of the cells themselves with respect to ground. Naturally, most of the current tends to take the path with the lowest impedance. Wide copper traces, with their low resistance and inductance, become the *diverters*— able to protect the sensitive electronics from grave danger.

In Figure 2 and Figure 3 can be seen the preferred diverting path for a zap to Pack+ and Pack–.

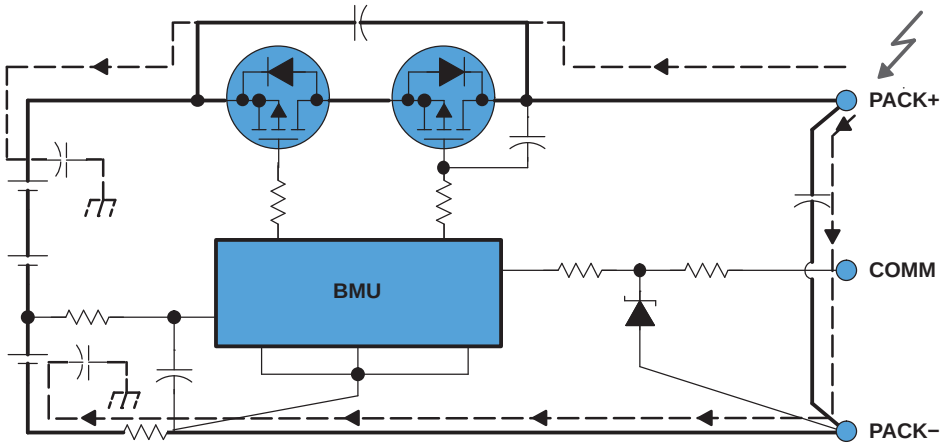


Figure 2. ESD Hit to PACK+ Connector Pin

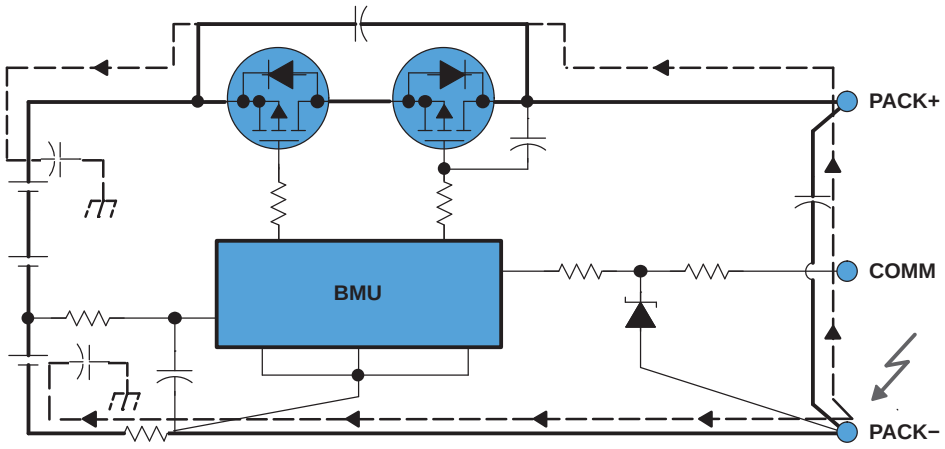


Figure 3. ESD Hit to PACK– Connector Pin

In both cases, the preferred path is similar. The copper to the FETS is wide, but then what? The capacitor (usually two in series in the event that one shorts) across the FETS helps to protect them. But this can only be realized if the copper traces to the capacitor are also wide enough to offer the required low resistance and inductance.

The capacitor (again, usually two in series) between Pack+ and Pack– is equally critical. It is desirable that current from a hit to Pack+ be diverted, as much as possible, away from the FETS and their associated nodes, which lead into the electronics. The copper between the pack connections and the capacitor(s) must be short and thick.

For a zap to a communications pin, again it is desirable to provide a low impedance path to the cell capacitance. In Figure 4, it can be seen that the desired current path is through the first series resistor, through the capacitance of the zener diode, then on to the wide PACK– copper trace. Keeping the zener close to the pack connector and using sufficient copper width ensures that the BMU is protected. In the case of a negative polarity zap, current flows out of the BMU in parallel with current through the zener. The resistor on the BMU side limits the ESD current to a safe level.

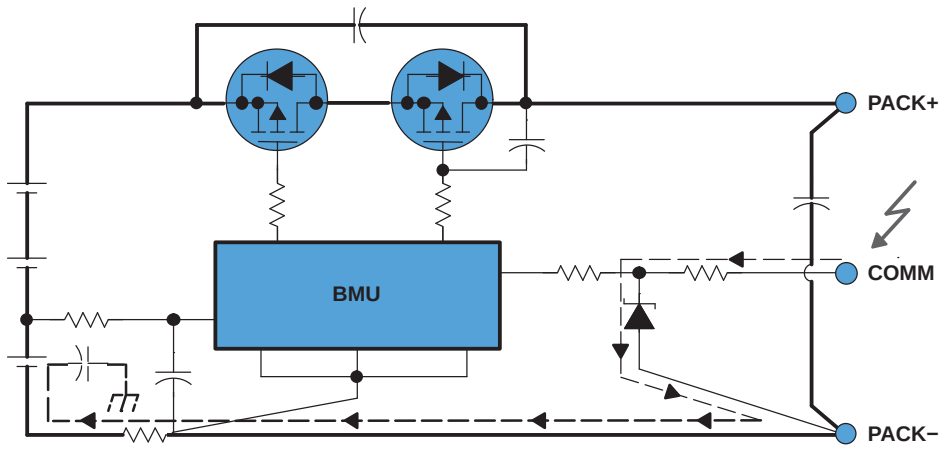


Figure 4. ESD Hit to the CLOCK or DATA Connector Pin

16.4 Keep ICs Off the Electron Highway

Whereas wide traces help to lower the inductance of copper traces, they still appear quite inductive at ESD pulse frequencies. At high frequencies, the diverting path can act as the primary of a current transformer, injecting unwanted and potentially disruptive currents into adjacent copper loops which feed into sensitive (ultralow power!) electronics.

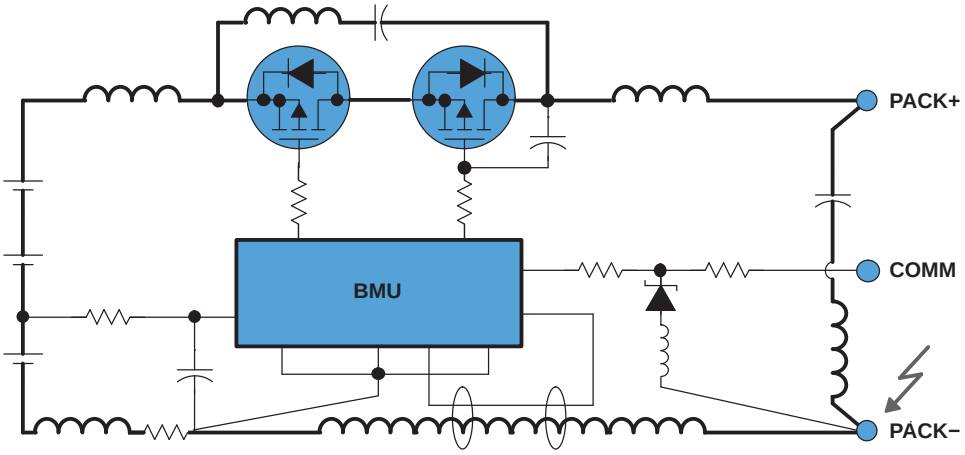


Figure 5. High-Frequency Currents From ESD or Inrush Can Be Inductively Coupled

The best defense against this sort of assault is to physically separate the high-current path from the sensitive electronics. Although this may not be feasible in many battery pack designs, it is an ideal goal for rugged design. High-current inrush pulses and ESD pulses do not mix well with ultralow power electronics. Both inductive and capacitive coupling must be considered in the layout.

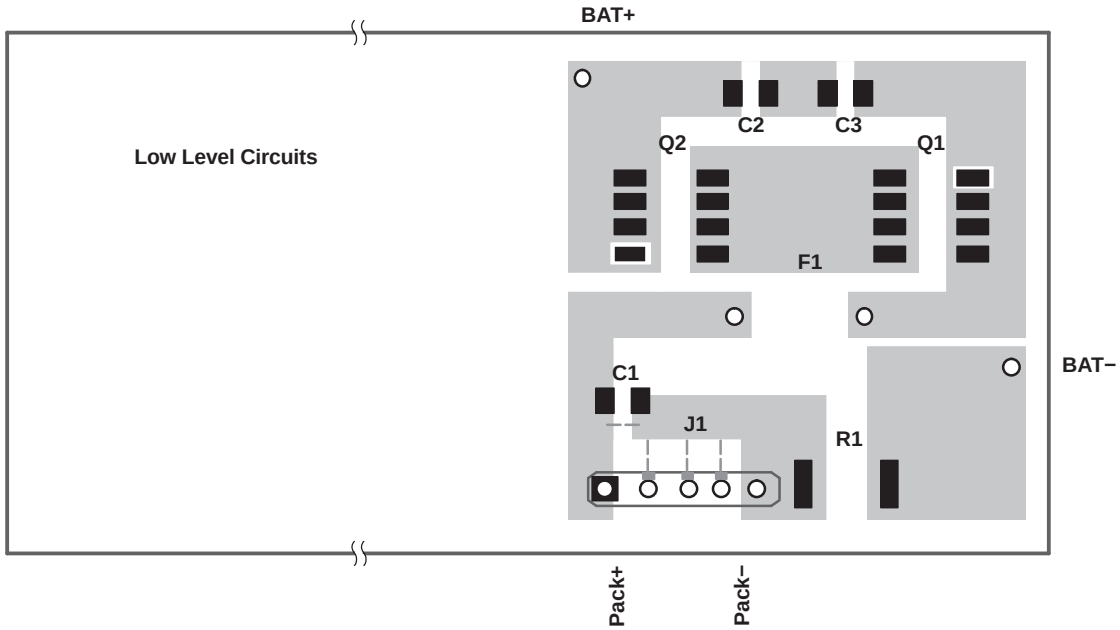


Figure 6. The Ideal Layout Separates the High-Current Path From the Low-Current Electronics

16.5 Separate Low-Level Ground Systems

Because e = L di/dt, and the derivative of the current is still quite large, significant voltages can be generated along the diverting current path. This is one of the reasons for using a separate low-level ground system with a single-point connection at the sense resistor. This avoids damage to the integrated circuits from circulating currents in the ground system during an ESD event . See Figure 7 and Figure 8.

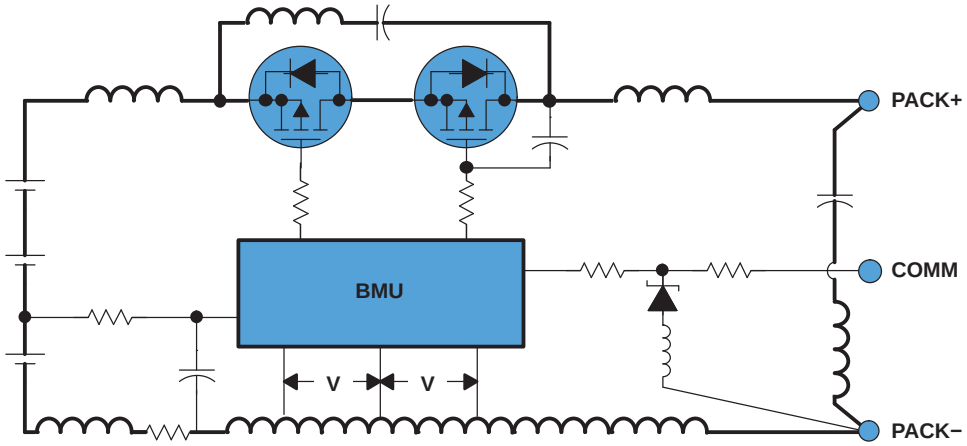


Figure 7. BMU Electronics Can Be Disrupted and Damaged From Circulating Ground Currents

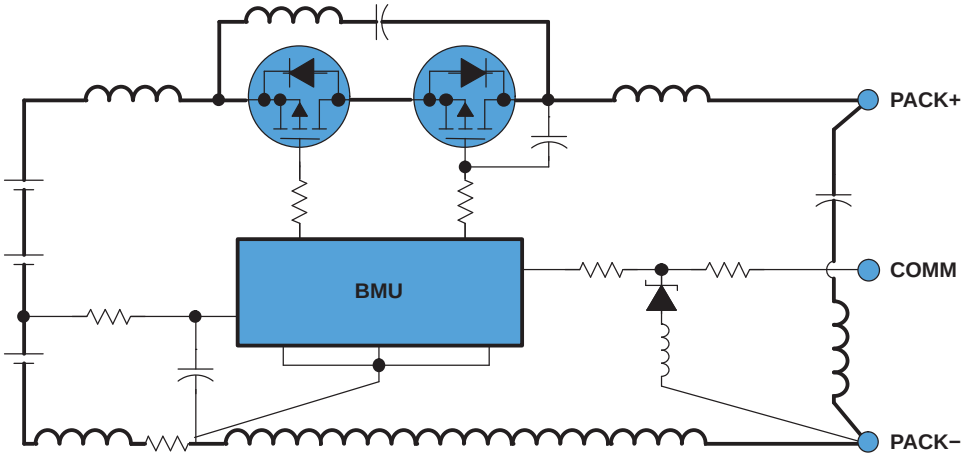


Figure 8. Correct BMU Grounding Is Separated From PACK– Except at the Single Connection at the Sense Resistor

16.6 Spark Gaps

Spark gaps are quite effective, especially for protecting the communication lines from ESD hits. Use the pattern as shown in the figure below, with a 10-mil (0,2-mm) gap. This provides a voltage breakdown at sea level of about 1500 V. For maximum effectiveness, the spark gaps must be on an outer layer of the PC board and should not be coated with any protective covering.

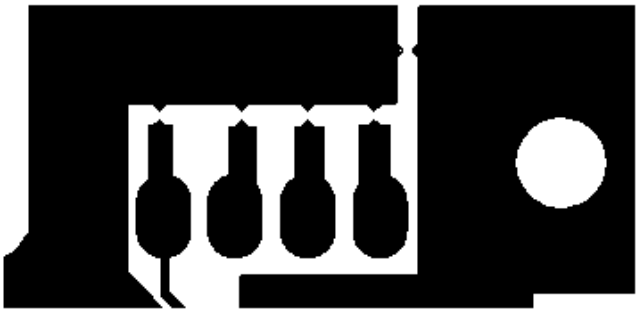


Figure 9. Recommended Spark Gap pattern on Battery Pack Connector

16.7 RF Bypassing

Perhaps the best way to understand RF interference is with the *crystal set* analogy. All semiconductors behave as diodes and rectify RF signals as with the simple demodulation of AM radio and TV picture transmission. The RF energy can be transported into a battery pack by either radiation or conduction. The cells and their leads can act as an antenna, or copper traces on the PC board itself can be the receiving antenna. Antennas are most effective at multiples of their length. A cell phone operating at 1800 MHz has a fundamental wavelength of 16.7 centimeters. A nice half-wave antenna would be 8.3 cm, while an effective quarter-wave antenna is only 4.2 cm. For this reason, RF testing of a new battery pack design is highly recommended to ensure its dependability in common RF environments, such as cell phones and other two-way radios.

Rectified RF can cause a number of problems including voltage, temperature, and current measurement errors. Also, microcontroller mis-operation and unintended fuse blowing are possible.

If any of these effects are observed during testing, it may be relatively easy to bypass the receiving semiconductor input with one or more small ceramic capacitors. Capacitors in the 68-pF to ~100-pF range have a low shunt impedance at VHF and UHF radio frequencies.

bq20z80 Printed Circuit Board Layout Guide

17.1 Introduction

Attention to layout is critical to the success of any battery management circuit board. The mixture of high current paths with an ultralow current microcontroller creates the potential for design issues that are not always trivial to solve. Guidelines are presented to provide a stable and well performing project. Careful placement and routing is required with regard to the principles described in this document.

17.2 Component Placement

Power Supply Decoupling Capacitors

Power supply decoupling is important for optimal operation of the bq20z80 advanced gas gauge. To keep the loop area small, place these capacitors next to the IC. Use the shortest possible traces to the IC. Ideally, the traces on each side of the capacitor should be the same length and run in the same direction to avoid differential noise during ESD. If possible, place a via near the VSSD pin to the digital ground plane and another from the VSSA pin to the analog ground plane

Figure 1 is an example of what NOT to do. The decoupling caps are close to the IC, but the loop area too wide, rendering the capacitor useless and forming an antenna for noise pickup

AFE Decoupling and LDO Compensation Capacitor

Power supply decoupling for the bq29312 can best be achieved by placing a 1-µF / 25-V capacitor mid way between pin 1 and pin 12.

The LDO voltage regulator within the bq29312 requires a 4.7-µF capacitor to be placed close to the REG pin. This cap is for amplifier loop stabilization as well as an energy for the load.

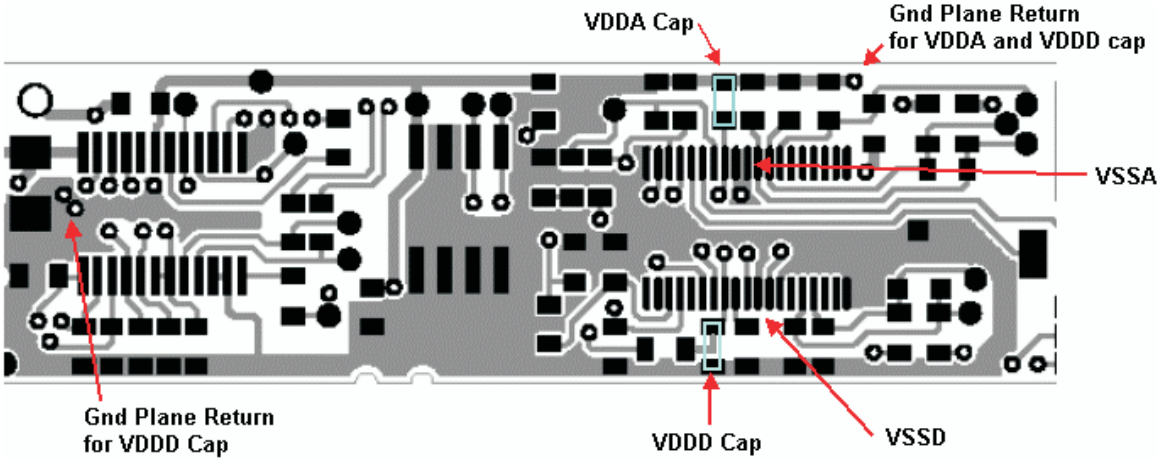


Figure 1. Bad example of decoupling capacitor placement and routing

PLL, Oscillator and Master Reset Components

The VCO in the phase locked loop (PLL) requires a low pass filter. Since this is a sensitive circuit, care should be used to place these components close to pin 32 of the IC.

The 100-K oscillator resistor, if used instead of a crystal, is perhaps the most critical component surrounding the bq20z80. Because the clock circuit is based on an extremely low level current source, any ground noise can introduce unwanted jitter into the 32 Khz clock. Place the resistor close to the IC, connecting to pins 33 and 34. Pin 34 must be connected to the analog ground when an oscillator resistor is used. Use a separate trace to connect pin 34 to analog ground at pins 29/30. This prevents any unwanted ground current from interfering with the clock

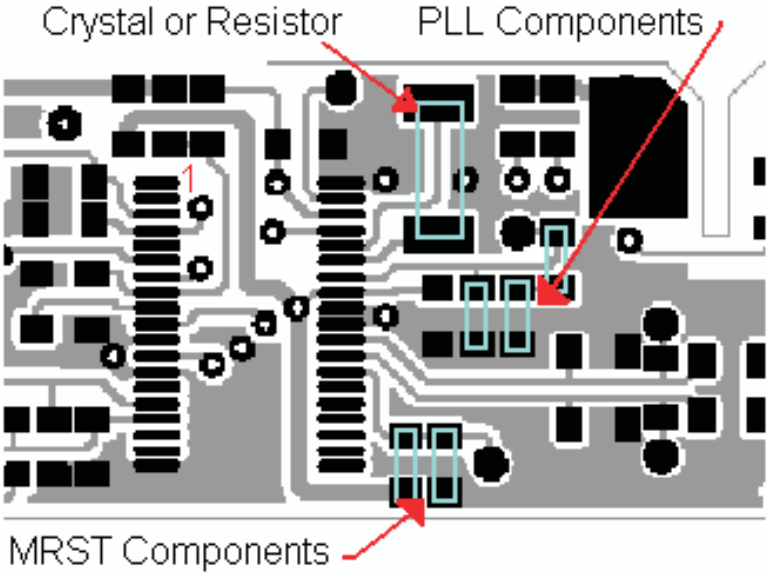


Figure 2. Minimize Length and Loop Area for These Critical Components to Reduce Noise Pickup.

Communication Line Protection Components

The 5.6-V zener diodes, used to protect the communication pins of the bq20z80 from ESD should be located as close to the pack connector as possible. The grounded end of these zeners should be returned to the Pack – node, rather than to the low current digital ground system. Therefore, ESD is diverted away from the sensitive electronics as much as possible.

17.2.114.9 Protector FET Bypass and Pack Terminal Bypass Capacitors The general principle is to use wide copper traces to lower the inductance of the bypass capacitor circuit. In Figure 3, an example layout demonstrates this technique.

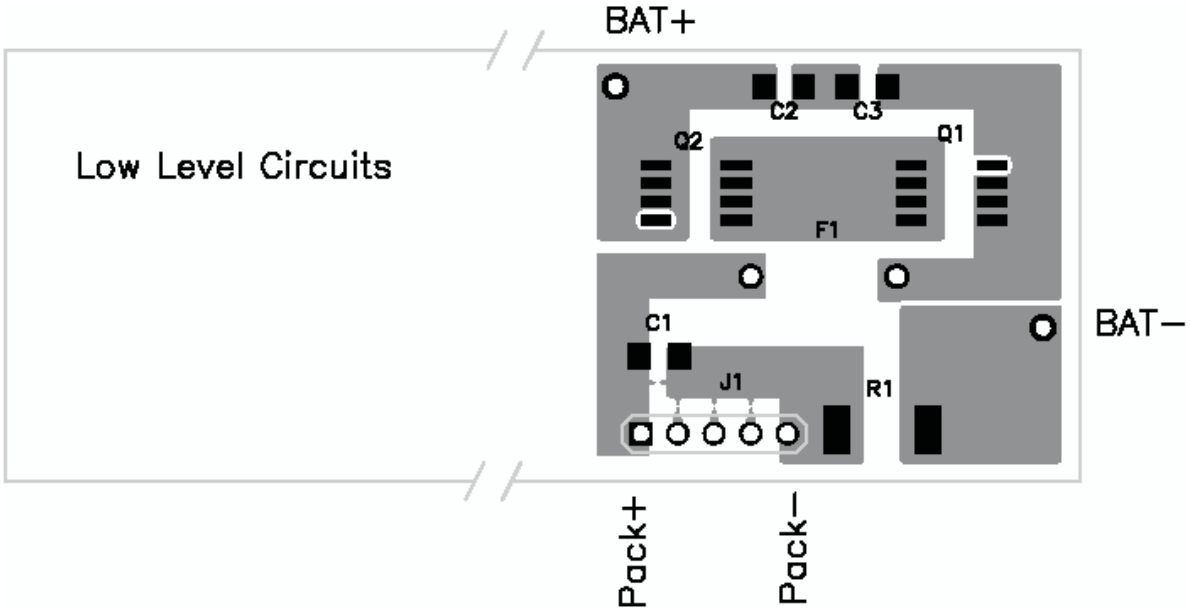


Figure 3. Use Wide Copper Traces to Lower the Inductance of Bypass Capacitors C1, C2, C3.

Ground Systems

The bq20z80 performs optimally when two separate low current ground systems are defined – analog and digital ground. In addition, ESD ground is defined along the high current path from the Pack– terminal to the sense resistor. Refer to the ground symbols in the bq20z80 reference design, and provide separate low current ground systems accordingly. It is important that these two ground systems only connect at the sense resistor Kelvin pick-off point as shown in Figure 4. Use inner layer ground planes, if possible, for each low current ground system.

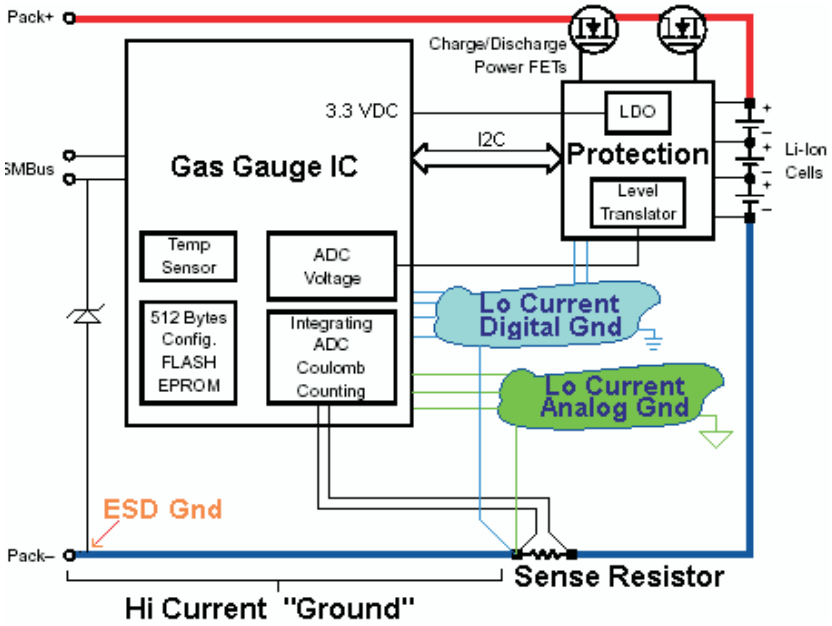


Figure 4. Use Separate Analog and Digital Low-Current Ground Systems

17.3 Kelvin Connections

Kelvin voltage sensing is important in order to accurately measure current, and top and bottom cell voltages. The figures below demonstrate “right” and “wrong” techniques

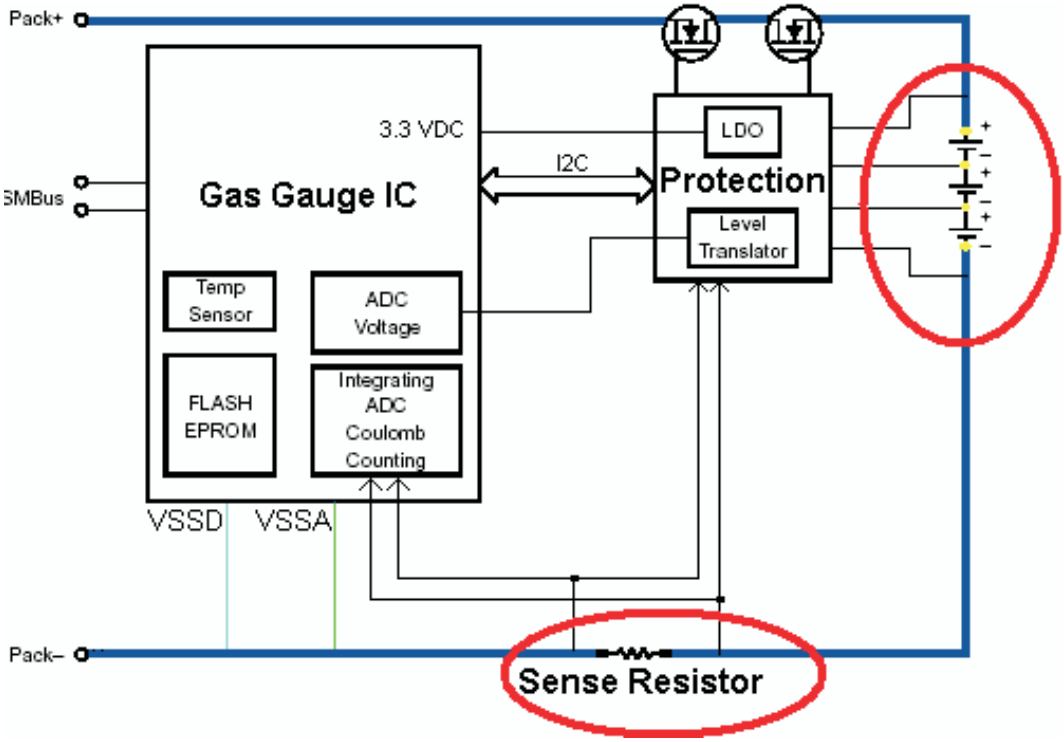


Figure 5. WRONG! Sensing Through High Current Copper Traces Produces Measurement Errors.

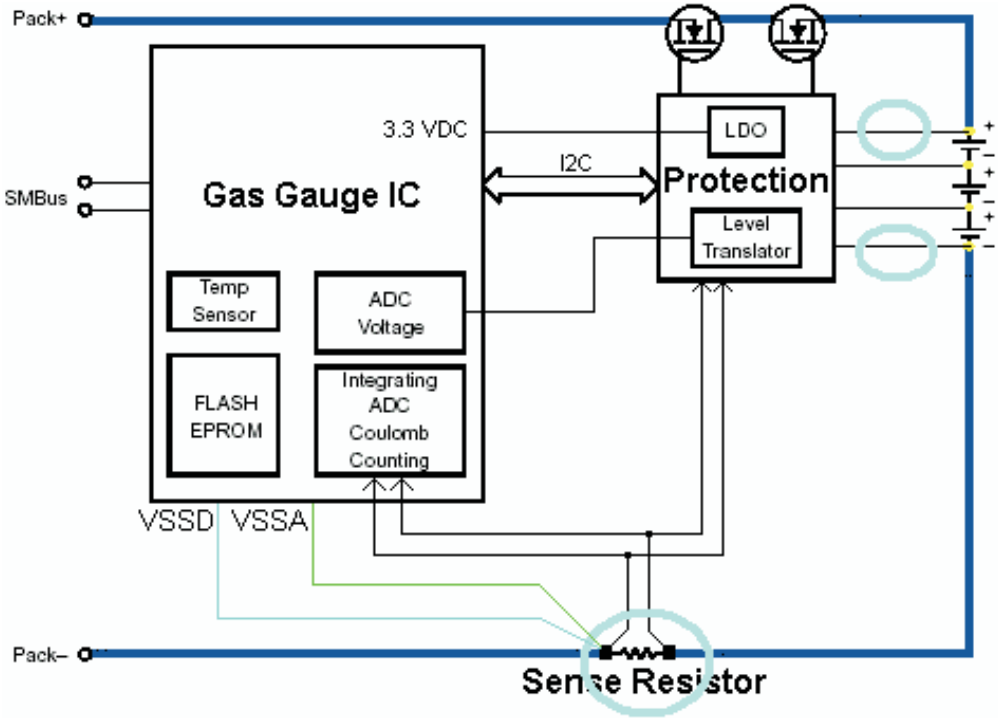


Figure 6. Fig 6. RIGHT! In Some Cases, Top and Bottom Cell Voltage Sensing may be Extended out to the Cells.

17.4 Board Offset Considerations

While the most important component for board offset reduction is the decoupling capacitor for VDDA, an additional benefit is possible by using this recommended pattern for the Coulomb Counter differential low pass filter network. Maintain the symmetrical placement pattern shown for optimum current offset performance. Use symmetrical shielded differential traces, if possible, from the sense resistor to the 100 ohm resistors

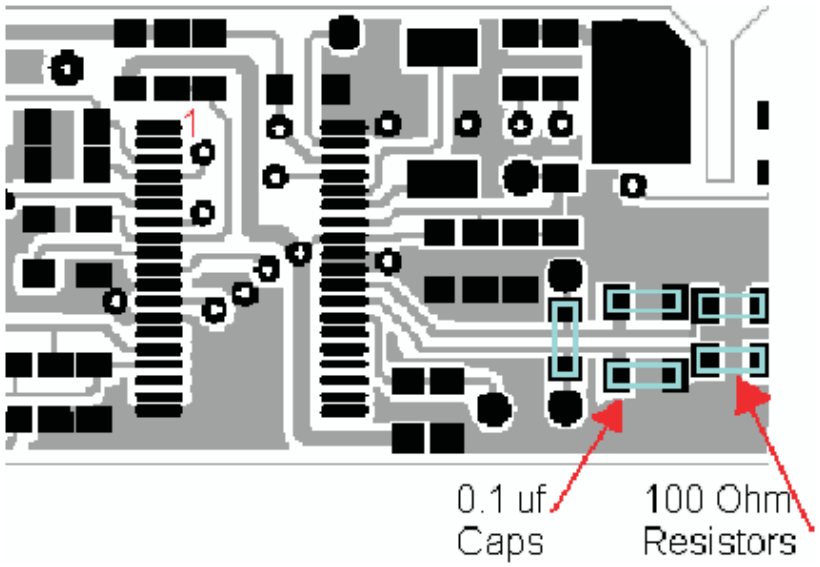


Figure 7. Differential Filter Components With Symmetrical Layout.

17.5 ESD Spark Gap

Protect SMBus Clock, Data, and other communication lines from ESD with a spark gap at the connector. The pattern below is recommended, with 0.2 mm spacing between the points.

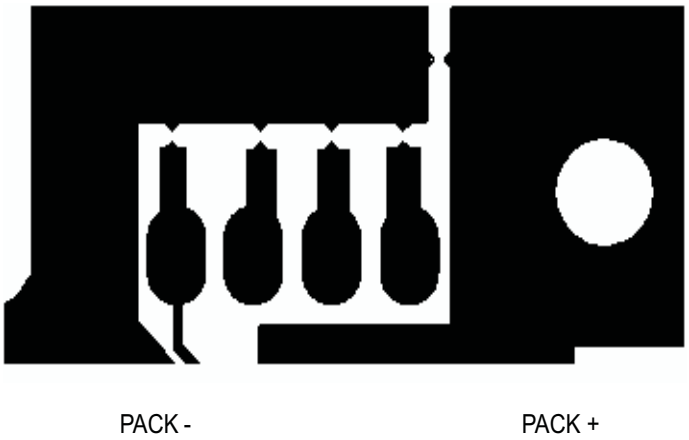


Figure 8. Recommended Spark Gap Pattern Helps Protect Communication Lines From ESD.

17.6 Unwanted Magnetic Coupling

A battery fuel gauge circuit board is a challenging environment due to the fundamental incompatibility of high current traces and ultralow current semiconductor devices. The best way to protect against unwanted trace to trace coupling is with a component placement such as that shown in Figure 3, where the high current section is on the right and electronics devices on the left. This is not possible in many situations due to mechanical constraints. Still, every attempt should be made to route high current traces away from signal traces, which enter the bq20z80 directly. ICs can be damaged due to magnetic and capacitive coupling from the high current path. Note that during current and ESD events, the high current traces appear inductive due to the fast current rise time

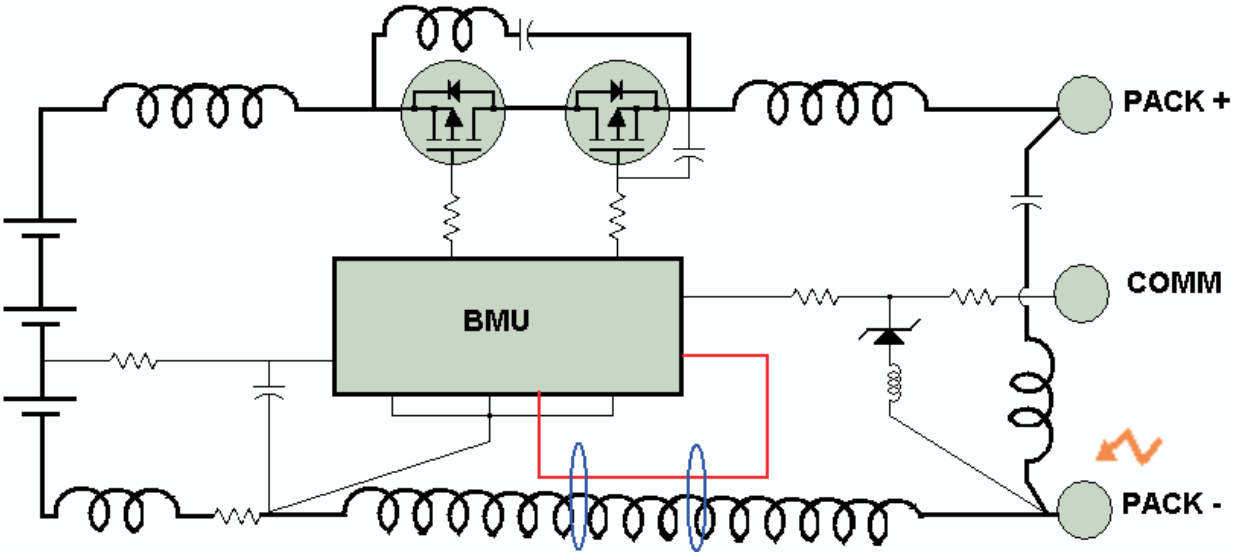


Figure 9. Avoid Close Spacing Between High Current and Low Level Signal Lines

Cell Balancing Using the bq20z80

Yevgen Barsukov *PMP Portable Power*

ABSTRACT

This application report discusses three types of cell imbalances that are observed in a battery pack with serially connected cells.

18.1 Types of Cell Imbalances

1. **State of Charge Imbalance**

   Charging cells to different states of charge (SOC) causes this type of imbalance. For example, given a configuration of 3 x 2200-mAh cells (QMax), if one cell is discharged by 100 mAh (Q1), the second by 100 mAh, and the third by 200 mAh from a fully charged state, the first and second cells' chemical state of charge is (Qmax-Q1)/Qmax = 95.4%, but the third cell is 91%. Therefore, cell 3 is imbalanced by 4.4%.

   This results in a different open-circuit voltage (OCV) for cell 3 compared to cells 1 and 2, because the OCV directly correlates with the chemical state of charge.

2. **Total Cell Capacity Imbalance**

   A specific cell's total chemical capacity, Qmax, initially may be different from the others in the cell package. So, even if all cells were discharged by an equal amount from a fully charged state, their chemical states of charge may be different. Indeed, if all 3 cells are discharged by 100 mAh, but cell 3 has different total capacity (e.g., 2000 mAh), the resulting chemical states of charge is 95.4% and 95%.

   This results in different OCVs. A 200-mAh difference in Qmax causes only a 0.4% difference in SOC because the SOC correlates with voltage. This indicates that the capacity imbalance causes less voltage difference than charge imbalance (cause 1).

3. **Impedance Imbalance**

   Internal impedance differences between the cells (that can be an approximate 15% range in the same production batch) do not cause differences in the OCV. However, they can cause differences in cell voltage during discharge. Indeed, cell voltage can be approximated as $V = OCV + I \times R$. If current is negative (discharge), voltage is lower for a cell with higher R. If current is positive (charge), voltage is higher for a cell with higher R.

   No balancing algorithm can help against resistance imbalance. However, it can significantly distort attempts to balance the SOC. If significant (< 200 mA) current is flowing, attempting to use voltage as a determining factor for passing more charge through a cell with higher voltage, fails to determine if the voltage differences is caused by differences in the SOC or by impedance. If it is caused by impedance imbalance, bypassing more current through this cell results in the opposite effect – increasing the SOC difference from other cells to a larger value than it would be without balancing. As a result, the OCV of this cell at the end of charge is different from the other cells, and can reach high levels, potentially causing the safety circuit to trip.

18.2 Cell Balancing Methods

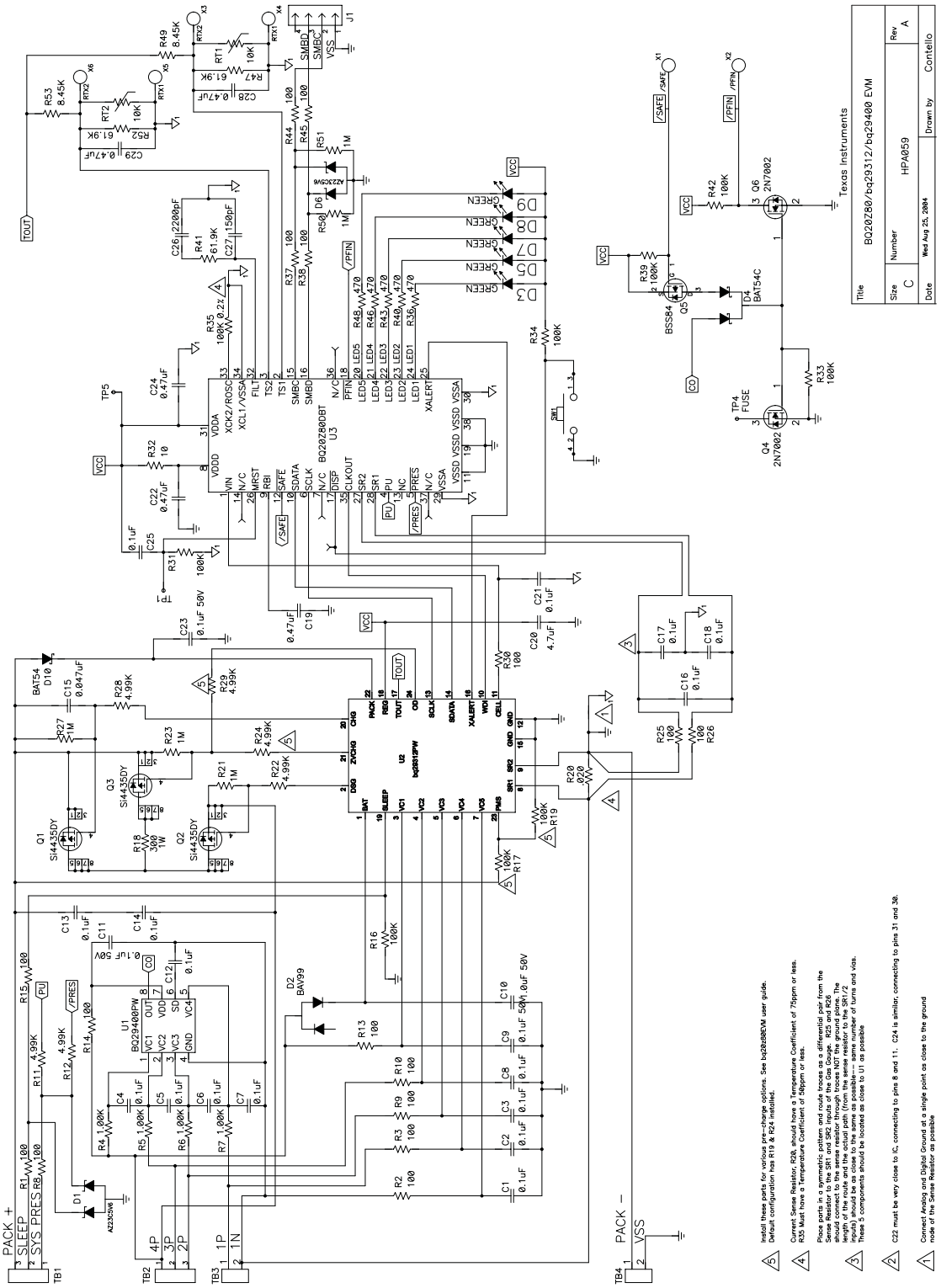
The bq20z80 uses the unique capabilities of Impedance Track™ technology to identify the chemical SOC of each cell, which does not rely on measuring voltage during charge or discharge. This removes the distortion caused by impedance imbalance, and permits precise SOC balancing. The cell-balancing algorithm operates as follows:

1. Determine the initial SOC for each series cell bank separately.
2. Determine the charge needed for each cell to reach a fully charged state.
3. Find the cell requiring the most charge to be fully charged, and then find the differences, dQ, between all the other cells requiring charge and that of the one requiring the most charge.
4. These differences must be bypassed for each “excessive” cell during one or multiple cycles. To achieve this, the bypass FET is turned ON during charging for the calculated duration for each cell bypass time.
5. The bypass time is calculated based on the value of bypass current, which in turn depends on bypass resistance values, R, as time = $dQ \times R / (V \times duty\_cycle)$.
6. R is calculated as the sum of the internal bypass resistor (500 Ω, typical) and the series filter resistors (Rx) leading to the cells. $R = Rx \times 2 + 500$. The resistors in question are R2, R3, R9, and R10. Their default value is 100 Ω, which results in R = 700.

7. The bq20z80 stores the value of R(Ω) × 3.6 / (V × duty_cycle (ratio)) as a flash constant DF.MinCellDeviation (s/mAh). Here, 3.6 is the mAh correction factor. For default values of voltage, V = 3.6 V, R = 700 Ω and duty cycle = 40% (ratio 0.4), the value is calculated as DF.MinCellDeviation = 700 × 3.6 / (3.6 × 0.4) = 1750

This value must be changed if values of resistors R2, R3, R9, and R10 are changed from the default value.

The schematic appears on the following page.


Texas Instruments
Title BQ20Z80/bq29312/bq29400 EVM
Size C
Number HPA059
Rev A
Date Wed Aug 25, 2004
Drawn by Contello
Install these parts for various pre-charge options. See bq20z80EVM user guide. Default configuration has R19 & RC4 installed.
Current Sense Resistor, R20, should have a Temperature Coefficient of 75ppm or less. R35 Must have a Temperature Coefficient of 50ppm or less.
Place parts in a symmetric pattern and route traces as a differential pair from the Sense Resistor to the SR1 and SR2 inputs of the Gas Gauge. R25 and R26 should connect to the sense resistor through traces NOT the ground plane. The length of the route and the actual path (from the sense resistor to the SR1/2 inputs) should be identical and the traces should be routed over Vcell and Vss. These 5 components should be located as close to U1 as possible
C22 must be very close to IC, connecting to pins 8 and 11. C24 is similar, connecting to pins 31 and 30.
Connect Analog and Digital Ground at a single point as close to the ground node of the Sense Resistor as possible
PACK +
SLEEP
SYS PRES
PACK –
VSS
TB1
TB2
TB3
TB4
U1 BQ029400PW
U2 bq2831DPW
U3 BQ20Z80DBT
Q1 Si4435DY
Q2 Si4435DY
Q3 Si4435DY
Q4 2N7002
Q5 BSS84
Q6 2N7002
D1 AZ23C5V6
D2 BAV99
D4 BAT54C
D10 BAT54
D5 GREEN
D6 AZ23C5V6
D7 GREEN
D8 GREEN
D9 GREEN
TP4 FUSE
TP5
SW1
J1 SMBD SMBC VSS
X1 /SAFE
X2 /PFIN
X3 RTX2
X4 RTX1
X5 RTX2
X6 RTX1
TOUT
VCC
CO
/PRES
PU

Support of Multiple Chemistries

19.1 Introduction

Impedance Track™ devices rely on a fixed open circuit voltage (OCV) table to determine the state of dharge (SOC), where OCV (SOC) dependence is defined by cell chemistry. Impedance Track™ devices come preprogrammed to support the most common Li-Ion cells with LiCoO2 cathode and graphitized carbon anode. However, multiple other chemistries are grouped under Li-Ion; two examples of which are Co/Mn oxide cathode cells and Ni/Co/Mn cathode cells. Therefore, Impedance Track™ devices are designed with the ability to be programmed with any Li-Ion chemistry OCV table. The process of selecting the correct chemistry OCV table for a particular cell and the specifics of correctly programming this information during production are described in this document.

19.2 Selection of correct chemistry

Chemistry Selection Table

Chemistries that are presently supported are listed in the Table 1 which can be found on the TI web site, www.ti.com, in the Tools & Software folder of the corresponding Impedance Track™ based device. Below is an example of the table format, which contains a sample of the data available. In the future more entries will be added to the web based table as additional chemistries are identified.

Table 1. Chemistry Selection Table

Description	Chemical ID	Known compatible cells (not exclusive)
LiCoO2/graphitized carbon (default)	0100	Sony US18650S, Sony 18650GR, Moly ICR-18650G, Panasonic CGR-18650C, LG Chem ICR18650A2, LG Chem ICR18650S2, A&TB LGR18650OU, Samsung SDI ICR18650-20
Co/Ni/Mn cathode	0101	Sony SF US18650GR
Hybrid Co/Mn oxide cathode	0102	Sanyo-laminate
LiCoO2 ATL	0103	ATL-laminate 554490

Firmware support for different chemistries

The firmware required to support the various chemistries is identical; therefore, no firmware upgrades are required when programming new chemistries into the data-flash (DF) of the corresponding Impedance Track™ based device. As an added feature, the Chemical ID of presently programmed OCV data can be checked using TI's EV Software. This is accomplished by entering 0008 into the Manufacturer Access field in the SBS screen and pressing <enter>. The Chemical ID is then reported back in the Manufacturer Access field. Note that scanning should be enabled.

Methods to identify chemistry of a particular cell:

1. Ask the manufacturer. If the use of standard LiCoO2 can be assured then the default database with ID 0100 can be used without any changes.
2. Search for the cell part number, in the "Known Compatible Cells" column of the Chemistry Selection table provided by TI. If found, then the corresponding chemistry ID can be used
3. In manufacturer information, search for a "Description" entry similar to that found in the Chemistry Selection table provided by TI. If a similar description is found, then the corresponding chemistry ID can be used.

4. If none of the above applies, then a chemistry selection test can be run to help select the best possible fit. It should be noted that this is the most time consuming option, which requires common charge/discharge test equipment such as a Maccor or Arbin tester. However, it provides the highest confidence in chemical data-base selection process. The chemistry selection test procedure is described in the Addendum “Chemistry Compatibility Check”.

Preproduction testing with nondefault chemistry

Preproduction testing, using a nondefault chemistry, is the same as when using the default chemistry, with one exception—a new firmware file (*.senc) containing OCV table specific for a particular chemistry has to be programmed into the pack first. Firmware files for selected chemistry ID’s can be download from the production folder of corresponding Impedance Track™ based device under power.ti.com (see the source files for application note SLUA372). Programming of the firmware file using TI’s EV Software is described in the chapter *Updating Firmware With The bq20z80 and EVM* (SLUA336).

After the correct firmware file is programmed, the normal production process may proceed using the steps described in *Basic Pack Assembly* (SLAU386). Note that prior to production a relaxation/discharge/relaxation test should be done to acquire optimized parameters to be used. This process is described in the chapter *Preparing Optimized Default Flash Constants For Specific Battery Types* (SLUA336).

Preparing optimized data-flash constants with nondefault chemistry

With the exception of preparing the data flash image file, the production process with nondefault chemistries is the same as with default chemistries, see *Produection Flow with bq20x80* (SLUA385) and *Data Flash Programming and Calibrating the bq20z80 Family of Gas Guages* (SLUA355).

The additional steps required to prepare the data-flash image file are outlined below.

1. Using an Impedance Track™ based device programmed with the corresponding chemistry specific firmware file (*.senc), complete the Battery Pack assembly steps, as outlined in *Basic Pack Assembly* (SLAU386). Keys step include: setting basic flash constants for a given pack configuration; calibrating the pack; connecting System Present to ground; and enabling IT. It is also important to correctly set the parameters specific to the number of serial cells used. This is described in *bq20z80 EVM Data Flash Settings for Number of Serial Cells and Pack Capacity* (SLVA208).
2. Input an initial estimate for QmaxCell 0, Qmax Cell 1, Qmax Cell 2, Qmax Cell 3 and Qmax Pack using the value specified in the battery manufacturer data sheet. For example, if single-cell data-sheet capacity is 2400 mAh and 3 parallel cells are used, set each value to 2400 ´ 3 = 7200 mAh.
3. Charge the pack to full.
4. Let the pack relax for 2 hours.
5. Discharge the pack to the minimum system-acceptable voltage (should be the same as DF:Term Voltage) at the typical application rate. Note that the exact rate is not critical.
6. Let the pack relax for 5 hours.
7. Repeat steps 3 through 6 two times to achieve the maximum accuracy. Using the Data Flash screen in the EVSW, verify that “Update Status”, under the Gas Gauging tab, reads 06. If not, then repeat the cycle.
8. Use the EVSW to export the (.gg) file.
9. Open the (.gg) file with an application like Notepad and manually change the [IT Cfg(Gas Gauging)] “Update Status” to 02 and the [Data(SBS Configuration)] “Cycle Count” to 0. Save and close the (.gg) file
10. Reprogram the pack with a fresh firmware (*.senc) file with selected chemistry ID, to clear all hidden constants and set the correct chemistry specific table.
11. Use the Data Flash screen in the EVSW to import the modified (.gg) file, saved in step 9.
12. In the Data Flash screen of the EVSW click “Write All”.
13. In the Pro screen of the EVSW, send the reset command (0x0041).

The golden pack is now ready to have its data flash read into a binary file, as described in Section 3 of the application note titled *Data Flash Programming and Calibrating the bq20z80 Family of Gas Gauges* (SLUA355).

Note that as an alternative option, small volume production facilities can use TI's single-channel prototype data-flash writing and calibration software called "bqTester". The single site bqTester software can be downloaded directly form the TI web site (see SLUA352). Note that care must be taken to ensure that the correct firmware version is inputted into the bqTester.ini file. For example for bq20z80-v102 set: DEV_VER_REV=800.1.02.

19.3 Chemistry Selection Test

Setup

- Use a single cell, or an assembled battery pack without any electronics connected. This is to avoid any current draw and is important because this test takes an extended amount of time and has long inactivity periods
- Measure the voltage at a single cell (even if a battery pack is used)
- Current measurement accuracy is important. The current offset should be calibrated to better than 1-mA accuracy
- Voltage measurement accuracy is equally important and should be accurate to 1mV (should be checked with a 0.1-mV accurate digital voltmeter)
- Configure a thermal chamber to 25°C. Note that testing at 0°C and 50°C are also required in order to create a database, but not for compatibility check
- Voltage, current and temperature data should be collected with 10sec - 100 sec intervals continuously during the test. The resulting file is used in the chemistry selection tool. Plain text files or excel spreadsheets are acceptable formats

Automated Test (can be set up using Maccor or Arbin battery testers):

1. Charge the cell to full using the CC/CV method and terminate the charge when taper current reaches C/100. This state of charge corresponds to full chemical capacity. Note that using the C/100 taper current is critical to ensuring an absolutely fully charged cell.
2. Turn off the current (make sure actual current is below 1 mA) and wait 5 hours for full cell relaxation. If dV/dt smoothed over 100 seconds is available, wait can be terminated before 5 hours if dV/dt < 1 µV/sec. This method helps speed up testing
3. Discharge at C/20 rate for 1 hour, than go to step 2. If voltage goes below 3 V, go to step 4.
4. Turn off current (make sure actual current is below 1 mA) and wait 5 hours for full relaxation. If dV/dt smoothed over 100 sec is available, wait can be terminated before 5 hours if dV/dt < 1 µV/sec. This method helps speed up testing. Check voltage after relaxation is terminated. If V < 3 V, exit test otherwise proceed to step 5.
5. Discharge at C/60 rate for 30 min, or until V < 2.7 V, go to step 4.

Data obtained in this test is used in a MathCad tool provided by TI. For database purposes, additional data at 0°C and 50°C is needed.

Using the MathCad tool to select battery chemistry

To use the chemistry selection tool, MathCad 2001i or higher is needed.

Download the chemistry selection worksheet "chemselect.mcd" from the Tools & Software folder of the corresponding Impedance Track™ based device and then follow these steps to verify battery chemistry:

1. Remove the charge portion of the data-file acquired in the above testing
2. Place the file in the same directory as the "chemselect.mcd" file
3. The chemistry selection file "chemselect.mcd"
4. Assign columns to reflect your file format:

Common assignment in data-file:	time	tn:=0	voltage	vn:=2	temper	ttn:=100	curr	in:=1	

Change the column numbers for time (tn), voltage (vn), temperature (ttn) and current (in). If temperature column is not available, set ttn:=100 and set correct chamber temperature in °C in the following section:

Temperature used in simulation of voltage if no temperature is present in file. Set ttn=100 if not temperature info present	T:=25 Tpress:=T . 10

5. Enter your file name into data-loading section. You can try running the program with included example data-file “tIV_example.dat.”

Data import: load tVIT file	Plain text	A:=READPRN("tIV_example.dat"
	Excel +	A:= some_excel_fle.xls 

If the file is in excel format, then right-click on the section to the right labeled "Excel" line, and click "enable evaluation". If the file is in plain-text format, leave this section disabled. Note that regardless, the file should not include any text headers, only data!

6. Scroll to the bottom of document and click anywhere to place the cursor below all lines. Press F9 to execute all calculations.
7. Read out the chemical ID best suited for your battery:

Best Chemistry ID	bestchem = 103

8. Analyze the reported error for best chemistry (on the top of the matrix). If it does not exceed 3%, this chemical ID firmware can be used with your chemistry:

Error % ID	maxerr =	1.96682	103
		3.937942	100
		9.521751	101
		17.384558	102

In this example, the max error is 1.96% for chemical ID 103 where anything below 3% is acceptable. Therefore, the firmware file (*.senc) for chemical ID 103, should be downloaded and used.

If “maxerrr” for all chemical ID’s exceeds 3% a new chemical table must be created. To help facilitate this, repeat the “Automated test” for the additional required temperatures of 0°C and 50°C. Then contact Texas Instrument support at http://www-k.ext.ti.com/sc/technical-support/product-information-centers.htm or the local sales representative. Using this data TI will create a new chemical database. Alternatively the cells may be sent directly to TI for evaluation/characterization but this process will take longer

Production Flow with bq20z80 Gas Gauges

20.1 Preproduction steps

Before production, the followings steps must be finalized

1. Design and testing of the PCB
2. Choice of the data-flash constants providing the desired functionality (most important, settings for number of serial cells and capacity)
3. The optimal value of the board offset should be found by characterizing several packs, see “calibration” (SLUA386).
4. The optimization cycle should be done on one battery pack for preparing optimized battery model related data-flash parameters as described in (SLUA334) “preparing optimized data-flash constants”
5. The data-flash image file (golden image) should be prepared using the bqTester or custom software as described in *Using the bqTester Software chapter to calibrate PCB* (SLUA352).

20.2 Typical production flow (some other custom steps can be added)

1. Assemble the PCB
2. Functionality test:

   Test the PCB for functionality of critical elements (ICs, FETs, Fuse blowing circuit). If necessary, the FET ON/OFF status can be controlled using command 46. To prevent data-flash corruption, do not enable IT at this stage .
3. Write data flash and calibrate:

   Use the previously created golden image with optimized data-flash constants , made as described in SLUA352 to calibrate the PCB. A multy-channel version of bqTester is also available. Alternatively, use a custom made software as described in *Data Flash Programming/Calibrating the bq20z80 Gas Gauges* (SLUA355).
4. Connect the cells to the PCB.
5. Send the IT enable command (Manufacturer Access 0021).

   This step starts the fuel-gauging and Life Time Data update. It should not be made until cells are connected. If cells were disturbed by charge or discharge testing during some previous steps, at least 30 min should pass before IT is enabled to assure that the open circuit voltage is stabilized.
6. Short discharge test:

   If the battery is removable (NR bit in DF.Op.Config B is 0), short the System Present pin to the ground to emulate battery insertion into system. If NR bit is 1, above is not needed. Connect the typical load for short time (1-2 seconds) to check that the battery can be discharged as expected. This tests correctness of data-flash programing and FETs functionality. It is not required for the gas-gauge functionality.
7. Check the reported RSOC by pushing the LED button. Typicaly, cells are in the 50% charged state, so half of the LEDs should light up.
8. Send the “seal” command to block assess to the data-flash (Manufacturer Access 0x0020). Note that after giving this command at least once, pack is unsealed by using the unseal code, but it reseals itself upon reset.
9. Before shipment and long storage, it use the “shut down” command (Manufacturer Access 0x0010), which causes GG to shut-down (lowest power mode) until the next application for the charger volage to Pack+ and Pack-.

Chapter 21

Data Flash Programming and Calibrating the bq20z80 Family of Gas Gauges

Doug Williams *High Precision Analog*

ABSTRACT

This application report presents a strategy for high-speed, economical calibration and data flash programming of the bq20z80 advanced gas gauge chipset family. VB6 code examples are provided, along with step-by-step instructions for preparing a golden battery pack.

21.1 Introduction

The bq20z80 family of advanced gas gauges is built with new technology and a new architecture for both data flash access and calibration. With this new architecture, unit production cost and capital equipment investment can be minimized, as there is no longer a need to perform a learning cycle on each pack. A single “golden pack” can become the source of data for all other packs. A method is shown to quickly read and write the golden image. Also, the calibration method is now quick and simple because the calibration routines are built into the firmware of the target device.

The methods in this document are presented as VB6 (Visual Basic 6) functions. These functions were copied directly from working code. In order to read from and write to the data flash, they use five types of SMBus read and write functions. These can be duplicated in any software environment that has SMBus communication capabilities. As used herein, each Read/Write function is designed for communication with a gas gauge, so the device address (0x16) is omitted for clarity.

1. WriteSMBusInteger() has two arguments – the SMBus command and a signed integer. Internally, this function separates the integer into two bytes for transmission by the SMBus write-word protocol.
2. WriteSMBusByteArray() has three arguments – the SMBus command, the array of bytes and an integer specifying the length of the byte array. Internally, this function separates the byte array into separate bytes for transmission by the SMBus write-block protocol.
3. WriteSMBusCommand() has only one argument – the SMBus command.
4. ReadSMBusWord() has three arguments – the SMBus command, the returned upper byte and returned lower byte. This one is especially useful for reading specific bit patterns.
5. ReadSMBusByteArray() has three arguments – the SMBus command, the returned array of bytes, and the returned length of the byte array. It is internally implemented with the SMBus read-block protocol.

Also used in these functions is a simple delay routine called DoDelay. VB6 code for this procedure is provided at the end of the document.

Error handling is not implemented in this sample code, because requirements are unique and varied. Also, constants are hard-coded into the functions to improve clarity rather than documenting them in code elsewhere as would normally be good coding practice.

A good strategy for production is a seven-step process flow:

1. Write the data flash image to each device. This image was read from a *golden* pack.
2. Calibrate the device.
3. Update any individual flash locations, such as serial number, lot code, and date.
4. Perform any desired protection tests.
5. Connect the cells.
6. Initiate the Impedance Track™ algorithm
7. Seal the pack.

In this document, the first three steps are examined in detail.

21.2 Preparing the Golden Pack

Impedance Track™ technology allows the bq20z80 gas gauge to automatically acquire and maintain parameters for battery modeling needed for continuous accuracy, regardless of battery model or manufacturer. The ICs are shipped preprogrammed with default values for these parameters. In the course of daily use (charge, discharge, unused), the algorithm collects new parameters. Parameter acquisition is complete after one full discharge cycle and subsequent relaxation takes place.

The default parameters that are used for fuel gauging prior to discharge activity are less accurate than parameters acquired during such activity. Therefore, the error of the gas gauge is more than the 1% that is achieved after parameter acquisition. It is desirable to have optimal accuracy in the battery packs coming from the production line even before any discharge activity occurs. This can be accomplished by performing a discharge cycle on one battery pack (let it acquire optimized parameters), save its data flash in a file, and then program the golden data into all battery packs coming from the production line.

Creating Pre-Learned Defaults

1. Assemble a battery pack with the bq20z80 solution, which includes setting basic flash constants for a given pack configuration, calibrating the pack, connecting *System Present* to ground, and enabling IT. This is described in detail in the application report *Pack Assembly and the bq20z80* (SLUA335).
2. In particular, it is important to set parameters specific to the number of serial cells used. This is described in application report *bq20z80 EVM Data Flash Settings for Number of Serial Cells and Pack Capacity* (SLVA208).
3. To achieve maximum accuracy of first cycle parameter acquisition, set an initial guess for Qmax Cell 0, Qmax Cell 1, Qmax Cell 2, Qmax Cell 3 and Qmax Pack. These values are in mAh as specified in the battery manufacturer data sheet. For example, if single-cell data-sheet capacity is 2400 mAh and 3 parallel cells are used, set each value to 2400 × 3 = 7200 mAh.
4. Charge the pack to full.
5. Let it relax for 2 hours.
6. Discharge the pack to the minimum system-acceptable voltage (should be the same as DF.Gas Gauging.IT Cfg.Term Voltage) at the typical application rate. The exact rate is not critical.
7. Let it relax for 5 hours.
8. Repeat steps 4 through 7 to achieve maximum impedance table accuracy. Verify that DF.Gas Gauging.State.Update Status reads 06. If not, repeat the cycle. Its normal value should be 06.
9. Use the EVSW to export the .gg File. Open the .gg file with Notepad to change DF.Gas Gauging.State.UpdateStatus to 02. Change DF.SBS Configuration.Data.Cycle Count to 0.
10. Reprogram the pack with a fresh .srec or .senc to clear all hidden constants.
11. Use the EVSW to import the modified .gg file as saved in step 9. Write All.
12. Send reset command (0x0041).

The *golden pack* is now ready to have its data flash read into a binary file as described in the function listed in Section 3.

21.3 Reading and Saving the Data Flash Image From the Golden Pack

Note that this step only needs to be done once for a given project.

```
Function SaveDataFlashImageToFile(sFileName As String) As Long

    Dim iNumberOfRows As Integer
    Dim lError As Long
    Dim yRowData(32) As Byte
    Dim yDataFlashImage(&H700) As Byte
    Dim iRow As Integer
    Dim iIndex As Integer
    Dim iLen As Integer
    Dim iFileNumber As Integer

    '// FOR CLARITY, WITHOUT USING CONSTANTS
    '// 0x700 is the data flash size for bq8024-based devices (eg: bq20z80). 0x700 \ 32 = 56 rows
    iNumberOfRows = &H700 \ 32

    '// PUT DEVICE INTO ROM MODE
    lError = WriteSMBusInteger(&H0, &HF00)
    DoDelay 0.01

    '// READ THE DATA FLASH, ROW BY ROW
    For iRow = 0 To iNumberOfRows - 1

        '// Set the address for the row. &H9 (0x09) is the ROM mode command.
        '// 0x200 is the row number where data flash starts.
        '// Multiplication by 32 gives us the actual physical address where each row starts
        lError = WriteSMBusInteger(&H9, (&H200 + iRow) * 32)

        '// Read the row. &HC (0x0c) is the ROM mode command.
        lError = ReadSMBusByteArray(&HC, yRowData, iLen)

        '//Copy this row into its place in a big byte array
        For iIndex = 0 To 32 - 1
            yDataFlashImage((iRow * 32) + iIndex) = yRowData(iIndex)
        Next iIndex
```

```
        Next iRow
        '// WRITE DATA FLASH IMAGE TO FILE
        iFileNumber = FreeFile
        Open sFileName For Binary Access Write As #iFileNumber
        Put #iFileNumber, , yDataFlashImage
        Close #iFileNumber
        '// EXECUTE GAS GAUGE PROGRAM
        lError = WriteSMBusCommand(&H8)
    End Function
```

21.4 Writing the Data Flash Image to Each Target Device

The following method is fast. It only takes about 2 seconds to write the entire data flash in this manner.

CAUTION
If power is interrupted during this process, the device may become unusable.

```
Function WriteDataFlashImageFromFile(sFileName As String) As Long

Dim lError As Long
    Dim iFileNumber As Integer
    Dim iNumberOfRows As Integer
    Dim iRow As Integer
    Dim iIndex As Integer
    Dim yRowData(32) As Byte
    Dim yDataFlashImage(&H700) As Byte

    '// READ THE FLASH IMAGE FROM THE FILE INTO A BYTE ARRAY
    iFileNumber = FreeFile
    Open sFileName For Binary Access Read As #iFileNumber
    Get #iFileNumber, , yDataFlashImage
    Close #iFileNumber

    '// FOR CLARITY, WITHOUT USING CONSTANTS
    '// 0x700 is the data flash size for bq8024-based devices (eg: bq20z80). 0x700 \ 32 = 56 rows
    iNumberOfRows = &H700 \ 32

    '// PUT DEVICE INTO ROM MODE
    lError = WriteSMBusInteger(&H0, &HF00)
    DoDelay 0.01

    '// ERASE AND WRITE EACH ROW
    For iRow = 0 To iNumberOfRows - 1

        '// Set the row to program
        yRowData(0) = iRow

        '// Copy data from the full array to the row array
        For iIndex = 0 To 31
            yRowData(iIndex + 1) = yDataFlashImage((iRow * 32) + iIndex)
        Next iIndex

        '// Erase the row
        lError = WriteSMBusInteger(&H11, iRow)
        DoDelay 0.01

        '// Write the row. Length is 33 because the first byte is the row number
        lError = WriteSMBusByteArray(&H10, yRowData, 32 + 1)
        DoDelay 0.01

    Next iRow

    '// EXECUTE GAS GAUGE PROGRAM
    lError = WriteSMBusCommand(&H8)

End Function
```

21.5 Calibration

Devices in the bq20z80 family of advanced gas gauges are quick and easy to calibrate. It only takes about 3 seconds to accurately calibrate offsets, voltage, temperature, and current. With the Impedance Track™ devices, the calibration routines have been incorporated into firmware algorithms, which can be initiated with SMBus commands. The hardware for calibration is also simple. One current source, one voltage source, and one temperature sensor are all that is required. The accuracy of the sources is not important, only their stability. However, accurately calibrated reference measurement equipment should be used for determining the actual arguments to the function. For periodic voltage measurement, a DVM with better than 1-mV accuracy is required.

The elapsed time for calibration can be changed by modifying values in the data flash, but this is not recommended. Use the default values for the times in DF.Calibration.Config

In the CalibrateAll( ) function, command 0x51 is used to setup a complete calibration of the device. Pack voltage calibration is generally not performed because its accuracy is not required for standard applications. In this case, Pack Voltage refers to a separate measurement of the voltage at the pack terminal and is unrelated to the SBS.Voltage( ) measurement.

The definition of the bits in command 0x51 are:

Bit 0	**Coulomb Counter Offset**	**Bit 8**	**Pack Gain**
Bit 1	**Board Offset**	**Bit 9**	**Pack Voltage**
Bit 2	**ADC Offset**	**Bit 10**	**AFE Error**
Bit 3	**Temperature, Internal**	**Bit 11**	**Reserved**
Bit 4	**Temperature, External 1**	**Bit 12**	**Reserved**
Bit 5	**Temperature, External 2**	**Bit 13**	**Reserved**
Bit 6	**Current**	**Bit 14**	**Run ADC Task Continuously**
Bit 7	**Voltage**	**Bit 15**	**Run CC Task Continuously**

Bits 14 and 15 should always be set. These cause the Coulomb Counter and ADC tasks to run continuously, just as they do in normal operation. This has been found to increase the accuracy of the calibration.

After command 0x51 is issued, the calibration sequence is started in the firmware of the gas gauge. The calibrations are run in sequence starting from the least significant bit. Then, command 0x52 is used to poll these bits, which change from high to low as the tasks are completed. However, bits 14 and 15 do not change; hence, the masking of them in the polling loop.

It can be seen from this code that a simple modification to command 0x51 would allow it to work as a single function calibration. For example, to only calibrate voltage, only bit 7 could be set.

```
Function CalibrateAll(iVoltage As Integer, iCurrent As Integer, iTemperature As Integer, iCells
As Integer) As Long
'// iVoltage is in millivolts
'// iCurrent is in milliamps (normally negative, such as -2000)
'// iTemperature is in Kelvin/10 units, so the argument is: 10 * (Celsius + 273.15)
    Dim lError As Long
    Dim bDoingCal As Boolean
    Dim yLS As Byte
    Dim yMS As Byte
    '// GO TO CALIB MODE
    lError = WriteSMBusInteger(&H0, &H40)
    '// WRITE THE NUMBER OF CELLS
    lError = WriteSMBusInteger(&H63, iCells)
    '// WRITE THE ACTUAL VOLTAGE, CURRENT & TEMPERATURE
    lError = WriteSMBusInteger(&H60, iCurrent)
    lError = WriteSMBusInteger(&H61, iVoltage)
    lError = WriteSMBusInteger(&H62, iTemperature)
    '// START CALIBRATION
    '// Useful cal lo byte  &HD5 - External temperature sensor 1
    '//                     &HF5 - External temperature sensor 1 and 2
    '//                     &HCD - Internal temperature sensor
    lError = WriteSMBusInteger(&H51, &HC0D5)
    '// POLL STATUS
    bDoingCal = True
    While bDoingCal
        lError = ReadSMBusWord(&H52, yMS, yLS)
        bDoingCal = (yMS And &H3F) Or yLS
        DoDelay 0.2 '// check every 200 millisecond
    Wend
    '// TRANSFER RESULTS TO DATAFLASH
```

```
    lError = WriteSMBusCommand(&H72)
    DoDelay 0.1 '// Insure write process is finished

    '// EXIT CALIB MODE
    lError = WriteSMBusCommand(&H73)

    End Function
```

21.6 Writing Pack-Specific Data Flash Locations

The third step is to fine tune the data flash a little for each pack, to give it a unique identity. In the following example, the pack Serial Number is written using subclass and offset information found in the gas gauge product data sheet. Modifications to single data flash locations normally require a block read of the 32-byte data flash page, then updating the desired element of the block, and writing it back to the device. This procedure is documented in the product data sheet.

```
Function WritePackSerialNumber(iSerialNumber As Integer) As Long

Dim lError As Long
    Dim yData(32) As Byte
    Dim iLen As Integer

    '// SET THE SUBCLASS TO 48 (FOUND IN PRODUCT DATASHEET)
    lError = WriteSMBusInteger(&H77, 48)

    '// READ THE PAGE
    lError = ReadSMBusByteArray(&H78, yData(), iLen)

    '// REPLACE THE TWO BYTES AT OFFSET 12 (FOUND IN DATASHEET) WITH NEW S/N
    yData(12) = (iSerialNumber And &HFF00) \ 256 '// modify MS byte
    yData(13) = iSerialNumber And &HFF '// modify LS byte

    '// WRITE THE PAGE BACK TO FLASH
    lError = WriteSMBusByteArray(&H78, yData(), iLen)

    '// FLASH WRITES ARE SLOW
    DoDelay 0.1

End Function

Sub DoDelay(fWaitTime As Single)
    Dim vTime As Variant

 vTime = Timer
    While Timer < (vTime + fWaitTime)

        '// fix midnight problem
        If Timer < vTime Then Exit Sub

        '// Yield to various Windows events while the delay is in progress
        DoEvents

    Wend

End Sub
```

Chapter 22

Using the BQTester Software

Gregory Grant *PMP Portable Power*

ABSTRACT

This application report describes the installation, setup, and testing of the BQTester software. This software is used to calibrate and program electronic smart battery modules based on the bq20z80 battery gas gauge IC.

22.1 Features and Specifications

Introduction

The BQTester software from Texas Instruments (TI) is designed to calibrate and program electronic smart battery modules based on the bq20z80 and future advanced battery gas gauges. The BQTester works with the TI EV2300 USB-based PC interface board for battery fuel gauge evaluation. The BQTester is open-source software and can be modified to suit the user's requirements.

Features

- Programs and calibrates smart battery modules based on the bq20z80
- Calibrates coulomb counter offset, voltage, temperature, and current
- Programs serial number, date, pack lot code, and other defaults obtained from a *gold* data flash file
- Test software is Windows™ 2000 and Windows XP compatible.
- Data-logging feature preserves calibration records.

22.2 Installation and Setup

Minimum System Requirements

- Computer: PC or compatible
- Operating System: Windows 2000, or Windows XP. Operation with Windows 98SE may be possible but is untested and unsupported.
- Minimum video resolution is 640x480; recommended: 800x600 or above
- 1 available USB port
- 1 EV2300 USB-based PC interface board for battery fuel gauge evaluation from Texas Instruments
- 5-MB available hard drive space
- bq20z80 bqEVSW must be installed. (for .ocx and .dll installation)
- VBRuntime (downloadable from Microsoft™) must be installed.
- Visual Basic version 6.0 with Service Pack 5 is required if user wishes to alter program operation.

Software Installation

- Download VBRuntime from www.microsoft.com, and install.
- Install bq20z80 EV software. This software can be downloaded from www.ti.com. For instructions on EV software installation, see user's guide *bq20z80EVM-001 SBS 1.1 ImpedanceTrack™ Technology Enabled Battery Management Solution Evaluation Module* (SLUU205) .
- Unzip bqtester.zip into a directory of your choice. This file can be downloaded from www.ti.com.

Double-click BQTester.exe to run the BQTester software. If the user wishes to modify the BQTester source code, follow these steps to install the source code:

- Unzip bqtestersource.zip into a directory of your choice. Contact Texas Instruments for access to this file.
- Install Visual Basic 6.0 and Service Pack 5 according to the instructions which come with the software.
- Run Visual Basic 6.0 and select File:Open Project. When the dialog box opens, navigate to the directory where bqtestersource.zip was unzipped and choose the file named BQTester.vbp.
- Make desired changes, and recompile.

Interface Connections

The BQTester software requires that the TI EV2300 USB-based PC interface board for battery fuel gauge evaluation interface be installed and running properly. The smart battery module should be connected to the EV2300 board and external power supplies as shown in Figure 1.

> Do not use actual battery cells with this software. Cells should be simulated with resistors as shown in Figure 1.

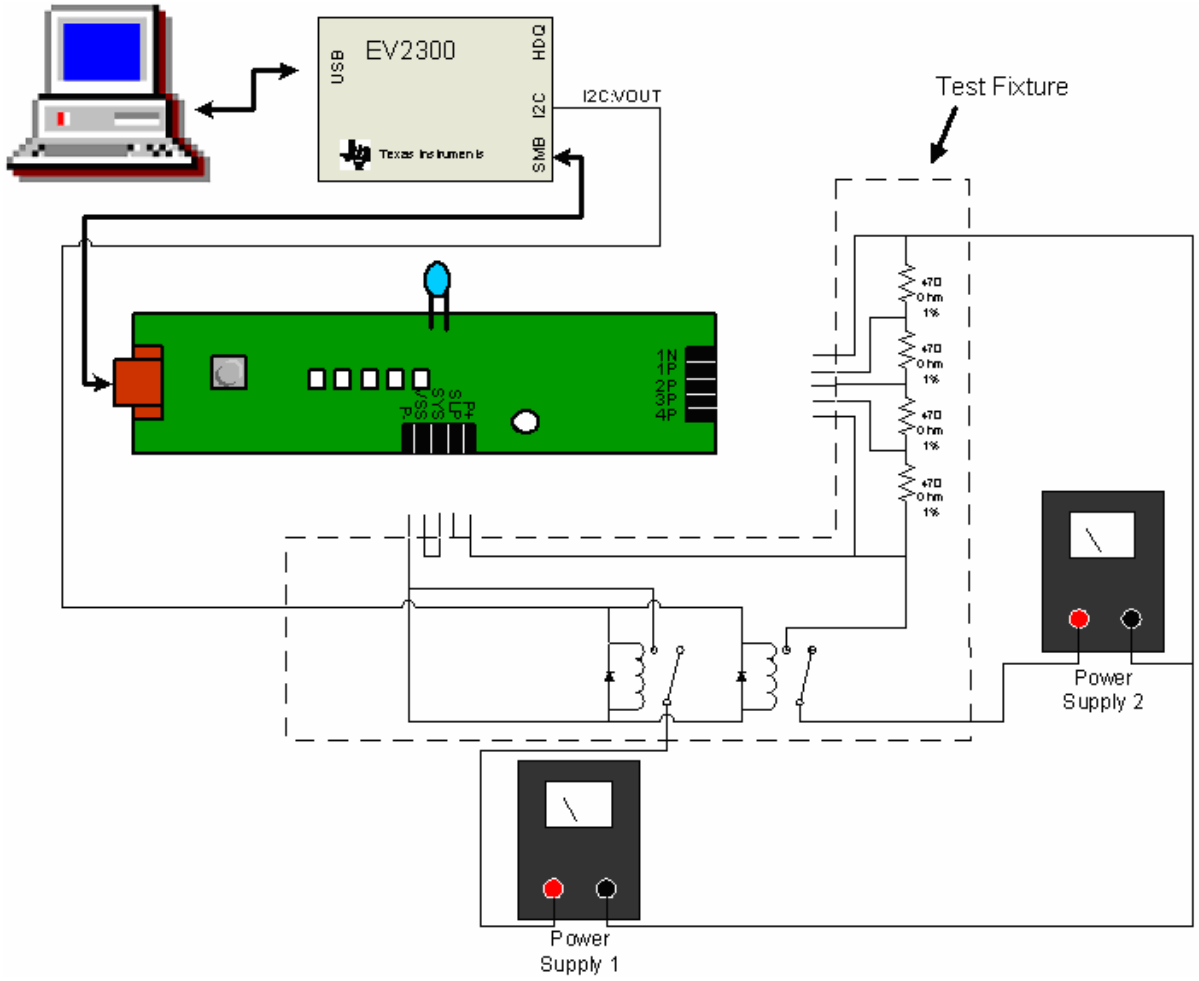


Figure 1. EV2300/Smart Battery Module Connections

The relays used to validate this procedure are 10-A, 250-Vac relays with a 5-Vdc coil. Any brand can be used but the ones used during this test were Omron model G6RN-1. The diodes used were 1N4148. Set Power Supply 1 to 3 Vdc and limit current to 2 A dc. Set Power Supply 2 to the voltage corresponding to the number of cells being simulated (e.g., 10.8 Vdc for 3 cells or 14.4 Vdc for 4 cells). A calibrated temperature probe also is needed to measure the actual temperature.

22.3 Testing

Creating a Gas Gauge Gold Data Flash File

A *gold* data flash file must be made to use as a default to program bq20z80-based smart battery modules. Follow these steps to create this file:

1. Ensure that the EV2300 and bq20z80-based smart battery module are connected as shown in Figure 1 and that all power supplies are turned on.
2. As an option for greater initial accuracy, see application report *Preparing Optimized Default Flash Constants For Specific Battery Types* (SLUA334) for instructions to make an optimized gg (gas gauge) file. If increased initial accuracy is not desired, ensure that the connected bq20z80-based smart battery module contains all desired configuration settings, and proceed to step 5.
3. Reset the *cycle count* field to 0 in the gg file created in step 2. To reset this field, open the gg file with a text editor such as Notepad, scroll down to the *cycle count* field, change from its current value to 0, and save the file.
4. Once the user has created the gg file in step 2 and edited the *cycle count* field in step 3, a new senc

file (1) should be written to the bq20z80 using the procedure given in the application report *Updating Firmware With the bq20z80 and EVM* (SLUA336). Note that: this step is included to ensure that private values unseen by the user are reset to default values.

5. Write the gg file created in steps 2 and 3 to the bq20z80 using the bq20z80 EV software. This can be accomplished by starting the EV software, clicking the *Data Flash* button on the left of the screen, choosing File:Import…. from the menu at the top, selecting the name of the gg file created in step 2, and then clicking the *write all* button.
6. Run the BQTester software by double-clicking the BQTester.exe file in the directory where it was unzipped. Choose File:Read Data Flash Image… from the top menu in the BQTester software. Type in a complete path and file name with a .rom extension in the dialog box that opens. This causes the software to read the data flash information from the bq20z80-based smart battery module and store it in this file. This .rom file is the *gold* data flash file which is used to program all other similar bq20z80-based smart battery modules.
7. Click the *configuration* button on the BQTester software main screen. Enter the full path and file name to the *gold* data flash file in the *Data Flash Image File* box.

(1) A senc file is an encrypted srec file; a srec file is a record file. The srec contains the firmware for the gas gauge.

Setting Configuration Values

In the configuration screen, all numeric values are specified in signed decimal except for the serial number field which is unsigned with a maximum value of 65535.

22.3.131.10 CC Offset Calibration This is the coulomb counter offset. No user-definable values are in this box. Select this calibration by placing a check in its selection box, or deselect it by removing the check. The default is checked. Note that if this test is disabled, the values from the *gold* data flash file are used and not the values currently in the part.

22.3.131.11 Voltage Calibration This box shows the currently measured voltage and provides a box for the user to enter the actual voltage being supplied to the part as measured by a calibrated meter. It also has a box for the user to enter the number of series cells being simulated. The default number of cells is 4. It also has a FET Control selection box. Select *Off (Batt)*, and supply voltage to the simulation resistors as shown in Figure 1 (this configuration is the default). Never select*On (Pack)*; it is only included for possible future use. To select voltage calibration, place a check in its selection box, or deselect it by removing the check. The default is checked. Note that if this test is disabled, the values from the *gold* data flash file are used and not the values currently in the part.

22.3.131.12 Temperature Calibration This box shows the currently measured temperature and provides a box for the user to enter the actual temperature as measured by a calibrated meter. If the ambient air temperature changes, this value needs to be updated. This box also offers three different temperature probe selections. The proper selections should be made depending on the application. Temperature calibration can be selected by placing a check in its selection box or deselected by removing the check. The default is checked. Note that if this test is disabled, the values from the *gold* data flash file are used and not the values currently in the part.

22.3.131.13 Pack Current Calibration This box shows the currently measured current and provides a box for the user to enter the actual current being supplied to the part as measured by a calibrated meter. It also has a FET Control selection box. Always select *On (External Load)* and supply current to the Pack– and 1N (Batt–) inputs of the bq20z80-based smart battery pack as shown in Figure 1 (this configuration is the default). Never select *Off (Bypassed)*; it is only included for possible future use. To select Pack Current calibration, place a check in its selection box, or deselect it by removing the check. The default is checked. Note that if this test is disabled, the values from the *gold* data flash file are used and not the values currently in the part.

22.3.131.14 Current Sense Resistor This box contains two values. Enter the value of the sense resistor used in the bq20z80-based smart battery pack in the *Sense Resistor* field. This value is entered in units of milliohms. Enter the desired acceptable percent error that the sense resistor can differ from the value listed in the *Sense Resistor* field in the *% Error* field. Note that the default value for this field is 25%. This test is intended only as a rough test to ensure that the sense resistor is mounted and not shorted; it is not intended to be a highly accurate test of the sense resistor value. This value must be specified as a positive integer value.

22.3.131.15 Voltage Reference/FSV This box contains two values. The tester calibrates the voltage gain my manipulating the Full Scale Voltage Reference. Do not change the values in these fields.

22.3.131.16 Temperature Maximum Offset This box contains one value. Enter the maximum amount of offset that can be put into the module being tested, either positive or negative from 0. The default value of this field is 40, meaning that the calibrated offset entered in the data flash cannot exceed positive or negative 4°C.

22.3.131.17 Starting Serial Number Enter the value for the serial number of the first bq20z80-based smart battery module to be tested. This number is incremented by one as each new module is tested. If the *Skip On Error* check box is checked, the number is not incremented in the case of a module that fails the test. The default for this box is 1. This value must be specified as a positive integer value.

22.3.131.18 Date Enter the value for the desired date to be programmed into the bq20z80-based smart battery module. If the *Use Current Date* check box is checked, the system date from the PC running the BQTester software is used.

22.3.131.19 Log File Name Enter the complete path and file name to be used for the log file. This file contains all relevant test data for each bq20z80-based smart battery module tested. If the *Clear Log* button is pressed, the log file contents are deleted

22.3.131.20 Pack Lot Code Enter the value for the Lot Code of the group of bq20z80-based smart battery modules currently being tested. This number does not change until it is changed manually and is programmed into each bq20z80-based smart battery module tested. This value must be specified as a positive integer value.

22.3.131.21 Save Clicking the *Save* button causes the current configuration settings to be saved.

Running the Test

22.3.132.22 Locking the Configuration The test cannot be started until the *Lock Configuration* button has been clicked. First, click on *Options* from the top drop-down menu. A selection called *Allow V, T, I while locked* appears. If selected, the user is able to change actual values for voltage, temperature, and current even though the configuration has been locked. If not selected, the user is unable to alter these values without unlocking the configuration. Note that the configuration must be currently unlocked to select this option. Once *Allow V, T, I while locked* has been selected or deselected, click on *Lock Configuration*. This causes a password dialog to appear. Enter a password, and record it in a safe location for future reference. Click on *OK*. Notice that the *Lock Status* icon changes from an open lock to a closed lock

22.3.132.23 Starting the Test Click on the *Start Test* button to run the test. The software displays a *Busy* indication and then indicates *Pass* or *Fail*. The software also displays information about each bq20z80-based smart battery module tested and its *Pass* or *Fail* status. This same information is also recorded in the log file. If a module fails, an error code is displayed. Appendix A defines the error codes for the BQTester software.

22.4 Software Change Recommendations

1. Edit only modCustom.bas to customize the software behavior.
2. Add new files when new functionality is added. Do not edit existing files.
3. Edit modSerial.bas to change the way serial numbers are generated.
4. Examples of how to use existing functions to read/write gas gauge constants can be found in the modGGDF.bas file. It is recommended that end users use these functions for data flash access instead of writing their own.

22.5 Revision History

Document Revision History

V1.00 June 2005

1. Original release for testing bq20z80

BQTester Software Revision History

V1.03 June 2005

1. Original release for testing bq20z80

Error Code Definitions

Gregory Grant *PMP Portable Power*

New error codes below		
VB_NO_ERROR	0	
VB_LOST_SYNC	1	
VB_NO_USB	2	Was VB_NO_RS232
VB_BAD_PEC	3	
VB_WRONG_NUM_BYTES	5	
VB_T2H_UNKNOWN	6	
VB_SMBC_LOCKED	260	Unused but reserved for backward compatibility
VB_SMBD_LOCKED	516	Unused but reserved for backward compatibility
VB_T2H_NACK	772	
VB_SMBD_LOW	1028	Unused but reserved for backward compatibility
VB_SMB_LOCKED	1284	Unused but reserved for backward compatibility
New error codes returned to VB		
VB_INCORRECT_PARAM	7	Invalid parameter type passed to function – especially Variant argument. ex. Variant containing integer instead of Variant containing array of bytes
VB_TIMEOUT_ERROR	8	USB Timeout
VB_INVALID_DATA	9	AssemblePacket could not build a valid packet
VB_ERR_UNSOLICITED_PKT	10	Found an unsolicited non-error packet when looking for error packets
VB_COMPARE_DIFFERENT	11	Comparison failed and data read is different from srec
Added codes for Programming/Compare Srec errors		
VB_BQ80XRW_OCX_INTERNAL_ERROR	12	Problems with pointers being NULL etc.
VB_SREC_OPEN_FAIL	221	
VB_SREC_BAD_START_RECORD	222	
VB_SREC_UNKNOWN_TYPE	223	
VB_SREC_BAD_CHECKSUM	224	
VB_SREC_BAD_RECORD_COUNT	225	
VB_SREC_DEV_MISMATCH	226	SREC targets a different device than the one detected on the SMBus
Config errors		
VB_CONFIG_OPEN_FAIL	227	
VB_CONFIG_UNEXPECTED_EOF	228	
VB_CONFIG_BAD_FORMAT	229	
VB_PCFG_DEVVER_MISMATCH	231	The VER byte in the devices instruction flash does not match the range expected by this config file
VB_PCFG_DEV_MISMATCH	232	The DEV byte in the devices instruction flash does not match what the config file expected
VB_PCFG_SRECDEVVER_MISMATCH	233	The VER byte in the instruction flash image to be programmed into the device does not match the one in config file
VB_PCFG_SRECDEV_MISMATCH	234	The DEV byte in the instruction flash image to be programmed into the device does not match the one in config file
VB_BCFG_DEVVER_MISMATCH	235	The VER byte in the devices instruction flash does not match the range expected by this config file
VB_BCFG_DEV_MISMATCH	236	The DEV byte in the devices instruction flash does not match what the config file expected
VB_USER_CANCELLED_OPERATION	34	
VB_DF_CHECKSUM_MISMATCH	51	
VB_IF_CHECKSUM_MISMATCH	52	

VB_OPERATION_UNSUPPORTED	53	
New Error codes corresponding to PKTSpec Error codes		
VB_ERR_TOO_MANY_QUERIES	81	
VB_ERR_BAD_QUERY_ID	82	
VB_BAD_CRC	83	
VB_ERR_TOO_MANY_RESPONSES	84	
VB_ERR_NO_QUERIES_TO_DELETE	85	
VB_ERR_QUERY_UNAVAILABLE	86	
VB_ERR_NO_RESPONSES_TO_DELETE	87	
VB_ERR_RESPONSE_UNAVAILABLE	88	
VB_ERR_TMMT_NO_RESPONSE	90	
VB_T2H_ERR_TIMEOUT	92	
VB_BUS_BUSY	94	
VB_T2H_ERR_BAD_SIZE	95	
VB_ERR_BAD_PAYLOAD_LEN	97	
VB_ERR_TMMT_LIST_FULL	98	
VB_ERR_TMMT_BAD_SELECTION	99	
VB_UNKNOWN	100	
New Generic error codes		
VB_UNEXPECTED_ERROR	110	Should not happen
VB_OUT_OF_MEMORY	111	
User defined error codes must be above 65536		
VBUSER_INVALID_FILENAME	65537	
VBUSER_DEVICE_VERSION_MISMATCH	65538	
VBUSER_RETURN_TO_ROM_FAILED	65539	
VBUSER_RUNGG_FAILED	65541	
VBUSER_WRITEFLASH_GG_FAILED	65542	
VBUSER_CALIBRATE_FAILED	65543	
VBUSER_POST_CAL_CHECKS_FAILED	65544	
VBUSER_WRITESERIAL_FAILED	65545	
VBUSER_ERR_UNEXPECTED	65552	
VBUSER_ERR_FILE	65553	Error opening/processing File
VBUSER_ERR_NOT_IN_ROM	65554	GG not in ROM mode when expected – communication failure?
VBUSER_ERR_ENTER_CALMODE	65555	Cannot put GG in Cal mode
VBUSER_ERR_CUSTOM_FUNC	65556	
VBUSER_BAD_FILE_FORMAT	65557	Header bad or format bad
VBUSER_ERR_WRITE_MFG_DATA	65558	Failed to write manufacturer data
VBUSER_CAL_VOLT_LESSTHANZERO	65600	Calibration voltage must be greater than 0
VBUSER_CAL_TEMP_LESSTHANZERO	65601	Calibration current must be greater than 0
VBUSER_CAL_CURR_LESSTHANZERO	65602	Calibration current must be greater than 0
VBUSER_WRITEFLASH_ROM_FAILED	65560	
VBUSER_SENSE_RES_CAL_HIGH	65570	
VBUSER_SENSE_RES_CAL_LOW	65571	
VBUSER_VOLT_CAL_HIGH	65580	
VBUSER_VOLT_CAL_LOW	65581	
VBUSER_TEMP_CAL_HIGH	65590	
VBUSER_TEMP_CAL_LOW	65591	

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