Application Report
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Designing the Hardware Configuration for the UCD92xx Family of Digital Power Supply Controllers

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ABSTRACT

This application report details the hardware configuration surrounding any of the UCD92xx digital power supply controllers. How to terminate and connect each pin on these devices for a typical application is discussed in detail and explained with examples. Emphasis is placed on the necessary components (mostly resistors and capacitors) and how to size them based on the system requirements for the power supply. Brief mention is given to the corresponding parameters in the Fusion Digital Power Designer (the GUI). This application report describes all the functions of the UCD9220 controller in particular, but the description applies to any other UCD92xx controller. The appendixes detail pins and functions that are unique to the UCD9240.

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1 Introduction

The UCD9220 is a 48-pin digital power supply controller. Each of its pin's functions can be divided into one of three types: digital input/output (I/O), analog input, and power. The following pin functionality and descriptions also apply to the other UCD92xx devices, although the pin naming is slightly different. Any additional functionality pertaining to the UCD9240 devices is explained in the appendixes.

2 Digital Input/Output Pins

The UCD9220 controller contains 27 digital I/O pins. Each digital pin accepts only 3.3-V logic level signals. All digital outputs are push-pull outputs, except for PMBus_CLK, PMBus_Data, and PMBus_Alert. PowerGood and any pins reconfigured as GPOs can be configured as push-pull or open-drain outputs in the GUI (graphical user interface).

2.1 PMBus™ Communication (PMBus_CLK, PMBus_Data, PMBus_Alert, PMBus_CNTL)

PMBus_CLK and PMBus_Data are the PMBus communications bus lines and are required for PMBus communications with the controller. Multiple PMBus devices can be connected to one PMBus communications bus. A 1-kΩ to 2-kΩ pullup resistor to 3.3 V is required on each of these lines. A pullup resistor on each line is needed per bus, not per device.

PMBus_Alert is a status output of the controller that is asserted (pulled low) as defined in the PMBus specification. If used in the system, a 10-kΩ to 100-kΩ pullup resistor to 3.3 V is required. It may be left floating if unused.

PMBus_CNTL is an input to the controller. It can be used to disable the output voltages that are configured to respond to the control pin in the On/Off Config definition for each rail in the GUI. If no output voltages are configured to respond to the control pin, the PMBus_CNTL input has no effect. For example, if rail 1 is set to operate on Control Pin Only or on Both Control Pin and Operation, asserting PMBus_CNTL disables rail 1. If rail 2 is set to operate on Operation Only or Always Converting, then the PMBus_CNTL pin has no effect on rail 2. This pin must always be terminated with either a pullup (to 3.3 V) or pulldown resistor between 10 kΩ and 100 kΩ. The PMBus_CNTL pin only affects the output rails and does not turn off or reset the controller.

2.2 JTAG Communication and Synchronization (TCK, TDO/Sync_Out, TDI/Sync_In, TMS, nTRST)

The UCD9220 also supports communication through a JTAG interface. Typically, this interface is only used in manufacturing and testing and so is not the default method of communication with the controller. See the UCD9220 data sheet (SLUS904) on how to enter JTAG communication mode.

Whether JTAG communication is used or not, TMS must be pulled up to 3.3 V with a 10-kΩ resistor, and nTRST must be pulled down with a 10-kΩ resistor. TCK can be left floating when unused.

When not in JTAG mode, the TDO/Sync_Out and TDI/Sync_In pins are multiplexed with a frequency synchronization functionality. TDO/Sync_Out can be used to synchronize other devices with the switching frequency of the controller. This functionality must be set and configured in the GUI. TDI/Sync_In can be used to synchronize any rail in the controller with an external frequency. This functionality must also be set and configured in the GUI. Multiple rails can be synchronized to the same input frequency on the Sync_In pin. TDI/Sync_In always requires a 10-kΩ resistor pullup to 3.3 V. TDO/Sync_Out can be left floating when unused.

2.3 Interface with the Digital Control Compatible Driver (DPWM-xx, SRE-xx, FLT-xx)

The controller regulates the output voltage through the PWM pulses generated on the DPWM signal for each phase of each output voltage rail. It is critical to route the proper DPWM signal to the proper phase of the converter and then route the proper EAPx/EANx signals back to the controller. Depending on which gate driver is used, it may be necessary to add a 10-kΩ to 100-kΩ pulldown resistor on each DPWM output to prevent that signal from floating while the controller powers up. If the driver contains 3-state detection circuitry, then this resistor must not be used, as it interferes with the 3-state detection circuits of the driver. Consult the driver's data sheet for any pulldown requirements on its DPWM input. The DPWM outputs of the controller may be buffered, but this is unnecessary for most applications. Unused DPWMs can be left floating.

The SRE outputs are designed as inputs to a digital control compatible driver and can disable the synchronous rectifier on their associated phase. When SRE is low, the synchronous rectifier is disabled. The SRE signal may be buffered, but this is unnecessary for most applications. No termination is required on the SRE pins and unused SRE pins can be left floating.

The FLT pins are almost always fault inputs directly from a digital control compatible driver, such as the CLF pin on the UCD7230 (SLUS741). See the driver's data sheet for details on what conditions assert the FLT signal for a particular driver. If desired, the user may logic OR various faults together, with external circuitry, to generate the FLT input signal. In either configuration, if FLT is high, the power stage associated with that FLT input has a fault, and the controller disables the DPWM and SRE outputs associated with that phase. Assuming that the circuitry feeding the FLT pin goes both high and low and never floats, no termination is required on the FLT pin. Unused FLT pins associated with unused/inactive phases may be left floating. However, unused FLT pins of used/active phases must either be terminated with a 10-kΩ to 100-kΩ pulldown resistor and/or be reconfigured in the GUI to be a GPIO pin (see the following Section 2.4 for information on reconfiguring pins to GPIO). The pulldown resistor prevents noise from pulling the FLT pin high and triggering a fault, whereas reconfiguring the pin forces the controller to ignore the pin if it goes high.

With the exception of the UCD921x controllers, any unused DPWM, SRE, or FLT pin can be reconfigured into a GPIO pin in the GUI. These pins then become GPIO pins and can be treated as such (i.e., they are no longer DPWM, SRE, or FLT pins). The following GPIO section explains how to terminate these pins if they are reconfigured as GPIO.

2.4 Reconfiguring Pins to GPIO (GPIO-x, PowerGood)

The UCD9220 contains two dedicated GPIO pins. In addition, any unused PowerGood, DPWM, SRE, or FLT pin on any UCD92xx controller (except for the UCD921x controllers) can be reconfigured as a GPIO pin in the GUI. Unused GPIO pins must be left in the Configure state in the GUI and can remain floating (unconnected). The one exception to this is unused FLT pins on used/active phases. These FLT pins must either be terminated or reconfigured, as explained in the previous section, and must not be left floating.

As an input, any GPIO pin can be used in sequencing. For example, one rail (not controlled by the UCD9220) may have to be in regulation before the UCD9220 can enable another rail. The power-good signal from the first rail can be fed into a GPIO pin on the UCD9220 and the UCD9220's rail can be programmed to have a dependency on the GPIO input. If a GPIO is configured as an input, pulldowns or pullups may be required to keep the pin in a known state.

As an output, any GPIO pin can be configured as a power good for any combination of rails. Alternatively, any GPIO pin can be configured to report overcurrent warnings on any combination of rails. Each GPIO pin can be configured active high or low and can be a push-pull or open-drain output. The only termination needed on a GPIO pin configured as an output is a pullup resistor if the GPIO pin is configured as open-drain.

The PowerGood pin is simply a GPIO pin that is already configured to be a push-pull, active-high output. It asserts (goes high) when all rails are in regulation. No termination is needed on PowerGood, if it is left in its default operation.

2.5 Other Digital Functions (TMUX-x, nRESET)

The TMUX pins are preconfigured pins that are designed to cycle an external analog multiplexer. To measure multiple temperature sensors or both input voltage and input current, an external multiplexer is required for the V_{in}/I_{in} pin and/or the Temperature pin. As explained in the data sheet (SLUS904), TMUX-0 is the LSB of the two TMUX signals. So, for measuring less than two temperature sensors and/or both input voltage and input current, only TMUX-0 needs to be used. TMUX-1 can be left floating. TMUX-1 must only be used when needing to measure more than two temperature sensors. Both TMUX pins are push-pull outputs and may be left floating if unused.

Holding the nRESET pin low disables the internal ARM core in the controller and shuts down all of the controller's circuitry. This is a hard reset pin that causes the controller to reboot. In the boot process, it copies its configuration settings from data flash to RAM. nRESET must be pulled up to 3.3 V with a 10-kΩ resistor to allow the controller to operate.

3 Analog Input Pins

The UCD9220 has 14 analog inputs. Ten of these are multiplexed into a 12-bit analog-to-digital converter (ADC). The other four (EAPx and EANx) are fed into two differential amplifiers, compared against the Vref DAC, and the difference fed into two dedicated 6-bit ADCs.

3.1 Current Sense Inputs (CS-xx)

Each CS pin is an analog input that accepts a voltage proportional to current for its associated power stage. The linear input range on this pin is from 0 V to 2.5 V. The voltage on each CS pin is scaled by the value in Iout Cal Gain and then offset by the value Iout Cal Offset in the GUI to transform the voltage on the pin into the output current. These gain and offset values can be different for each phase and usually are if output current calibration is done. Each phase's values can be independently calibrated to account for slight differences in components. Unused CS pins on used phases must be grounded and Iout Cal Gain, Iout Cal Offset, and Fast Over Current all be set to 0 in the GUI. CS pins on unused phases may be left floating.

Before the voltages are converted to currents (and before the ADC multiplexer), they are compared against adjustable references in fast, analog, overcurrent comparators in the controller. The exceptions to this are the UCD9220 CS-1B input and the CS-xB inputs on the UCD9240, which do not have analog comparators monitoring them. The trip point is adjustable in the GUI in the Fast Over Current box. These analog comparators can be disabled if Fast Over Current is set to 0 A. The maximum input voltage that the comparator can be set to is 2 V. Good design practice dictates that the Fast Over Current limit be ~150% the maximum steady-state value of the output current. This gives margin for component variations and noise. A design example with these settings follows.

After the CS voltages are converted to currents, they are averaged with previous values to get a smoothed current. This smoothed value is what the GUI displays as output current. This smoothed value is also compared against separate thresholds in the controller for overcurrent faults and overcurrent warnings in the Over Current, Warn, and Fault boxes in the GUI.

Because the CS pins are inputs to an ADC (through a multiplexer), they must be conditioned with an antialiasing, low-pass filter. This filter must be at 2 to 3 kHz. Also, because they feed an analog comparator that cannot be adjusted above 2 V, the level of the CS signal may need to be attenuated so that it is below 2 V at 150% of the maximum load current. The circuit in Figure 1 shows a simplified schematic of the sense resistor current sensing method using the UCD7230 and an interface to the controller's CS-xx pin. R1, R2, and C1 accomplish both the attenuation and filtering necessary and must be located close to the controller.

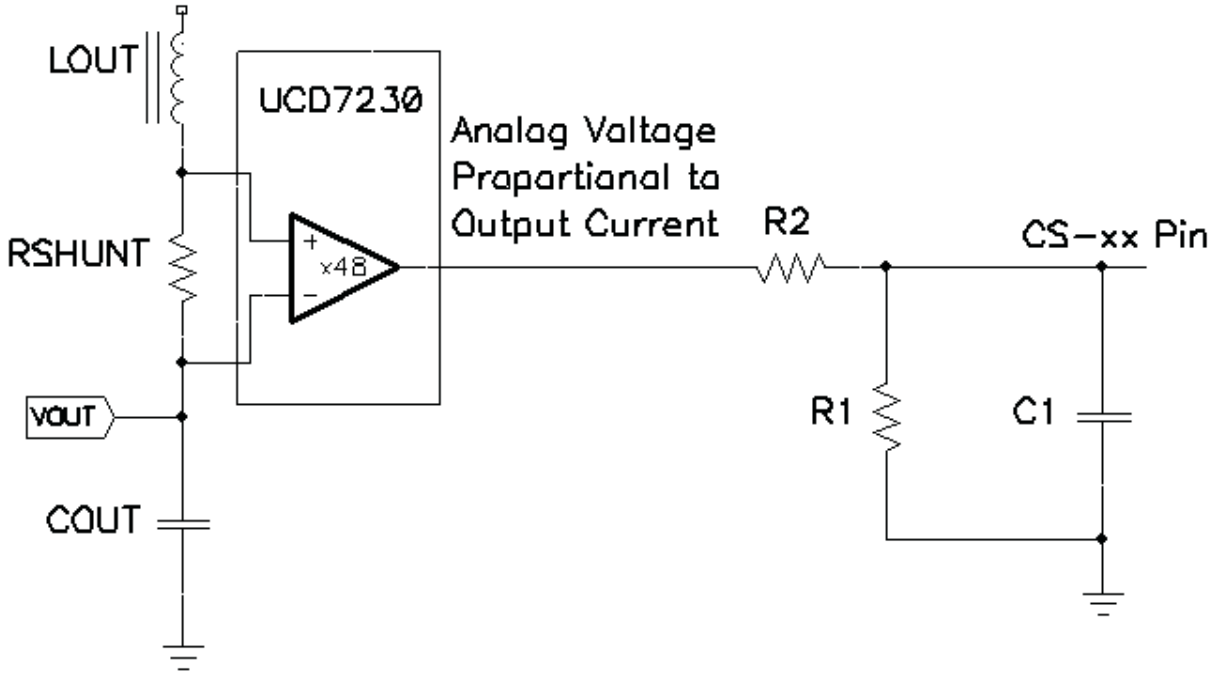

Figure 1. Simplified Schematic for Output Current Sensing With the UCD7230

To design this circuit, first determine the maximum output current of each phase and build in some margin (typically 150%) to this value. For this example, the maximum current the rail must deliver is 6 A, and 150% margin is desired. Thus, 9 A of current is used for the following calculations.

Next, calculate the ratio of the analog voltage that is proportional to the output current. This depends on the technique used for current sensing, the gain of the current sense amplifier, and any other attenuation circuitry. This value is also the value in the Iout Cal Gain box in the GUI and is represented in mΩ (mV/A). For the UCD7230 driver and the sense resistor sensing method shown in Figure 1, the Iout Cal Gain is simply the resistance of the sense resistor times 48 (the gain of the UCD7230's internal amplifier) times the attenuation created by R1 and R2. Using a 5-mΩ RSHUNT, the voltage applied to R1 and R2 at the maximum output current with margin becomes 2.16 V ($48 \times 0.005\ \Omega \times 9$ A). Thus, at 9 A of output current, the CS-xx input (without any attenuation by R1 and R2) is 2.16 V.

Next, determine if the current sensing circuit has any dc voltage offset or pedestal associated with it. This allows for reporting of negative output current when a phase is sinking current. The UCD7230 has 0.6 V of offset which must be added to the previous voltage to get 2.76-V peak voltage at the output of the amplifier.

Now, all the information necessary to choose R1, R2, and C1 is available. The 2.76-V peak voltage is greater than the 2-V maximum voltage that the analog comparator in the UCD9220 can be adjusted to. So, R1 and R2 are required to attenuate it. If the maximum amplifier output voltage is less than 2 V (as would be the case in this example with a lower RSENSE or lower gain amplifier or lower output current), R1 is not needed. However, R2 and C1 are still needed as a low-pass filter.

First, pick a value for R2. Generally, if R2 is less than 10 kΩ, this keeps the current sense circuit's impedance low and robust from noise. For this example, pick R2 = 10 kΩ. Then, R1 is selected by Equation 1:

$$R1 \le \frac{R2}{\left(\frac{V_{out\_max}}{2\,V}\right) - 1} \tag{1}$$

Thus, R1 must be no greater than 26.3 kΩ to keep the voltage on the CS-xx pin below 2 V at a 9-A output current. For this example, select R1 = 26.1 kΩ.

After selecting the sense resistor, the amplifier gain, and the attenuation resistors, the values Iout Cal Gain and Iout Cal Offset can be entered into the GUI. For this example, Iout Cal Gain is 174 mΩ (0.005 Ω × 48 × 26.1 kΩ/(26.1 Ωk + 10 kΩ)) and Iout Cal Offset is -3.45 A (0.6 V/Iout Cal Gain).

After R1 and R2 are selected, C1 finishes the low-pass filter and is selected by Equation 2:

$$C1 = \frac{1}{\left(2 \times \pi \times 2.5\ kHz \times \left[\frac{R1 \times R2}{R1 + R2}\right]\right)} \quad (2)$$

Rounding the result, set C1 equal to 10 nF. If R1 is not needed, then Equation 2 simplifies to:

$$C1 = \frac{1}{\left(2 \times \pi \times 2.5\ kHz \times R2\right)} \quad (3)$$

3.2 Input Power Sensing (V_{in}/I_{in})

The V_{in}/I_{in} pin is used to measure input voltage and input current. This pin is primarily used for only input voltage sensing, but can be used for input current sensing with the addition of an external analog multiplexer. Based on the level of the TMUX-0 pin, the multiplexer output (which is connected to the V_{in}/I_{in} pin input) is connected to either input voltage or input current. Thus, the one input to the ADC toggles between reading input voltage or input current based on the level of the TMUX-0 pin.

When TMUX-0 is low, the input voltage is read by the ADC on the V_{in}/I_{in} pin and then scaled by the gain Vin Scale in the GUI. This value is then smoothed and displayed in the GUI and compared against the Vin Over Voltage, Vin Under Voltage, Vin Off, and Vin On levels set in the GUI. Because the ADC has a full-scale input range of 2.5 V, a voltage divider on V_{in} is always required. Good design practice dictates that the divider must attenuate the maximum input voltage to 80% of 2.5 V. Furthermore, an antialiasing filter on the V_{in}/I_{in} pin with a cutoff of less than 2 to 3 kHz is also needed. Figure 2 shows the implementation of V_{in} sensing only. The value of Vin Scale in the GUI for these resistors is 0.130 (1.5 kΩ/(1.5 kΩ + 10 kΩ)).

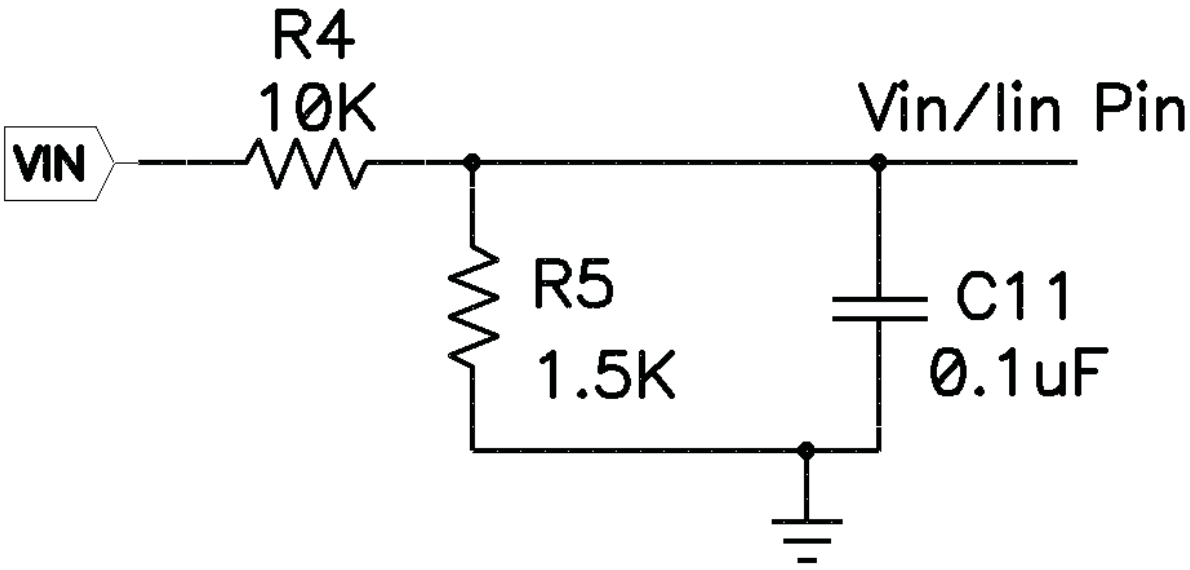

Figure 2. Input Voltage Sensing

The recommended value for R4 is 10 kΩ and for C11 is 0.1 µF. These values generally keep the antialiasing filter cutoff frequency below the required 2 to 3 kHz. R5 can be sized from Equation 4, based on a given V_{in_max}:

$$R5 = \frac{R4}{\left(\frac{Vin\_\max}{2\,V}\right) - 1} \quad (4)$$

With the values of R4 and R5 in Figure 2, V_{in_max} is roughly 15V.

When TMUX-0 is high, the input current is read by the ADC on the V_{in}/I_{in} pin and then scaled by the gain, Iin_Scale_Monitor (in Ω or V/A), set in the GUI. The value of Iin_Scale_Monitor is the total gain from the input current sense resistor to the V_{in}/I_{in} pin. The circuit in Figure 3 gives a typical input current measurement solution, whose gain is simply RSENSE × 200 (the gain of the INA210). Select the gain of the amplifier such that the maximum voltage on the V_{in}/I_{in} pin is never more than 2.5 V. Also, an antialiasing filter with a cutoff of less than 300 Hz is needed on the output of the amplifier (R6 and C7 in Figure 3). R6 is recommended to be 10 kΩ and C7 is recommended to be 0.1 µF to achieve this requirement. Figure 3 shows a simple implementation of input voltage and input current sensing.

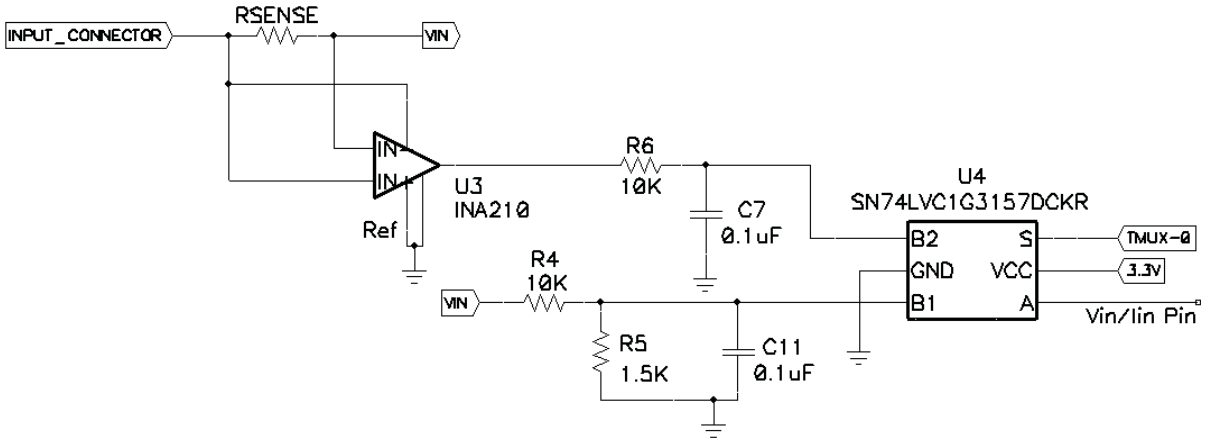

Figure 3. Input Voltage and Input Current Sensing

The input voltage sensing circuit in Figure 2 is always required, whereas the input current sensing circuit in Figure 3 is optional. Thus, the V_{in}/I_{in} pin can never be left floating. If input current sensing is not used, the analog multiplexer may be omitted.

3.3 Address Pins (ADDR-x)

The ADDR-x pins determine the PMBus address of each controller. Each controller on the same PMBus must have a different address. Other address restrictions and recommendations are explained in the data sheet (SLUS904).

The controller detects its address at power up by applying a current onto each of the ADDR-x pins. After the voltage on these pins is captured by the internal ADC, the corresponding address is stored to RAM, and the current is turned off. Thus, during normal operation, no voltage is on either of the ADDR-x pins, as the current is off. The ADDR-x resistors must be located close to the controller and tied back to the nearest ground (AGND2).

3.4 Other Analog Functions (Vtrack, Temperature, ADCref)

The Vtrack pin is used to configure one or both output rails to track (follow) another rail on start-up and shutdown. If this feature is not needed, Vtrack may be left floating. If the rail to be tracked never goes above 2.5 V (the linear input range of the ADC), then that voltage may be fed directly into the Vtrack pin, through a low-pass filter. If the rail to be followed goes above 2.5 V or if some margin is desired in the tracking circuit, implement a voltage divider on the Vtrack pin. If a voltage divider is used, the Tracking Scale value in the GUI needs to be set to the divider ratio. A low-pass filter is recommended on Vtrack to smooth the tracked voltage and provide antialiasing to the ADC. Lower cutoff frequency filters add more smoothing but can add some tracking delay. The cutoff frequency of the filter must be less than 10 kHz.

The Temperature pin is the analog input for a voltage proportional to the output temperature. The voltage on the Temperature pin is scaled by the value in “Temp Cal Gain” and adjusted by Temp Cal Offset in the GUI to generate a temperature. This calculated temperature is used in thermal shutdown, temperature balancing, and thermal compensation of the inductor DCR. If the inductor DCR method is used for output current sensing, then the value of the Thermal Coefficient in the GUI must be set to the thermal coefficient of the inductor’s windings (0.38%/°C for copper) and the temperature sensor must be placed near the inductor in order that the sensor’s temperature is a good estimate of the inductor’s temperature. This helps to achieve accurate output current readings over temperature and load. If the Temperature pin is not used, it must be left floating, and the value of Temp Cal Gain in the GUI set to zero.

Multiple temperature sensors for each phase may be connected to the Temperature pin through an external analog multiplexer. It is critical to connect the temperature sensors in the correct order, so that phase 1A is the first read (pin A0), followed by phase 1B (pin A1), etc. A simplified schematic of a circuit that uses four external temperature sensors and monitors both V_{in} and I_{in} is shown in Figure 4. A low-pass filter (not shown) is recommended on each temperature input to the multiplexer. The filter must have a cutoff frequency less than 300 Hz and so must be the same as used on input current sensing in Figure 3.

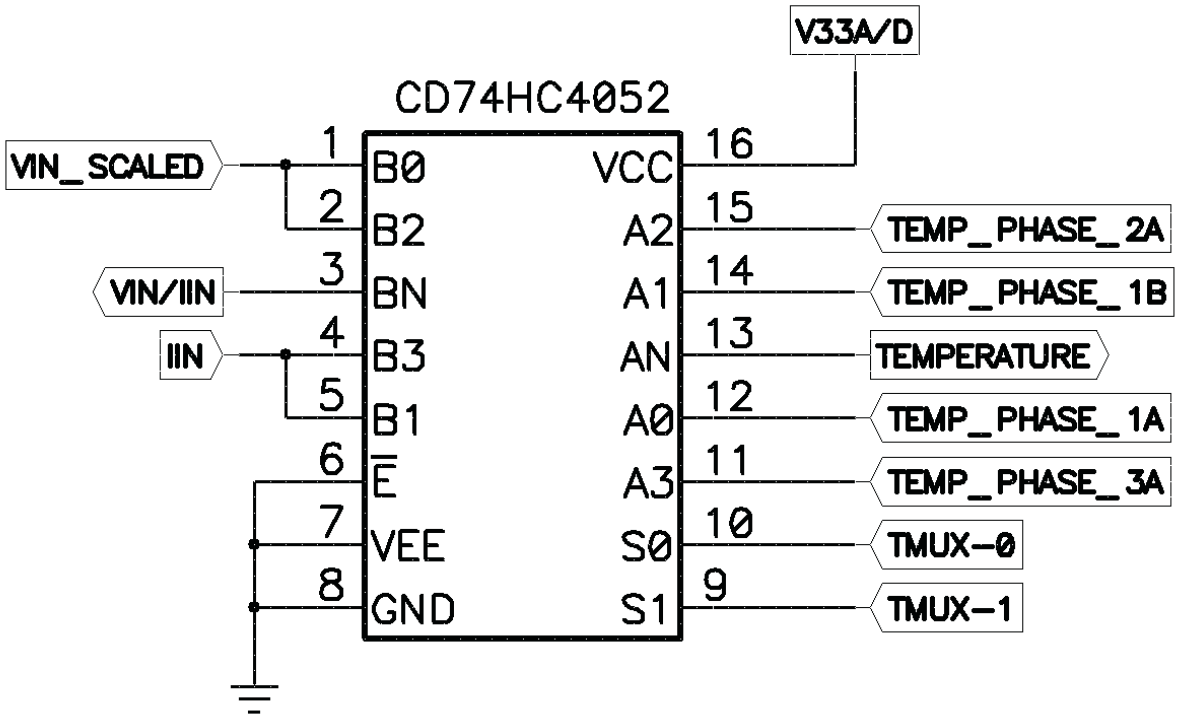

Figure 4. External Analog Multiplexer Implementation for the Temperature and V_{in}/I_{in} Pins

The ADCref pin is the reference for the ADC12 and requires a decoupling capacitor between 0.1 µF and 1 µF on it. This capacitor mut be placed right next to the controller and connect to the nearest ground (AGND2). Do not connect anything besides the capacitor to the ADCref pin.

3.5 Error Amplifier Inputs (EAPx, EANx)

The EAPx and EANx pins are differential inputs to the power supply control loop, which regulates the output voltage. Remote sensing is commonly used to take advantage of the differential input and to better regulate the output voltage. For best performance, route the output voltage traces to the EAP/N pins as a separate, shielded, noncurrent-carrying, differential pair, away from noise and make the connection to the output voltage right at the load.

The maximum steady-state voltage that can be regulated across the EAP/N inputs is 1.6 V. Thus, for any output voltage larger than 1.6 V, a voltage divider must be used. Good design practice recommends that the maximum voltage applied across the EAP/N inputs be 1.4 V to allow room for margining and calibration, which accounts for resistor tolerances. An antialiasing filter is also required at 35%-40% of the

switching frequency. Lastly, the impedance of the voltage divider must remain small to lessen the effect of bias currents into the error amplifier. Taking all this into account, the simple circuit in Figure 5 is recommended. R7 and C4 are always required, whereas R8 is only required for output voltages above 1.4 V. R7, R8, and C4 must be located close to the controller. To keep the impedance of the divider low and minimize the error due to bias currents, R8/(R8 + R7) must be between 1 kΩ and 4 kΩ.

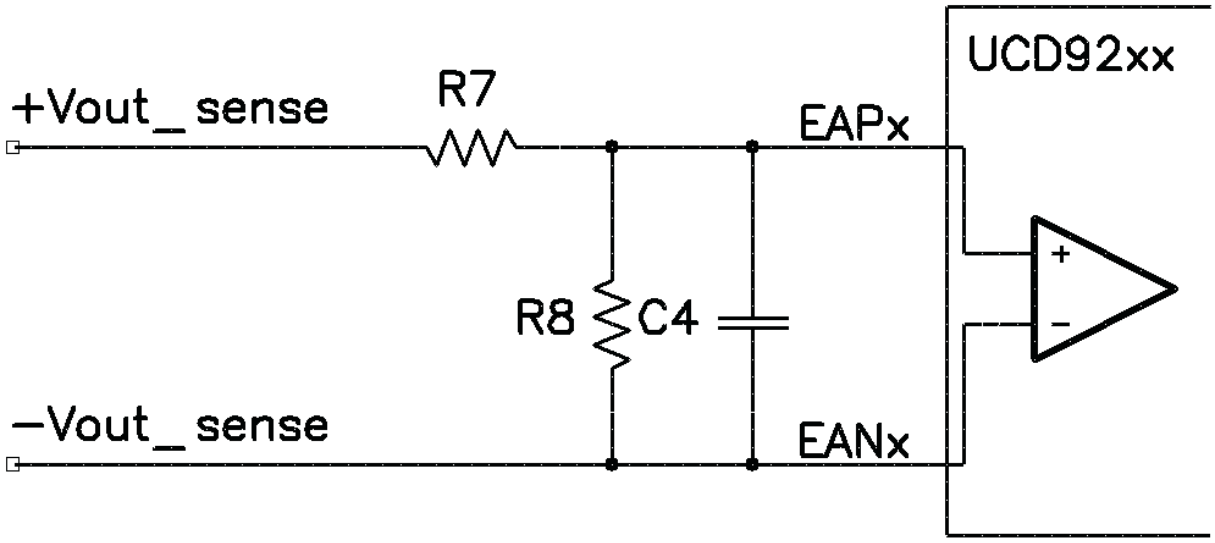

Figure 5. Error Amplifier Circuitry

As a design example, to regulate an output voltage of 2.5 V, first set R7 to 3.01 kΩ. Then, R8 is calculated from Equation 5:

$$R8 < \frac{\left(\frac{R7 \times 1.4\,V}{V_{out}}\right)}{\left(1 - \frac{1.4\,V}{V_{out}}\right)} \tag{5}$$

Thus, R8 needs to be less than 3.83 kΩ and is selected to be 3.74 kΩ. If the switching frequency is set to 500 kHz, C4 can be calculated from Equation 6:

$$C4 = \frac{1}{\left(2 \times \pi \times f_{SW} \times 0.375 \times \left[\frac{R7 \times R8}{R7 + R8}\right]\right)} \tag{6}$$

C4 is then set to 470 pF. If R8 were not needed, then Equation 6 simplifies to:

$$C4 = \frac{1}{\left(2 \times \pi \times f_{SW} \times 0.375 \times R7\right)} \tag{7}$$

Although a voltage divider is not always needed, the antialiasing filter formed by R7 and C4 is always required. Unused EAP/N pins for unused rails may be left floating.

4 Power Pins

The UCD9220 has seven power pins and a power pad under the integrated circuit (IC). Internally, the controller powers the digital and analog circuitry from separate power and ground pins.

4.1 Grounding (DGND1, AGNDx, Power Pad)

The controller has separate ground connections for the digital and analog circuitry. Both digital and analog ground must be tied together to the same net on the circuit board. The easiest and recommended place to do this is at the power pad under the IC. Good layout practice dictates that this signal ground must connect to power ground at a single point on the board. Signal ground is the low-current grounds of DGND1 and AGNDx, whereas power ground is the ground for the high-current, switching circuitry.

The power pad must be connected to a signal ground plane with vias connecting to layers directly beneath the IC. The power pad is the primary method of heat removal from the IC.

4.2 3.3-V and 1.8-V Power (V33A, V33D, BPCap)

The controller requires 3.3 V to operate. Typically, this is generated from a linear regulator, either completely external or partially internal via use of the V33FB pin. V33A and V33D can be tied to the same, low-noise, 3.3-V source and must be decoupled with a 4.7-µF ceramic capacitor and a 0.1-µF ceramic capacitor in parallel. These capacitors must be right next to the controller and connect directly to the nearest power (V33A and V33D) pins and ground pin (DGND1).

The controller generates 1.8 V from an internal regulator for some of its internal circuits. This voltage appears on BPCap and must be stabilized with a 0.1-µF to 1-µF ceramic capacitor. This capacitor must be placed right next to the controller and connect directly to the nearest ground pin (AGND1). This LDO is not designed to provide any power to other external circuitry.

4.3 3.3-V Linear Regulator (V33FB)

The V33FB pin is not to be connected to the 3.3-V supply. Rather, it is the control mechanism for building an inexpensive linear regulator to generate 3.3 V for the controller. The V33FB pin controls the drive to an external NPN transistor, which is the pass element in the linear regulator. The voltage on the base of the BJT is held constant at ~4 V. This corresponds to roughly a diode drop above the emitter voltage of 3.3 V. This transistor must be a high beta, power transistor with a thermal tab that is capable of dissipating up to 1 W, depending on the exact conditions. A resistor must be connected from the input voltage to V33FB to provide the base drive. Those two components (transistor and resistor) are all that is required to build this linear regulator and power the controller. Figure 6 shows the typical application schematic for this circuit. The V33FB pin sinks any extra current provided by R3 that does not flow into the base of the BJT. The maximum current that the V33FB pin can sink is typically 10 mA for the UCD9220.

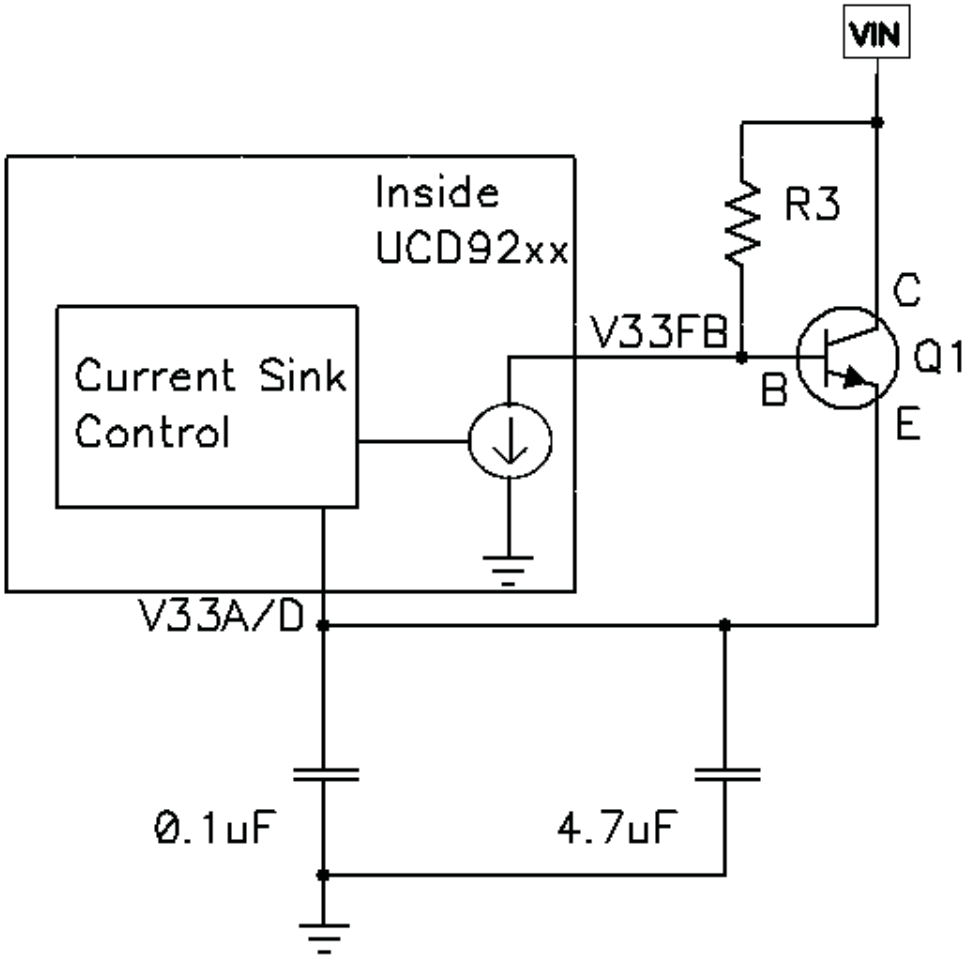

Figure 6. Linear Regulator Circuit Using the V33FB Pin

To design this circuit, Q1 must be selected first. Two things are important about this NPN transistor: rated power and beta value (β or h_{FE}). A higher beta allows R3 to be larger which results in a more efficient circuit. Also, Q1 must be able to dissipate the power lost in it, as it is the pass element in this linear regulator. This power can be calculated from Equation 8:

$$P_{diss\_Q1} = \left(V_{in\_max} - 3.3\,V\right) \times I_{UCD92xx} \tag{8}$$

$I_{UCD92xx}$ is the maximum current drawn by the controller on the V33A and V33D pins and is 80 mA for the UCD9220.

Once a transistor is selected, R3 must be sized based on the maximum input voltage. At V_{in_max}, the current through R3 is highest, because the base voltage is still held at ~4 V. At high V_{in}, the base current is also constant as the emitter current is still the same (80 mA). Thus at V_{in_max}, more current needs to be sunk by the V33FB pin. Good design practice dictates keeping the current sink required by the V33FB pin at high input voltage to half of the maximum rating for the V33FB pin—thus, 5 mA. This corresponds to a minimum value for R3. Therefore, R3 must be set by Equation 9:

$$R3 = \frac{V_{in\_max} - 4\,V}{5\,mA + \left(\frac{I_{UCD92xx}}{\beta + 1}\right)} \tag{9}$$

A maximum value of R3 corresponds to the minimum input voltage. This assumes that the V33FB pin is sinking no current and all the current through R3 flows into the base of the BJT. R3 must be below this value or else the linear regulator does not operate reliably at low input voltage:

$$R3 < \frac{V_{in\_min} - 4\,V}{\frac{I_{UCD92xx}}{\beta + 1}} \tag{10}$$

If the value of R3 from Equation 10 is less than the value of R3 from Equation 9, then a transistor with a larger beta needs to be chosen. For completion, the power lost in R3 can be calculated from Equation 11:

$$P_{diss\_R3} = \frac{\left(V_{in\_max} - 4\,V\right)^2}{R3} \tag{11}$$

For the following example, the input voltage is 12 V, but can range from 10 V to 14 V. The FMMT491A BJT has been selected as the pass transistor (Q1). From the FMMT491A data sheet typical characteristics, the β (h_{FE}) value at a collector current of 80 mA and 25°C is roughly 710.

To satisfy Equation 9, R3 must be 2 kΩ. To ensure that the chosen transistor works, check Equation 10 and find that R3 must be less than 53.3 kΩ. Because R3 (2 kΩ) is less than 53.3 kΩ, this circuit is reliable. From Equation 8, Q1 needs to dissipate 856 mW. From Equation 11, R3 must be rated for dissipating 50 mW.

Of course, this 3.3-V rail can also be used to power other circuitry on the board that needs 3.3 V. To design for this extra circuitry, simply add the current draw of the additional circuitry to the $I_{UCD92xx}$ current in the preceding equations. The preceding equations are still valid if this extra current is accounted for in the $I_{UCD92xx}$ variable.

An external LDO, such as the TPS715A33 (SBVS047), may be used to provide the needed 3.3 V instead of the above regulator. In this case, the V33FB pin may simply be left floating.

5 Conclusion

The UCD92xx family of digital power supply controllers gives the power supply designer a large degree of design flexibility and pin configurability. This application report has described the function and required hardware termination of each of the pins on the UCD9220 for the typical circuit implementations. Table 1 summarizes how to terminate each pin on the UCD9220. The appendixes describe certain pins and functions peculiar to the UCD9240.

Table 1. Summary of Required Pin Terminations on the UCD9220

Category	Pin Name	Pin Number	Termination if Used	Termination if Unused
Digital Input/Output	PMBus_Clk	10	Pullup to 3.3 V with a 1-kΩ to 2-kΩ resistor	Always used
Digital Input/Output	PMBus_Data	11	Pullup to 3.3 V with a 1-kΩ to 2-kΩ resistor	Always used
Digital Output	PMBus_Alert	19	Pullup to 3.3 V with a 10-kΩ to 100-kΩ resistor	Float
Digital Input	PMBus_CNTL	20	Ensure that the pin does not float	10-kΩ to 100-kΩ pullup or pulldown resistor
Digital Input	TCK	27	Ensure that the pin does not float	Float
Digital Output	TDO/Sync_Out	28	None required	Float
Digital Input	TDI/Sync_In	29	Pullup to 3.3 V with a 10-kΩ resistor	Pullup to 3.3 V with a 10-kΩ resistor
Digital Input	TMS	30	Pullup to 3.3 V with a 10-kΩ resistor	Pullup to 3.3 V with a 10-kΩ resistor
Digital Input	nTRST	31	Pulldown with a 10-kΩ resistor	Pulldown with a 10-kΩ resistor
Digital Output	DPWM-1A	12	None required(1)	Always used
Digital Output	DPWM-1B	13	None required(1)	Float
Digital Output	DPWM-2A	14	None required(1)	Float

(1) See Section 2.3 for a configuration where termination may be necessary.

Table 1. Summary of Required Pin Terminations on the UCD9220 (continued)

Category	Pin Name	Pin Number	Termination if Used	Termination if Unused
Digital Output	DPWM-3A	16	None required(1)	Float
Digital Output	SRE-1A	9	None required	Float
Digital Output	SRE-1B	18	None required	Float
Digital Output	SRE-2A	15	None required	Float
Digital Output	SRE-3A	17	None required	Float
Digital Input	FLT-1A	6	Ensure that the pin does not float	Pulldown with a 10-kΩ to 100-kΩ resistor and/or reconfigure to GPIO pin in GUI
Digital Input	FLT-1B	7	Ensure that the pin does not float	Float, if power stage 1B is not used
Digital Input	FLT-2A	8	Ensure that the pin does not float	Float, if power stage 2A is not used
Digital Input	FLT-3A	25	Ensure that the pin does not float	Float, if power stage 2B is not used
Digital Input/Output	GPIO-1	21	None required(2)	Float
Digital Input/Output	GPIO-2	22	None required(2)	Float
Digital Input/Output	PowerGood	26	None required(2)	Float
Digital Output	TMUX-0	23	None required	Float
Digital Output	TMUX-1	24	None required	Float
Digital Input	nRESET	5	Pullup to 3.3 V with a 10-kΩ resistor	Pullup to 3.3 V with a 10-kΩ resistor
Analog Input	CS-1A	42	Low-pass filter	Tie to ground
Analog Input	CS-1B	2	Low-pass filter	Float, if power stage 1B is not used
Analog Input	CS-2A	3	Low-pass filter	Float, if power stage 2A is not used
Analog Input	CS-3A	1	Low-pass filter	Float, if power stage 2B is not used
Analog Input	V_{in}/I_{in}	4	Connect voltage divider from V_{in}	Always used
Analog Input	ADDR-0	44	Connect resistor to ground	Always used
Analog Input	ADDR-1	43	Connect resistor to ground	Always used
Analog Input	Vtrack	45	Low-pass filter	Float
Analog Input	Temperature	46	Low-pass filter	Float
Analog Input	ADCref	48	Connect a 0.1-µF to 1-µF capacitor to ground	Always used
Analog Input	EAP1	37	Low-pass filter across EAP1 and EAN1	Always used
Analog Input	EAN1	38	Low-pass filter across EAP1 and EAN1	Always used
Analog Input	EAP2	39	Low-pass filter across EAP2 and EAN2	Float
Analog Input	EAN2	40	Low-pass filter across EAP2 and EAN2	Float
Power	DGND1	32	Connect to ground	Always used
Power	AGND1	36	Connect to ground	Always used
Power	AGND2	47	Connect to ground	Always used
Power	Power Pad	Pad	Connect to ground	Always used
Power	V33A	34	Connect to 3.3 V	Always used
Power	V33D	33	Connect to 3.3 V	Always used

(2) See Section 2.4 for full explanation.

Table 1. Summary of Required Pin Terminations on the UCD9220 (continued)

Category	Pin Name	Pin Number	Termination if Used	Termination if Unused
Power	BPCap	35	Connect a 0.1-µF to 1-µF capacitor to ground	Always used
Power	V33FB	41	See Section 4.3	Float

Appendix A UCD9240RGC – 64 Pin

The 64-pin version of the UCD9240 provides two unique capabilities beyond the additional functionality needed to regulate two extra rails. These are fan control/spare GPIO (FAN-PWM and FAN-TACH), and additional JTAG functionality (TRCK). The other pins on the UCD9240RGC can be terminated or implemented as described in the preceding discussion of the UCD9220.

A.1 Fan Control (FAN-PWM and FAN-TACH)

FAN-PWM is a push-pull digital output used to drive an external fan. The frequency of this digital output is fixed at 156 kHz, and the duty cycle is meant to produce an average voltage, once filtered. This average voltage is not regulated with a control loop, but is simply set by the host via PMBus. Typically, this output is low-pass filtered and then fed to an amplifier which drives a fan. See the UCD9240 data sheet (SLUS766) for an example circuit.

FAN-TACH is used to read back the fan speed to the controller. It is not used to regulate the FAN-PWM, but simply gathers information on the fan speed to report to the host via PMBus.

FAN-PWM and FAN-TACH also may be reconfigured as GPIOs, as in the UCD9220. Note that FAN-PWM may only be reconfigured as a general-purpose input. If the fan is not used, these two pins may be left floating.

A.2 JTAG Test Return Clock (TRCK)

The TRCK pin is a push-pull output for use in JTAG mode. It must be left floating if unused.

Appendix B UCD9240PFC – 80 Pin

The 80-pin version of the UCD9240 provides the necessary control pins to implement two additional output phases (or six additional GPIOs), as well as breaking out the JTAG pins to be completely independent and not multiplexed with other functions. It also adds an additional dedicated general-purpose input (GPI) pin (Diag LED). Leave the Aux-in pins (pins 71 and 72) floating.

B.1 GPI (Diag LED)

Diag LED may only be used as a general-purpose input. Diag LED may be left floating if not used.

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