APPENDIX A -- ERROR AMPLIFIER AND COMPENSATION NETWORK DESIGN

The error amplifier with its associated compensation network completes the closed loop system by comparing the output voltage to a voltage reference at the input of the error amplifier and feeding the inverse of the amplified error signal back to the control input. The compensation networks provide phase leads and lags at appropriate frequencies to cancel excess phase lags and leads of the power circuit. The goal is to obtain an overall loop gain characteristic approaching that of a single pole, rolling off -20 dB/decade with 90° phase lag with the gain crossing 0 dB at high frequency (appx. $f_s/4$).

Single Pole Topologies. The circuit of Figure A-1 provides essentially a flat gain characteristic with zero phase shift (not including normal 180° negative feedback). One or two poles are introduced at high frequency to compensate for power circuit zeros. Figure A-1 is intended for use with all power circuits which have single pole filter characteristic. This includes all topologies in the discontinuous inductor current mode (regardless of control method) and all continuous mode topologies when used with current mode control.

Pole #1, R_f and C_f, compensates for the zero of the output filter capacitor ESR in the power circuit.

Pole #2 compensates for the right-half-plane zero that occurs with continuous mode boost and flyback topologies. R_p should be one tenth of R_i to avoid interaction between poles 1 and 2. Pole #2 is not used (R_p and C_p are omitted) with topologies whichhave no right-half-plane zero, such as the continuous mode buck regulator and all discontinuous power circuits.

Resistor R_{ref} should be equal to the net DC resistance seen by the E/A inverting input (R_d in parallel with R_i) in order to cancel input voltage offset caused by amplifier input bias current.

Resistor R_d forms a voltage divider with R_i and R_p when the regulated output voltage, V_o, is larger then V_{ref}. R_d simply provides a DC offset. It has absolutely no effect on loop gain. This is because under normal operation, the voltage on the inverting input is a DC voltage always within a millivolt or two

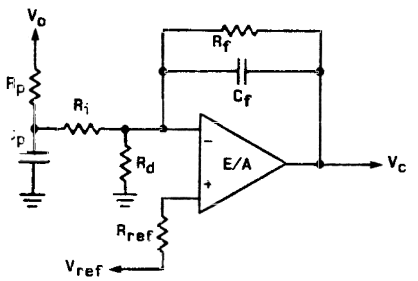
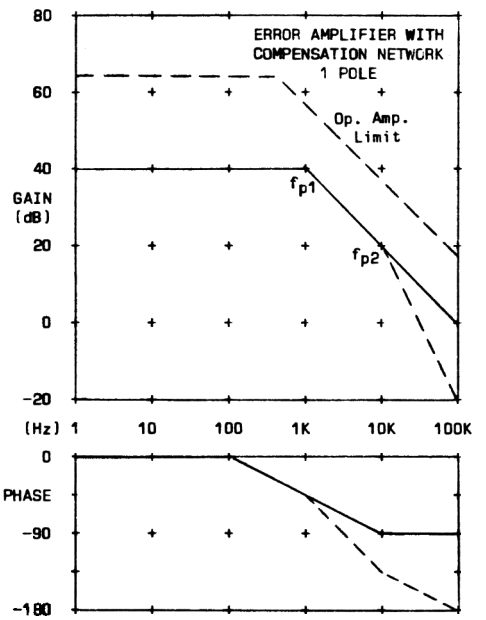


Figure A-1



$$\text{Gain (below } f_{p1}) = R_f/R_i$$

$$\omega_{p1} = \frac{1}{R_f C_f}, \qquad \omega_{p2} = \frac{1}{\Gamma \sim \backslash}, \qquad R_p \ll R_i$$

$$R_d = \frac{V_{ref}(R_i + R_p)}{V_o - V_{ref}}$$

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of V_{ref} applied to the non-inverting input. DC current flows through R_d, but no AC current. R_d sets the DC input voltage level, but does not effect the gain.

Two Pole Topologies. The circuit of Figure A-2 is intended for power circuits which have a two-pole filter characteristic — all continuous inductor current mode topologies when not using current mode control. Pole #3 is used with the flyback and boost circuits to compensate for their right-half-plane zero which would otherwise flatten out the gain curve at high frequency. Pole #3 (R_p, C_p) is omitted in buck regulator applications. Pole #2 is used in all cases to compensate the filter capacitor ESR zero.

Zero #2 is required to cancel one of the two filter poles. Unfortunately, this usually reduces the low frequency gain below the gain required to meet DC regulation requirements. Pole #1 is added to boost the low frequency gain. Zero #1 is then required to cancel Pole #1 when the filter pole frequency is reached. Zeros #1 and #2 are often placed at one-half the filter pole frequency to provide anticipatory phase shift. This is because the two pole second order resonant filter can have an extremely rapid phase shift at the pole frequency. This whole mess is avoided by using current mode control and/or discontinuous inductor current operation.

Pole #1 frequency is determined by C_f and R_f. However, in most cases R_f is omitted (open), which would predict the gain rising to infinity at $f_{p1} = 0$. In reality, the gain cannot exceed the error amplifier capability, and f_{p1} occurs where the gain curve intersects this limit at a frequency below 1 Hz.

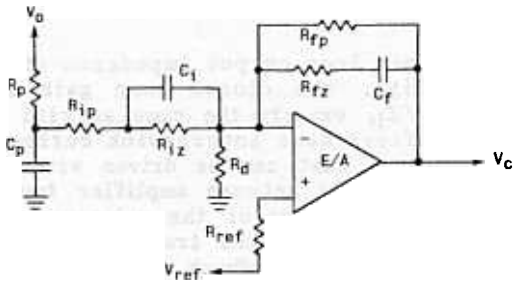
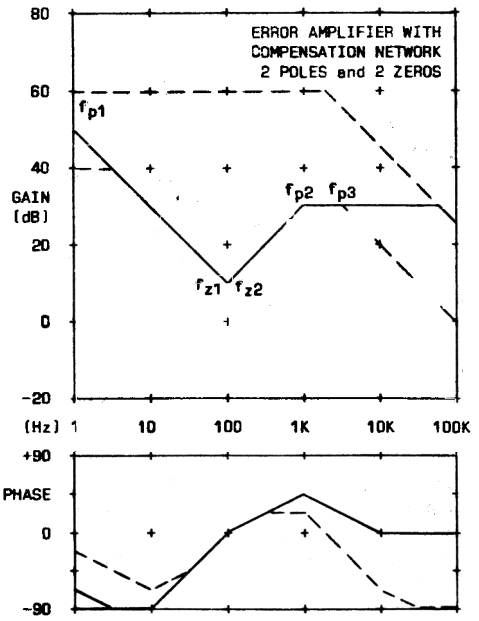


Figure A-2



Gain (at f_{z1}, f_{z2}) = R_f

$$\omega_{z1} = \frac{1}{R_{fz}C_f}, \qquad R_p \ll R_i$$

$$\omega_{z2} = \frac{1}{\Gamma \quad \sim}$$

$$\omega_{p1} = \frac{1}{(R_{fp} + R_{fz})C_f}, \qquad \omega_{p2} = \frac{R_{ip} + R_{iz}}{R_{ip}R_{iz}C_i}$$

Although well-designed compensation networks similar to Figure A-2 will provide excellent regulation and small-signal dynamic performance, the input capacitor, C_i, severely impairs large signal transient performance. This is because in all the continuous inductor current mode circuits, the inductor current cannot keep up with large step changes in load current. The rate of change of inductor current depends on the excess volt-seconds available when the duty cycle is at its max. limit. It may take up to 10 or 20 switching periods for the inductor current to follow a step change from half to full load, especially at low V_{in}. During this time, the error amplifier is driven into its bounds (max V_c), and

the closed loop is temporarily 'open'. The voltage at the inverting input is no longer held equal to V_{ref}, and C_i and C_f will charge to abnormal voltage levels. When the inductor current reaches the new value and the loop is again able to resume functioning, the error voltage on C_i causes a corresponding error in V_O. Further, the time constant for recovery, C_iR_{iz}, may be milliseconds.

The circuit of Figure A-1 does not have this problem because there is no C_i and the circuit can recover almost immediately. The only capacitors are small with relatively high frequency poles with much shorter time constants. This is a good recommendation for discontinuous mode power circuits and current mode control of continuous mode circuits which can be compensated with Figure A-1.

Minimum Load Resistance. Be careful not to use too small a value of feedback resistance, R_f, and/or other loading on the output of the error amplifier. Every amplifier (whether voltage or transconductance type) has a maximum source and sink output current capability. If the load impedance is too small, the ability to swing the output over the desired range will be restricted. For example, the UC1524A is limited to 100 μA source or sink current. An output load resistance less than 25 K will limit the output voltage swing to less than the 2.5 volts necessary to swing the duty cycle over the full range.

Gain Limits. After the desired E/A compensation network has been designed and plotted, make sure the indended error amplifier can provide the gain required at low and high frequencies. The high frequency end of the error amplifier gain characteristic is a −20 dB/decade slope crossing 0 dB at the specified unity gain-bandwidth frequency. This slope terminates at lower frequencies at the specified open loop voltage gain.

Transconductance Amplifiers. Although the open loop output impedance of a transconductance type error amplifier is high, the closed loop gain is determined by the feedback impedance ratio, Z_f/Z_i, exactly the same as with a voltage mode amplifier. Both types of amplifiers have source/sink current limits which determine the minimum load impedance that can be driven without limiting the output voltage swing. The one difference between amplifier types is: the open loop voltage gain (the feedback gain limit) of the voltage type amplifier is fixed, whereas the open loop voltage gain of the transconductance amplifier is gmR_L, and varies with output load (note the feedback resistor is an output load). Curves shown on the UC1524A data sheet illustrate this point. If the required gain runs into the gain limit, it can be raised by increasing all the impedances of the compensation network.

Slope Compensation. Recommended for all continuous mode regulators with current mode control, although not necessary for stability when duty cycle is less than 50%. Ideal slope compensation is achieved by introducing a ramp whose slope is one-half the downslope of the current ramp. It can be either a negative going ramp superimposed on the current programming voltage (the output of the error amplifier), or a positive ramp added to the current ramp. For example, a 0.2 V ramp is easily added to the current ramp by a 10:1 voltage divider in series with the input of the current amplifier, taken from the 2 Volt UC1846 oscillator ramp.

TABLE A-1	UC1524A UC1525A/27A UC1526	UC1840	UC1846
Gain-Bandwidth (MHz)	3	3	0.8
Transconductance (gm)	.002		
Open Loop Gain (30K load)	37 dB	66 dB	80 dB
Open Loop Gain (1M load)	66 dB	66 dB	>80 dB
Full Output Swing (V)	2.5	3.5	3.5
Min Load R for Full Swing	30K	15K	10K

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