TPS40422 Design Example

Vout 1: 1.2V Output, 20A max
Vout 2: 3.3V Output, 15A max
12V Input

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Design Example TPS40422 EVM PWR091

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1 Introduction

This document describes the design procedure used to generate the design of the dual-output EVM for the TPS40422, PWR091 EVM.

2 Description

The PWR091 EVM is the dual-output EVM which uses the TPS40422 controller. The TPS40422 is a two channel Synchronous Buck Controller with PMBus. It can be configured as a dual-output or two phase single output voltage mode controller. This design example is focused on the dual-output configuration. This controller combines the performance of an analog control loop with the convenience and configurability of a PMBus interface. While the control loop is purely analog, several parameters can be configured via the PMBus, and the PMBus can also be used to retrieve several operating conditions from the controller.

This dual-output design example provides the design procedure for one output of 1.2V at 20A, and a second output of 3.3V at 15A. The input voltage range is 8V to 14V.

2.1 Typical Applications

The TPS40422 is well suited for:

- Multiple Rail Systems
- Telecom Base Stations
- Switcher/Router Networking
- Server and Storage Systems

2.2 Features

This dual-output EVM features:

- Two independent outputs, 180° out-of-phase switching
- 1.2V at 20A
- 3.3V at 15A
- Input voltage range 8V to 14V
- Connector to interface with Texas Instruments Fusion Digital Power Designer GUI
- Convenient test and access points for several key signal nodes
- Low output noise
- High efficiency
- Four layer PWB with components on both sides

3 Electrical Performance Specifications, 1.2V at 20A

Table 1: **1.2V Design Electrical Parameters**

Parameter	Symbol	Notes and Conditions	Min	Nom	Max	Units
INPUT CHARACTERISTICS						
Input Voltage	Vin		8	12	14	V
Input Current	Iin	Vin = 8V, Iout = 20A	-	3.6	-	A
No Load Input Current		Vin = 12V, Iout = 0A	-	60	-	mA
Vin Start Voltage	Vin_START		-	7	-	V
Vin Stop Voltage	Vin_STOP		-	5	-	V
OUTPUT CHARACTERISTICS						
Output Voltage	Vout	Vin = 12V, Iout = 20A	1.08	1.2	1.32	V
Line Regulation		Vin = 8V to 14V, Iout = 20A	-	-	0.5	%
Load Regulation (at sense points)		Vin = 12V, Iout = 0A to 20A	-	-	0.5	%
Output Ripple Voltage	Vout_ripple	Vin = 12V, Iout = 20A	-	-	50	mVpp
Output Current	Iout	Vin = 8V to 14V	0		20	A
Output Over Current Inception Point	IOCP	Vin = 12V	21	25	29	A
Soft-Start	SS	(default)	-	2.6	-	mSec
Transient Response						
Load Step	ΔI	Iout = 10A to 5A	-	5	-	A
Load Slew Rate			-	1	-	A/µS
Overshoot			-	100	-	mV
Settling Time			-	100	-	µS
SYSTEM CHARACTERISTICS						
Switching Frequency	Fsw			300		kHz
Peak Efficiency	η_{pk}	Vin = 12V, Iout = 0A to 20A	-	90	-	%
Full Load Efficiency	η	Vin = 12V, Iout = 20A	-	85	-	%
Operating Temperature Range	Toper	Vin = 8V to 14V, Iout = 0A to 20A	-40		60	°C

4 Simplified Buck Schematic

The figure below is a simplified circuit schematic of a non-isolated Buck converter:

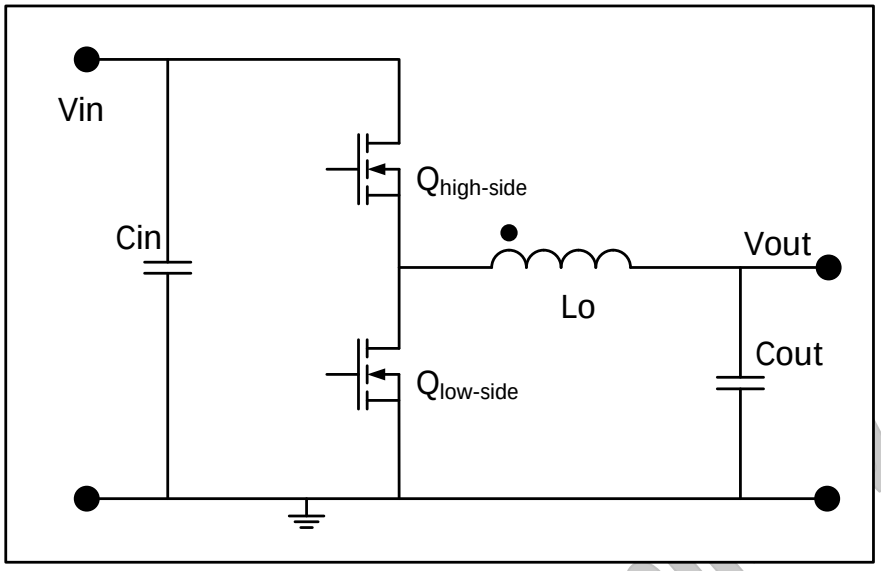


Figure 1: **Simplified Buck Schematic**

5 Design Calculations, 1.2Vout

Following are detailed design calculations of the components in the above Buck converter with the specifications in Table 1:.

5.1 Output Inductor, Lo

Several parameters affect the value selection of the output inductor. The current up-ramp and down-ramp are equal in amplitude at any steady state, and either can be used to determine the inductor value. The down-ramp is set by the output voltage and the OFF or freewheeling time, which is the time the low-side FET is ON. This time is in turn set by the switching frequency and the ratio of input to output voltage.

For typical applications, the inductor value is chosen such that its peak-peak current ramp is about 30% of the maximum load current. The highest current ramp occurs at high line, so these calculations are done at high line. This leads to:

Equation 1 Ip-p

$$Ip-p = 0.3 * 20 = 6A$$

More details:

Parameter	Note	Value
Ip-p	30% of Imax	6A
Fsw	Switching Frequency	300kHz (defined)
Period	1/(Fsw)	3.33uSec

Duty Cycle (at Vin_max)	Vout/Vin = 1.2/14	8.57%
ON time (at Vin_max)	high-side FET ON = (8.57%)*3.33uSec	285.7nSec
OFF time (at Vin_max)	low-side FET ON = (100-8.57%)*3.33uSec	3.05uSec

Equation 2 Equation Describing Inductor

$$V_L = L\frac{di}{dt} \quad \text{or:} \quad L = V_L\frac{dt}{di} \quad \text{or:} \quad di = dt\frac{V_L}{L} \quad \text{or:} \quad \frac{di}{dt} = \frac{V_L}{L}$$

Using the OFF time and the current ramp-down:

$$L = V_L\frac{dt}{di} = 1.2\frac{3.05u}{6} = 610nH$$

This defines the inductance that will yield a current ramp or ripple of no more than 6Ap-p at high line of 14V. For this design a 750nH inductor from Würth (part number 744355182) was selected. The actual ripple current should now be recalculated using the actual inductance value:

$$di = dt\frac{V_L}{L} = 3.05u\frac{1.2}{0.75u} = 4.88Ap\text{-}p$$

With this ripple current, the inductor RMS and Peak current values can be calculated. Shown below are examples of inductor current at different line voltages, all at 10A dc load current.

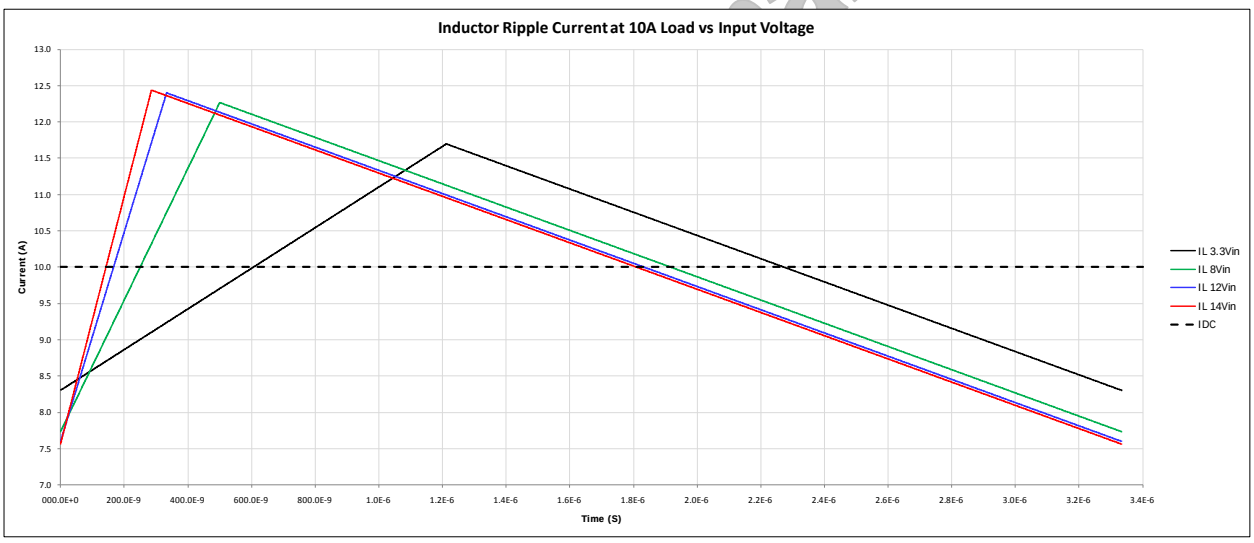


Figure 2: **Inductor Current vs Line Voltage at 10A Load**

The RMS value of a zero-average triangular wave, regardless of rise and fall symmetry, is given by:

Equation 3 RMS of Triangle

$$RMS_{Triangle} = \frac{Amplitude(p\text{-}p)}{\sqrt{12}}$$

Substituting, we get:

$$\mathrm{RMS_{Triangle}} = \frac{4.88(\mathrm{p-p})}{\sqrt{12}} = 1.409\ \mathrm{A_{RMS}}$$

Equation 4 Inductor RMS Current, I_{RMS}

$$\mathrm{I_{RMS}} = \text{Root of Sum of Squares of DC and AC Current} = \sqrt{(\mathrm{I_{DC}})^2 + (\mathrm{I_{AC}})^2}$$

At max load, this leads to:

$$\mathrm{I_{RMS}} = \sqrt{(\mathrm{I_{DC}})^2 + (\mathrm{I_{AC}})^2} = \sqrt{20^2 + \left(\frac{4.88}{\sqrt{12}}\right)^2} = \sqrt{400 + 1.9845} = 20.05\ \mathrm{A_{RMS}}$$

At max load and max line, the peak inductor current is given by:

$$\mathrm{I_{Peak}} = \mathrm{I_{DC}} + \frac{(\mathrm{I_{p-p}})}{2} = 20 + \frac{4.88}{2} = 22.44\ \mathrm{A_{Peak}}$$

The conduction losses in the inductor can be calculated with RMS current and the DC resistance (DCR) of the inductor. The DCR of the selected inductor, from the datasheet, is:

$$\mathrm{DCR} = 0.9\mathrm{m\Omega}$$

This leads to:

Equation 5 Inductor Conduction Losses

$$\mathrm{P} = \mathrm{I^2R} = (\mathrm{I_{RMS}})^2\mathrm{DCR} = 20.05^2(0.9\mathrm{m\Omega}) = 0.3618\ \text{Watts}$$

5.2 Output Capacitance, Cout

The output capacitance can be selected using different criteria. For the purposes of this design example, the capacitor will be selected based on two criteria: 1) the allowable output ripple voltage, and 2) a rule-of-thumb of a fixed amount of energy storage per watt output.

The ripple voltage developed across the output capacitor is due to the ripple current in the capacitor and the three elements within the capacitor:

1) The ripple current flowing through the resistive ESR of the capacitor.
2) The integral of the ripple current and the resulting charging and discharging of the capacitance C.
3) The derivative of the ripple current and the resulting voltage developed across the ESL of the capacitor.

Depending on the type of capacitor chosen, the majority of the output ripple will usually be due to either the ESR or the value of C. If an electrolytic capacitor is chosen, typically the resistive element (ESR) of the output noise dominates and is much larger than the capacitive charging/discharging. In order to obtain an effective ESR low enough to meet the noise specifications of the power supply, often several electrolytics must be placed in parallel, and the resulting capacitor bank will have a large value of capacitance. As such, the capacitive component of the output noise adds little to the overall ripple voltage. The inductive element (ESL) does typically produce a significant amplitude of output noise, but often this higher frequency noise is excluded from the noise performance of a power supply because most real loads have a local decoupling capacitor bank. This local decoupling, along with the

inductive and resistive parasitic elements of the copper traces between the power supply and the load, effectively attenuate this component of noise. The inductive element will not be considered here, but note that good component layout and copper routing at the switcher will always help reduce the inductive component of power supply output noise.

If instead only ceramic capacitors are chosen, typically the ESR and ESL are quite low value, and the majority of the voltage ripple results from the ripple current charging and discharging the capacitance. While ceramic capacitors offer very good ripple performance, often the value of C is relatively small and so the power supply transient response performance can suffer during very large transients such as hot plugging a capacitive load.

The approach of using a rule-of-thumb of joules of storage per watt output can be used in cases where there is a potential for hot-plugging loads. Most real electronic circuits contain decoupling capacitors within the circuitry, and when these loads are hot-plugged they present a bank of discharged capacitors. This hot-plug event results in a very rapid transfer of charge from the power supply capacitor bank to the load capacitor bank, and the transient is so rapid that the control loop cannot be designed to be fast enough to respond before a very large voltage deviation appears across the output bus. If there is not sufficient capacitance in the power supply output, the voltage bus can collapse briefly, and other electronic loads previously connected to the bus can crash as well. For systems where hot plugging of loads is expected, in general it is desirable to design to have at least 10 times the energy storage in the power supply as is expected at the hot-plugged capacitive load. While the joules per watt storage can be any number depending on the type of load environment, the number used in this example is 25uJ/Watt load. If this were a shelf converter design where entire electronic cards could be hot-plugged, this number would be much larger, in the range of 150uJ/W or 300uJ/W. Joules per watt load is related to the time constant of the output capacitor bank and the equivalent resistance of the load.

Equation 6 Energy Storage Per Watt Load

$$\mathrm{E} = (25\mathrm{uJ/Watt}) \times (1.2 \times 20) = 25\mathrm{u} \times 24 = 600\mathrm{u\ Joules}$$

$$\mathrm{E} = 600\mathrm{u\ Joules} = 0.5 \times \mathrm{C} \times (1.2)^2$$

Solving for C:

Equation 7 Minimum Capacitance Required

$$\mathrm{C_{out\,min}} = \frac{600\mathrm{u}}{0.5 \times (1.2)^2} = 833\mathrm{uF}$$

This is the minimum capacitance required at this voltage and power level, and it implies that any hot-plugged load should have no more than 83uF of bus capacitance. With a requirement of at least 883uF, it would be costly to use only ceramic capacitors. Often a parallel combination of different types and values of output capacitors yields the best overall performance, and that is the approach taken here.

Consider the following capacitors:

Part Number	Value	ESR	ESL	Quantity
T520D337M006ATE015 Kemet Polymer	330uF	15mΩ	2nH	2
Standard Ceramic	100uF	3mΩ	0.85nH	3
Standard Ceramic	22uF	2.1mΩ	0.85nH	2

The impedance versus frequency for each individual capacitor was obtained as well as the parallel combination of all 7 capacitors using Texas Instruments simulation tool TINA. These results are shown here:

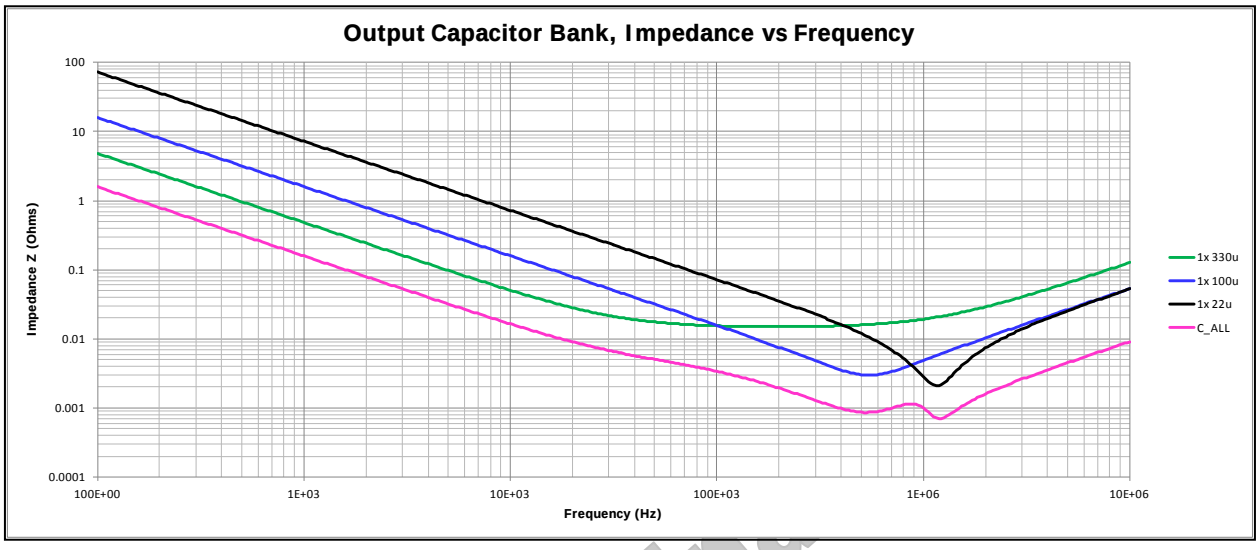


Figure 3: **Output Capacitor Bank Impedance vs Frequency**

Using the same TINA simulation tool and with the worst case ripple current previously calculated, the resulting ripple voltage for the parallel bank of output capacitors was obtained and is shown here:

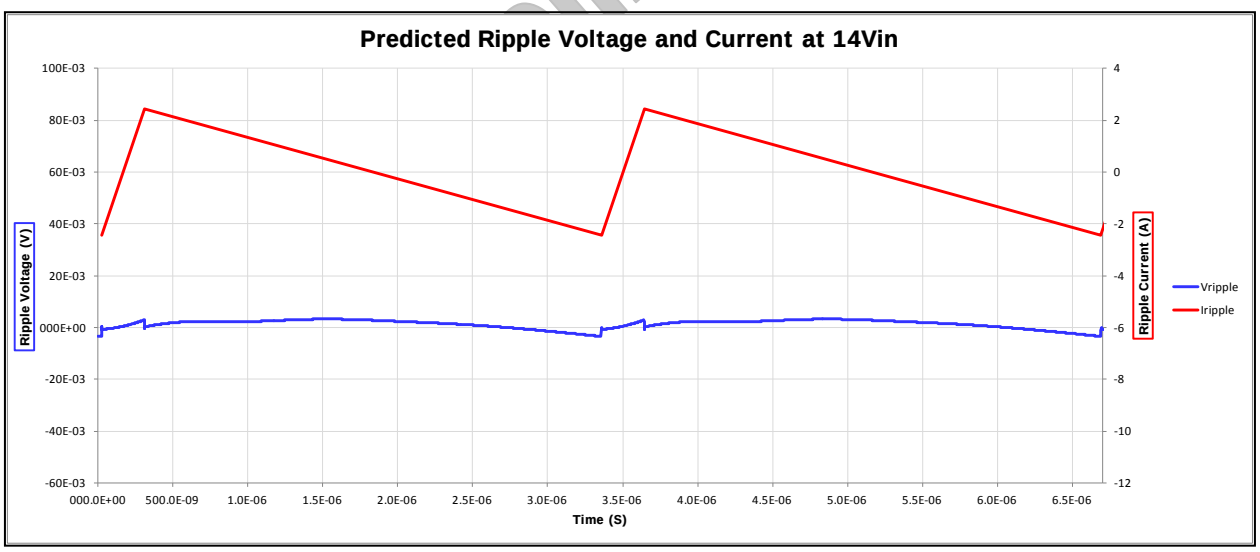


Figure 4: **Predicted Output Ripple on Capacitor Bank**

Neglecting any additional noise due to non-ideal layout, these results meet both the minimum capacitance requirements as well as the ripple voltage requirement.

5.3 Input Capacitance, Cin

The input capacitor is selected to handle the ripple current of the buck stage while maintaining the ripple voltage on the supply line low. This is especially important in cases where the supply line has relatively high impedance, which means that all or most of the AC current required by the buck stage must be supplied by the input capacitor bank. Due to the discontinuous nature of the buck input current, the high-frequency ripple current requirements on the input capacitors are often greater than those of the output capacitors.

In this design example, the design goal was to select input capacitance such that the input ripple voltage is 20% or less of Vin. The ripple voltage is due to the current flowing in the input capacitor bank and like the output capacitor ripple, this will be a combination of ESR drop as well as capacitance charging and discharging. To simplify the calculations, an infinitely large series input inductance is assumed. In reality the input inductance will be a finite value, and the result will be that the AC current in the input capacitor bank will be lower than calculated here as will be the resulting AC ripple voltage, but at the cost of an increase in the AC ripple current in the supply lines as compared to the case with an infinitely large inductor.

Consider the capacitor EEETK1E331UP from Panasonic, which is an electrolytic 330uF, 25V capacitor with 200mΩ of ESR and 100nH ESL. Calculations show that the rms value of the input capacitor bank current at full load and 14Vin has a value of 6Arms, while this capacitor only has a rating of 270mA. This implies that if this capacitor is used, there will also need to be other capacitance with a much lower ESR across the input bus so as to steer most of the AC current to this low ESR capacitor.

Another readily available capacitor was selected, and it is a 22uF ceramic, 25V, 5.5mohm ESR, 0.99nH ESL device, three in parallel. These four capacitors in parallel yield the following results:

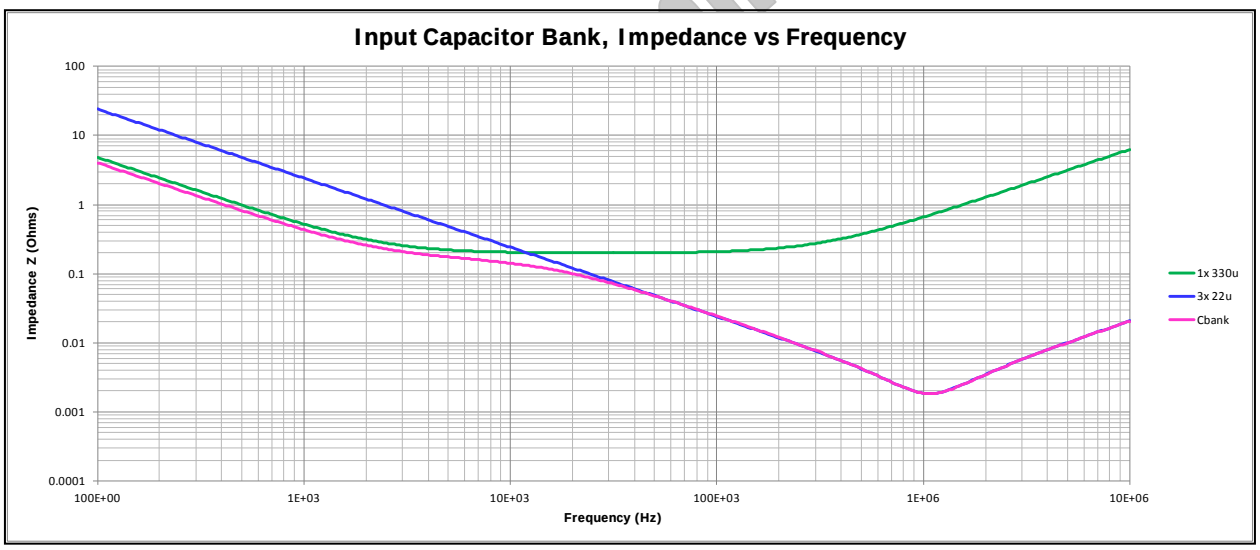


Figure 5: **Input Capacitor Bank Impedance vs Frequency**

Shown below are the resulting currents in the input electrolytic and ceramic capacitors (Iceramic and I electro), again assuming an infinitely large input inductance. Also shown is the resulting capacitor bank ripple voltage. Note that even with the large value electrolytic capacitor, the very low ESR ceramic capacitors carry the bulk of ripple current, and the resulting ripple in the electrolytic is well within its rating with a value of 146mA$_{rms}$ (calculated but not shown here).

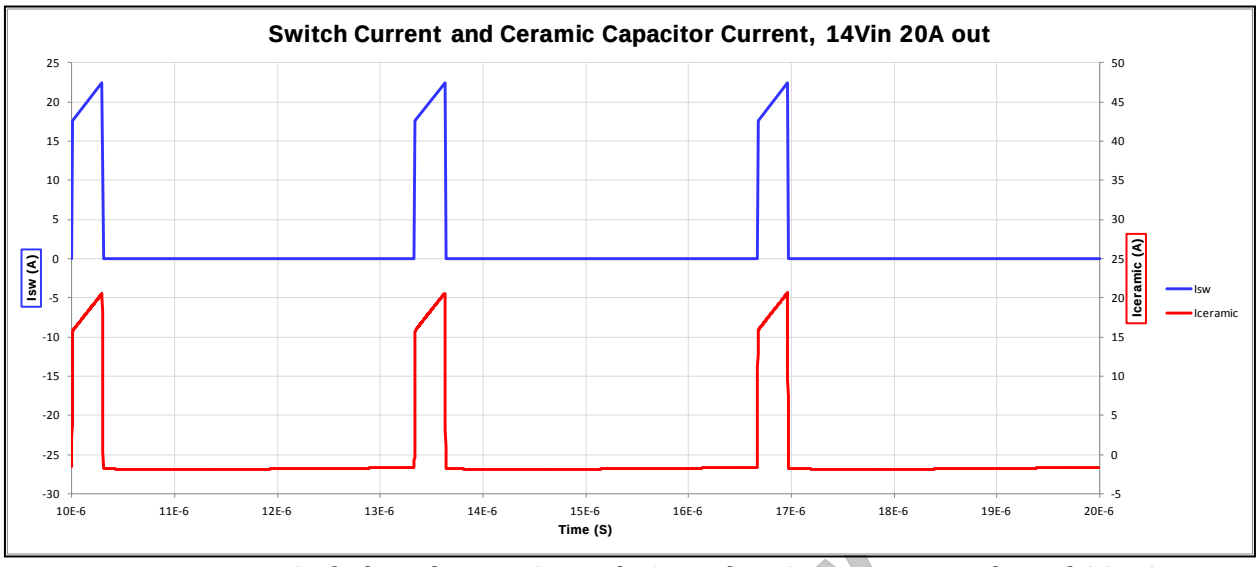


Figure 6: **Switch and Input Ceramic Capacitor Currents at 14Vin and 20A Out**

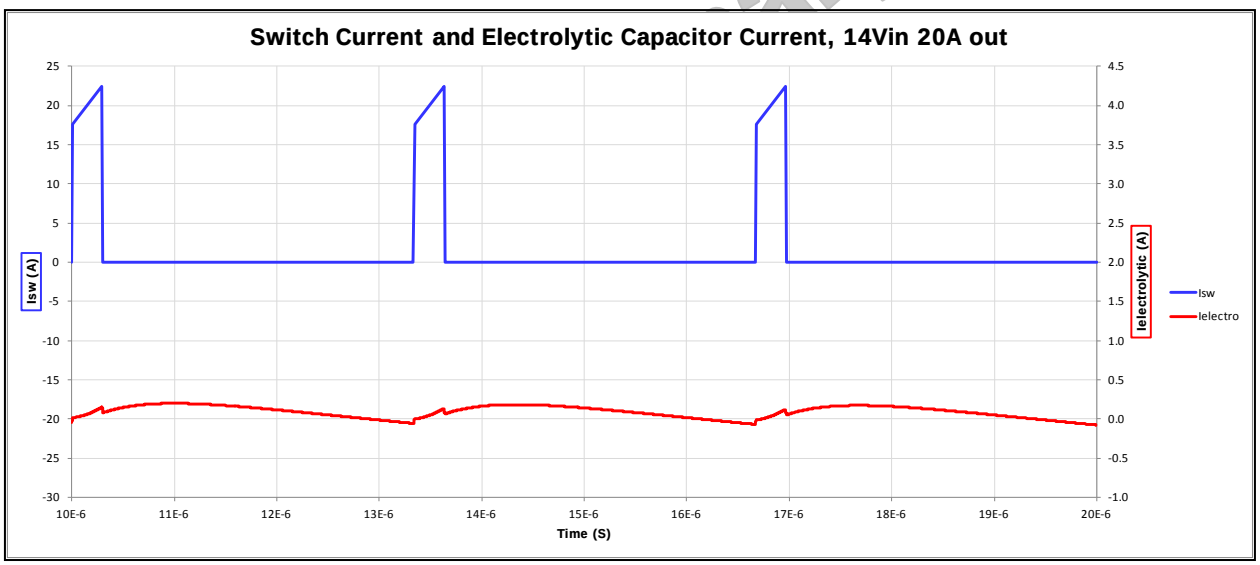


Figure 7: **Switch and Input Electrolytic Capacitor Currents at 14Vin and 20A Out**

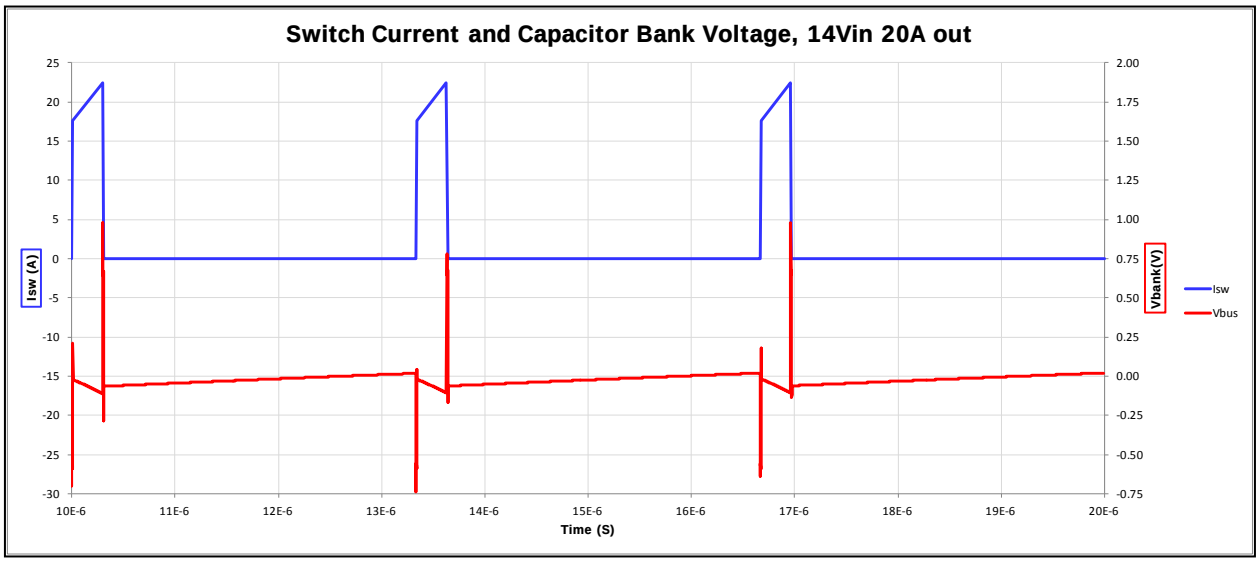


Figure 8: **Switch Current and Input Bus Voltage at 14Vin and 20A Out**

5.4 Switching MOSFETs, Q_{HS} and Q_{LS}

The following key parameters need to be met when selecting the FETs for the buck stage.

- Vds – The drain to source voltage rating must be able to handle the maximum input voltage plus inductive spikes. This design requires a 30V device.
- Vgs – The gate to source voltage rating must be able to handle the gate drive voltage. For the TPS40422 this voltage is 6.5V.
- Power dissipation – The Rdson of the MOSFET must be low enough to minimize the power loss due to conduction currents
- Gate Charge – The MOSFET's gate charge should be low enough for the PWM controller to easily drive the MOSFET. This will minimize switching and body diode losses.

The FETs were selected based on voltage rating and R_{DS_ON}. These devices are:

Location	Part #	Vrating	$R_{DS\ ON}$	Q_G
High-side	CSD87350Q5D (1/2)	30V	5mΩ	8.4nC
Low-side	CSD87350Q5D (1/2)	30V	1.2mΩ	20nC

From the datasheet, the body diode forward voltage and recovery data is:

Part #	Diode Vf	Recovery Charge Qrr	Recovery Time trr
CSD87350Q5D	0.77V	32nC	28nS

The losses in these FETs are the sum of conduction losses and switching losses:

Equation 8 FET Losses

$$P_{FET} = P_{conduction} + P_{switching}$$

Breaking this down further we get:

$$P_{conduction} = \left(I_{RMS}{}^2 \times R_{DS\_ON}\right) + \left(P_{body\ diode\ conduction}\right)$$

$$P_{switching} = P_{channel\ turn\ ON} + P_{channel\ turn\ OFF} + P_{Coss\ charge} + P_{Coss\ discharge} + P_{gate} + P_{BD\ Reverse\ Recovery}$$

Where:

Term	Description
I_{RMS}	RMS current in FET
R_{DS_ON}	resistance of FET when fully enhanced
$P_{body\ diode\ conduction}$	losses in FET body diode when FET is OFF and conducting source-to-drain current (V*I)
$P_{channel\ turn\ ON}$	resistive losses in the channel as FET turns ON (∫I*V)
$P_{channel\ turn\ OFF}$	resistive losses in the channel as FET turns OFF (∫I*V)
$P_{Coss\ charge}$	losses in the channel as it charges complement FET's Coss (½CV^2)
$P_{Coss\ discharge}$	losses in the channel as it discharges its own Coss (½CV^2)
P_{gate}	losses in the drive circuit as it drives the FET gate capacitance (½CV^2)
$P_{BD\ Reverse\ Recovery}$	reverse recovery losses in body diode of low-side FET (QVF)

The low-side switch will not have any switching losses related to ∫I*V because it will always experience ZVS during turn ON, and will experience ZVS during turn OFF at loads higher than $\frac{(I_{p-p\ ripple})}{2}$, and so it will not be included here. Normally the terms ($P_{channel\ turn\ ON}$) and ($P_{channel\ turn\ OFF}$) are significant and need to be calculated for the high-side switch. However, since this design will be using Texas Instruments NexFETs which have extremely low gate-to-drain charge Q_{GD} and therefore very rapid switching times, the switching loss terms in the high-side FET related to the integral ∫I*V will be neglected. So the switching losses will be limited to the four remaining terms:

$$P_{switching} = P_{Coss\ charge} + P_{Coss\ discharge} + P_{gate} + P_{BD\ Reverse\ Recovery}$$

First, the RMS current in the high-side FET can be calculated by:

Equation 9 High-Side FET RMS Current

$$I_{HS\_rms} = \sqrt{\left(\frac{Vout}{Vin}\right) \times \left(Iout^2 + \left(\frac{Iripple}{\sqrt{12}}\right)^2\right)}$$

Substituting at high line of 14V and full load:

$$I_{HS\_rms} = \sqrt{\left(\frac{Vout}{Vin}\right) \times \left(Iout^2 + \left(\frac{Iripple}{\sqrt{12}}\right)^2\right)} = \sqrt{\left(\frac{1.2}{14}\right) \times \left(20^2 + \left(\frac{4.88}{\sqrt{12}}\right)^2\right)} = 5.87\ A_{RMS}$$

and similarly for the low-side FET:

Equation 10 Low-Side FET RMS Current

$$I_{LS\_rms} = \sqrt{\left(\frac{Vin - Vout}{Vin}\right) \times \left(Iout^2 + \left(\frac{Iripple}{\sqrt{12}}\right)^2\right)} = \sqrt{\left(\frac{14 - 1.2}{14}\right) \times \left(20^2 + \left(\frac{4.88}{\sqrt{12}}\right)^2\right)} = 19.17\ A_{RMS}$$

There are 2 sections of dead-time per cycle, which leads to:

$$P_{\text{body diode conduction}} = 2 \times I_{DC} \times 0.77 \times 25\text{nSec} \times 300\text{kHz} = 231\text{mW}$$

The reverse recovery losses in the low-side FET body diode occur once per period, and are due to the rapid snap-off of the diodes as they transition from forward conduction to reverse blocking. The losses incurred during this recovery can be obtained by:

$$P_{\text{BD Reverse Recovery}} = \frac{1}{2} CV^2F$$

The implied capacitance is quite non-linear, so it is more accurate to use the Reverse Recovery charge Qrr, which is usually specified. Combining:

$$P_{\text{BD Reverse Recovery}} = \frac{1}{2} CV^2F \quad \text{and} \quad Q = VC \quad \text{or} \quad C = \frac{Q}{V}$$

we get:

$$P_{\text{BD Reverse Recovery}} = \frac{1}{2}\frac{Q}{V}V^2F = \frac{1}{2}QVF = \frac{1}{2} \times 32\text{n} \times 14 \times 300\text{kHz} = 67.2\text{mW}$$

The R_{DS_ON} losses in the FETs can be calculated:

$$P_{\text{HS conduction}} = {I_{RMS}}^2 \times R_{DS\_ON} = (5.87)^2 \times 5\text{m} = 172.3\text{mW}$$

$$P_{\text{LS conduction}} = {I_{RMS}}^2 \times R_{DS\_ON} = (19.17)^2 \times 1.2\text{m} = 441\text{mW}$$

The energy required to drive the gate is related to the gate capacitance, the voltage to which it is charged, and how frequently it is charged. This energy is defined by:

Equation 11 Gate Energy

$$E_{\text{gate}} = \frac{1}{2} CV^2 \times \text{Frequency}$$

Note that:
- the energy required to charge a capacitor through a resistor is double the resulting stored energy
- it does not require any drive energy to discharge the same gate capacitance (other than a small amount of energy to supply the associated logic, which will be ignored)
- in a non-isolated Buck, there is only one such charging event per period per FET
- usually the gate C is non-linear, and it is more accurate to use the gate charge

$$Q = C \times V \quad \text{or} \quad C = \frac{Q}{V}$$

Substituting:

$$E_{\text{gate}} = 2 \times \frac{1}{2} \times \frac{Q}{V} V^2 \times \text{Frequency} = QVF$$

For the high-side FET, this becomes:

$$E_{gate} = \frac{2}{2} \times \frac{Q}{V} V^2 \times \text{Frequency} = (8.4E-9) \times 6.5 \times 300000 = 16.4\text{mW}$$

For the low-side FET, this becomes:

$$E_{gate} = \frac{2}{2} \times \frac{Q}{V} V^2 \times \text{Frequency} = (7.9E-9) \times 6.5 \times 300000 = 15.4\text{mW}$$

In the equation above, the charge that was used is the sum of the Q_{GS} and the Q_{GD} (3.6n+4.3n) but not the Q_{OSS} since the Q_{OSS} will be charged and discharged by the ZVS transitions and not by the gate drive circuitry that is incurring these implied losses.

In order to calculate the terms $P_{Coss\ charge}$ and $P_{Coss\ discharge}$, it must be noted that during the transition from high-to-low on the switch node, the high-side FET Coss will obtain its charge from, and the low-side FET Coss will deliver its charge to the load through the output choke. So even though it requires twice the resulting stored energy to charge a capacitor through a resistor, the stored capacitive energy is not lost in this case, but rather used. This negates the doubling in the calculation of energy to charge the Coss capacitors during this transition. This transition is the charging of the high-side Coss and the discharging of the low-side Coss. So the energy loss occurs only during the low-to-high transition of the switch node, which is the discharging of the high-side Coss and the charging of the low-side Coss.

Equation 12 Coss Losses

$$E_{HS\_Coss} = \frac{1}{2} \times \frac{Q}{V} V^2 \times \text{Frequency} = \frac{9.7\text{n} \times 14 \times 300000}{2} = 20.37\text{mW}$$

and

$$E_{LS\_Coss} = \frac{1}{2} \times \frac{Q}{V} V^2 \times \text{Frequency} = \frac{28\text{n} \times 14 \times 300000}{2} = 58.8\text{mW}$$

Now the total losses in the FETs are:

$$P_{HS\ Total} = P_{conduction} + P_{HS\ Coss\ discharge} + P_{LS\ Coss\ charge} + P_{gate} = 172.3\text{m} + 20.37\text{m} + 58.8\text{m} + 16.4\text{m} = 267.87\text{mW}$$

$$P_{LS\ Total} = P_{conduction} + P_{body\ diode\ conduction} + P_{gate} + P_{BD\ Reverse\ Recovery} = 441\text{m} + 231\text{m} + 15.4\text{m} + 67.2\text{m} = 754.6\text{mW}$$

It must be noted that the gate losses (P_{gate}) were included here in the FET losses, but they are actually losses incurred by the drive circuitry in the TPS40422.

5.5 Component Selection

Refer to the schematic below for device reference designators and connections.

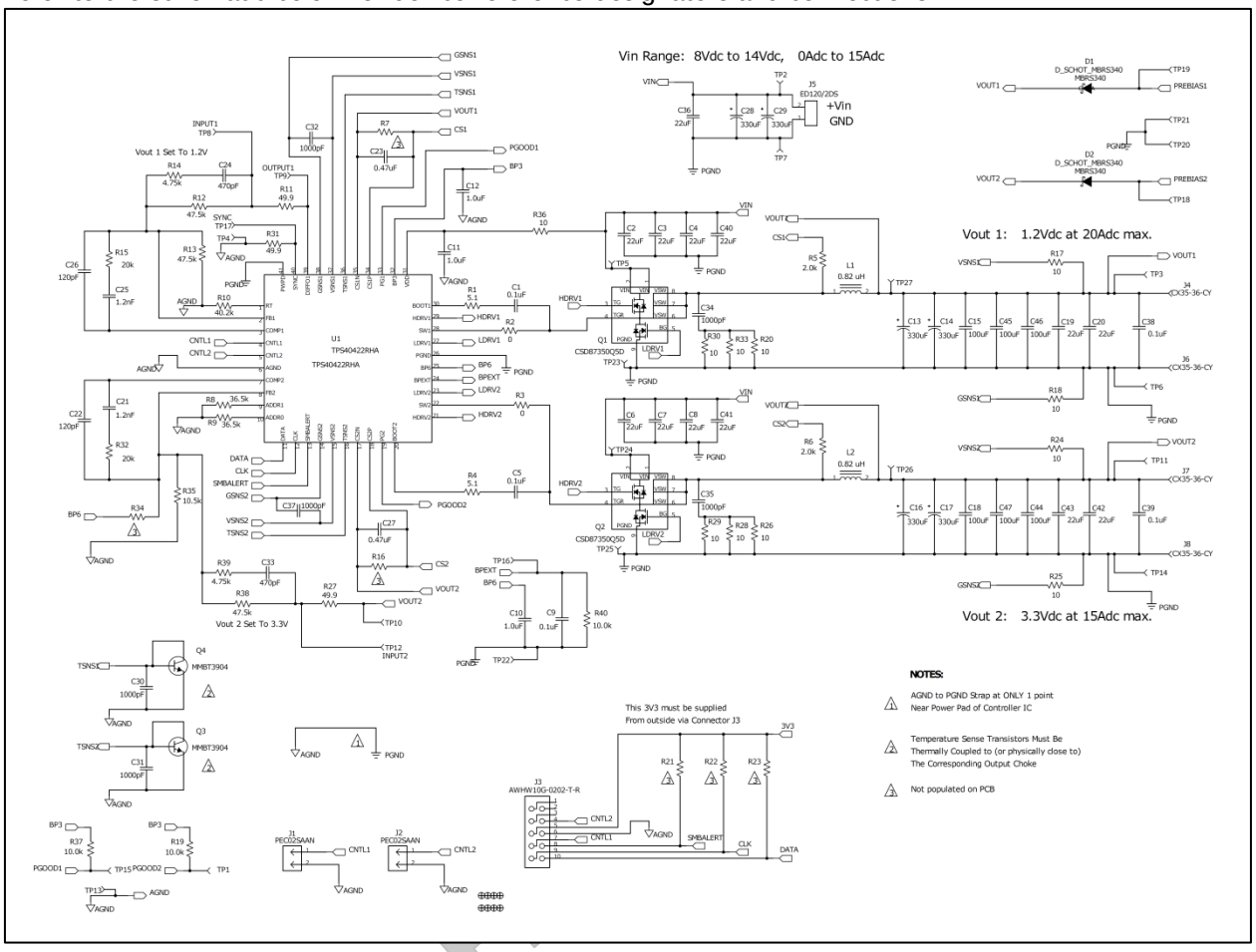


Figure 9: **Schematic**

5.5.1 Device Addressing, R_{ADDR0} and R_{ADDR1}

The PMBus address for the device must be read from the ADDR0 and ADDR1 pins. Each pin has an internal pull-up current source from BP3 and is connected to one of the inputs to the ADC. The external resistors R_{ADDR0} and R_{ADDR1} from the address pins to ground set 8 possible states which are distinguishable on each pin for a total of 64 possible addresses. The address states are determined by voltages on the address pins per Table 2:.

Table 2: **Address Configuration**

Digit	Resistance (kΩ)
0	10
1	15.4
2	23.7
3	36.5

Digit	Resistance (kΩ)
4	54.9
5	84.5
6	130
7	200

For this design, the address of 33 octal, or 27 decimal will be selected arbitrarily. In order to achieve this address, the ADDR0 resistor R5 would be 36.5k and the ADDR1 resistor R4 would be 36.5k.

5.5.2 Current Sense Filter, R5 and C23

Current sensing for the TPS40422 is typically done by sensing the voltage drop across the output inductor's DC resistance. In order to do this, the large AC switching voltage forced across L1 must be filtered out so that the measured voltage is only the DC drop. This is done by placing an R-C filter directly across the output choke L1. The R-C combination is chosen such that it provides enough filtering for the application, but for the TPS40422 the resistance value must not exceed 2kΩ in order to keep the error from the ISNS bias current to a minimum. So in order to limit the error introduced by the value of Rsense (R5), its value must be no more than 2kΩ.

For the filter capacitor, a design goal for the R-C time constant is to have it match the time constant of the output choke L1 and its DCR, which is given by: $\tau = \frac{L1}{DCR}$. So we get:

Line	Parameter	Result
1	L1	$= 750\text{nH}$
2	DCR_{L1}	$= 0.9\text{m}\Omega$
3	R5	$= 2\text{k}\Omega$
4	C23	$= \frac{L1}{DCR} \times \frac{1}{R} = \frac{750\text{n}}{0.9\text{m} \times 2\text{k}} = 416.7\text{nF. Choose } 470\text{nF}$

The capacitor C23 should be placed as close to the ISNS+ and ISNS- pins as possible to provide good bypass filtering. R5 should be placed close to the inductor to prevent traces with the switch node voltage from being propagated across the PWB and getting close to sensitive pins of the TPS40422.

5.5.3 Voltage Decoupling Capacitors, C_{BP3}, C_{BP6}, and C_{VDD}

Three pins on the TPS40422 have DC bias voltages. It is necessary to add small decoupling capacitors to these pins. Below are the recommended minimum values:

Device Location	Recommended Minimum Value	Function	Selected Value
C_{BP3}, C12	0.1uF low ESR	Bypass cap for the internal regulator that supplies power to the internal controls of the device.	1uF ceramic
C_{BP6}, C10	1uF low ESR	Bypass pin for the internal regulator that supplies power to the gate drivers.	1uF ceramic
C_{VDD}, C11	0.1uF low ESR	Bypass cap for input power to the device.	1uF, with additional series 10Ω filter resistor R36 to filter out switching noise from the power FETs.
C_{BPEXT}, C9	0.1uF low ESR	Bypass cap for the external voltage source to be used instead of BP6 if desired. **	0. 1uF ceramic, and a 10kΩ resistor in parallel.

**Note: It is also recommended to use a resistor in parallel with C_{BPEXT} when BPEXT is not being used, to avoid this voltage floating towards the turn ON threshold for BPEXT. A resistor of no more than 10kΩ should be used.

5.5.4 Bootstrap Capacitor, C1

Selection of the bootstrap capacitor is based on the total gate charge of the high-side FET and the allowable ripple on the BOOT pin. A ripple of 0.2 V is chosen as maximum for this design. Using these two parameters the minimum value for C_{BOOT} can be calculated:

Equation 13 C_{BOOT}

$$C_{BOOT}, C1 \geq \frac{Q_{G\ HS}}{V_{BOOT\ Ripple}} = \frac{8.4n}{0.2} = 42nF, \qquad \text{Choose a standard value of } 100nF$$

Additionally, a series resistor R1 is added for the purpose of slightly reducing the turn-ON speed of the high-side FET Q1. This resistor has only limited effect because at the beginning of the HDRV gate pulse when the absolute value of gate voltage is still less than BP6, most of the gate current will come directly from BP6 instead of the BOOT cap.

5.5.5 Snubber R20/R33/R40 and C34

The purpose of this snubber network is to damp the high frequency ringing on the switch node, and in doing so also reduce the peak voltage stress on the low-side FET. The amount and amplitude of ringing depends on several parameters, some of which are parasitic components and not necessarily well defined. It is possible to attempt to include all discrete and parasitic parameters in a calculation of snubber values, but experience shows that a simpler method is quick and well suited to a first iteration of snubber values. This method consists of designing the snubber based on an allowable power budget to be dissipated in the snubber. Once these values are determined and real hardware is obtained, the snubber values can be adjusted to further optimize results, but often this approach will yield a good first iteration.

This design is a 1.2V 24Watt power converter. If we were to design a snubber that dissipated 2.4 watts, the result would likely be very well behaved switch node waveforms with little ringing and overshoot, but at an unacceptable cost of 10% in efficiency. Instead, we will use a rule-of-thumb of a target power dissipation in the output snubber of between 0.25% and 0.5% (of Pout).

Normally the RC time constant is designed to be short enough such that the capacitor is fully charged or discharged before the next switching edge. This implies that the power dissipation in the snubber resistor is determined only by the capacitor value and independent of resistor value. While it may seem contradictory, we will assume an ideal switch node waveform, so that the highest voltage to which the capacitor gets charged is Vin max, in this case 14V. This, along with the target dissipation will determine the capacitor value.

The remaining snubber component, the resistor, will be determined such that the RC time constant (actually 5RC) is set to 10% of the shortest pulse width. The shortest pulse width will occur also at Vin max of 14V. Putting all this together, we get:

Parameter	Description	Result
Vmax	Max capacitor voltage	$\mathrm{Vmax} = 14\mathrm{V}$
Tpulse	Shortest Pulse Width	$\mathrm{T} = \frac{1.2}{14} \times \frac{1}{300\mathrm{kHz}} = 286\mathrm{nSec}$
Psnubber	Power Budget for Snubber	$\mathrm{P} = \mathrm{Pout} \times \frac{0.25}{100} = \frac{24 \times 0.25}{100} = 60\mathrm{mW}$
E/edge	Energy in cap for each switching edge	$\frac{\mathrm{E}}{\mathrm{edge}} = \frac{1}{2}\mathrm{CV}^2$
E/cycle	Energy in cap for each switching cycle	$\frac{\mathrm{E}}{\mathrm{cycle}} = \frac{2\mathrm{E}}{\mathrm{edge}} = \mathrm{CV}^2$
E/second	Energy in cap each second, or Joules/sec, or Watts	$\frac{\mathrm{E}}{\mathrm{Sec}} = \frac{\mathrm{E}}{\mathrm{cycle}} \times \mathrm{Fsw} = \mathrm{CV}^2 \times 300\mathrm{kHz}$
$C_{Snubber}$	Snubber cap value	$\mathrm{C} = \frac{60\mathrm{mW}}{\mathrm{V}^2 \times 300\mathrm{kHz}} = \frac{60\mathrm{mW}}{196 \times 300\mathrm{kHz}} = 1.02\mathrm{nF}$
5RC	5 Snubber Time Constants	$5\mathrm{RC} = \frac{286\mathrm{nSec}}{10} = 28.6\mathrm{nSec}$
$R_{Snubber}$	Snubber resistor value	$\mathrm{R} < \frac{28.6\mathrm{n}}{5\mathrm{C}} = \frac{28.6\mathrm{n}}{5 \times 1\mathrm{n}} = 5.72\Omega$

The above yields a good first iteration for the snubber components. For reasons of form factor and availability of components, three 10Ω resistors were chosen in parallel. See figure below for details on the associated waveforms. Shown are calculated results with three different R values but with the same 1nF snubber cap. The waveforms shown are the switch node and the voltage across the resistor.

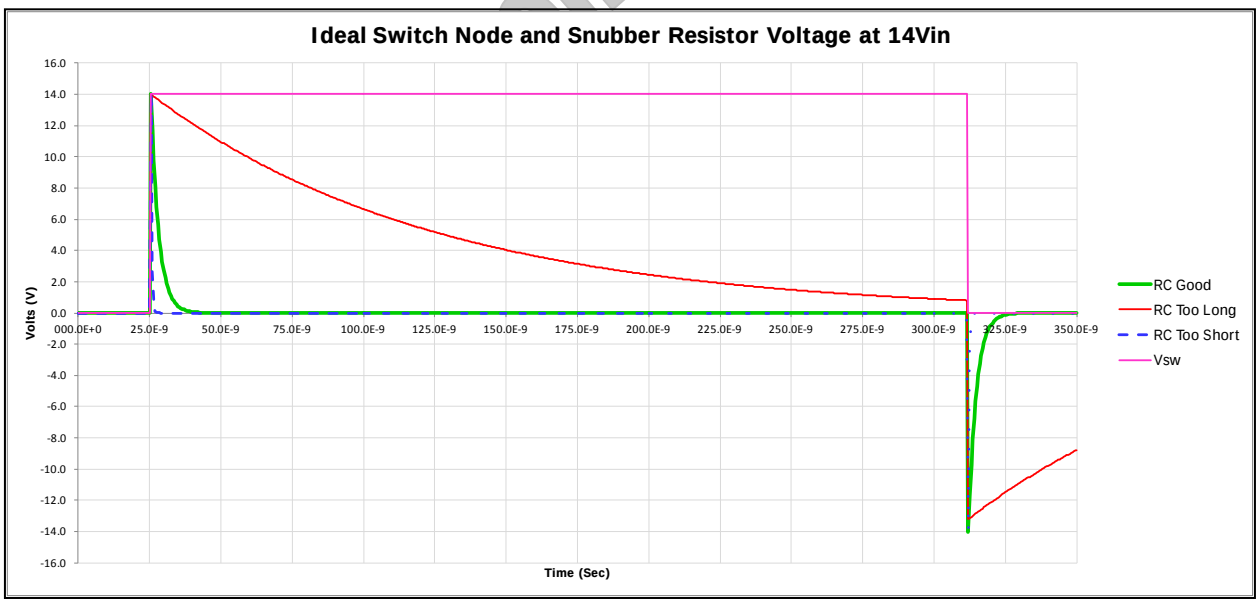


Figure 10: **Ideal Snubber waveforms**

5.5.6 Loop Compensation Components

The natural response, or plant, of this power converter is determined by the voltage mode topology, the output inductor, the output capacitors, and the DC gain of the controller. Once these parameters are determined, the plant

can be calculated. The output inductor and capacitor have already been determined, and from the TPS40422 datasheet we can find the DC gain, and it is specified as 8.3V/V. Combining these parameters together we can calculate the plant. These calculations will not be shown here, but the resulting plant is shown in Figure 11:below.

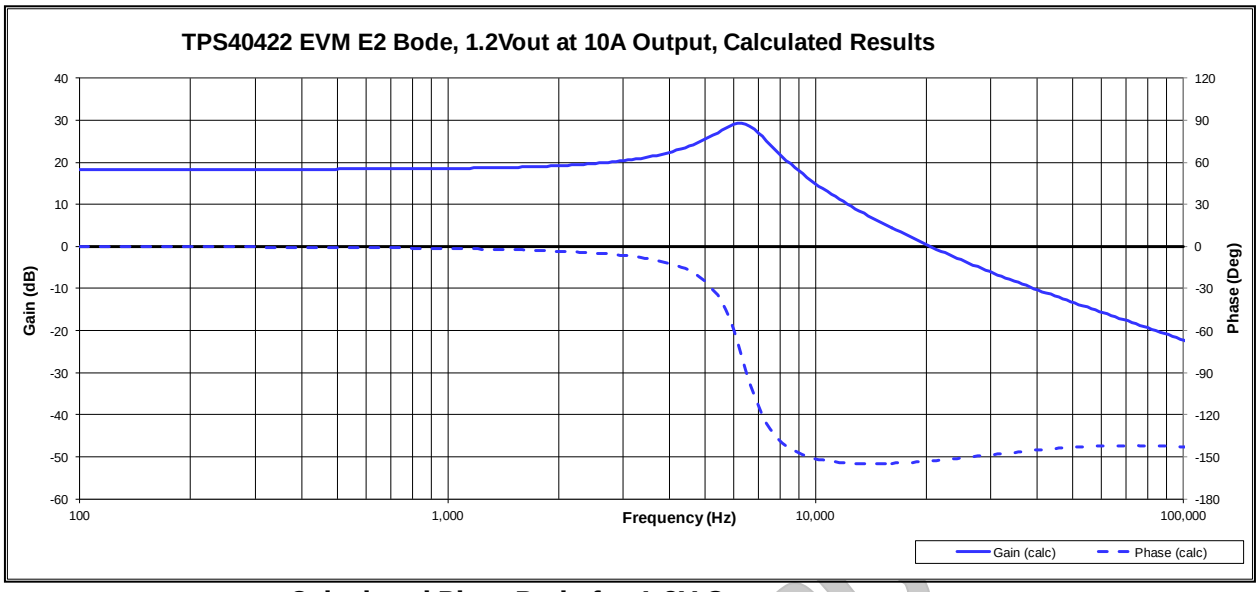


Figure 11: **Calculated Plant Bode for 1.2V Output**

Shown above is the calculated plant Bode. The desired crossover frequency was chosen at a target of approximately 4x Fo, or 20kHz, where Fo is:

Equation 14 Output L-C F_0

$$F_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{750n \times 1004u}} = 5.8kHz$$

The Texas Instruments SwitcherPro design tool was used along with Venable's K-Factor method to compensate the above plant, and this yields the following 5 compensation component values for a Type-III compensator. Measured results are given in the Performance Data section.

Component Location	Value
R14	4.75kΩ
R15	20kΩ
C24	470pF
C25	1.2nF
C26	120pF

5.5.7 Output Voltage Set Point, Rbias

The output voltage can be set by choosing and calculating R1 and Rbias using Equation 15.

Equation 15 Vout Set Point

$$R_{bias} = \frac{V_{ref} \times R_1}{V_{out} - V_{ref}} \quad \text{or using the schematic Ref Des:} \quad R_{13} = \frac{V_{ref} \times R_{12}}{V_{out} - V_{ref}} = \frac{0.6 \times 47.5k}{1.2 - 0.6} = 47.5k$$

In this design R12 was chosen to be 47.5kΩ. R13 is calculated to also be 47.5kΩ.

5.5.8 Remote Sensing

Remote sensing can be done with the integrated differential amplifier. The VSNS1 and GSNS1 lines, which are the inputs to the differential amplifier, should be remotely connected to the load as well as through low-ohm resistors to the output connector. This configuration is used to compensate for voltage drops in the high current paths between the converter output and the load. This is typically used to improve load regulation in high current designs. Resistors R17 and R18 in the schematic are used in case the sense connections fail or get damaged. In this case, these resistors would prevent the converter from going into an open loop condition where a high voltage on the output could occur that could damage the load or the converter. The values of R17 and R18 are bound by an upper value such that the voltage drop across them does not introduce appreciable error from the bias current, and a lower value such that the voltage drop in the load wires which appears across these resistors does not dissipate appreciable power. Values of 10Ω to 50Ω are usually chosen.

6 Performance Data, 1.2Vout

6.1.1 Output Ripple, Measured Results

Shown below is a comparison of the calculated (simulated) output ripple versus the actual measured output ripple with the selected capacitors. Note that this is not a perfect match, and the differences are due to the typical values used in the calculations versus the actual values which often have a lower than typical ESR value.

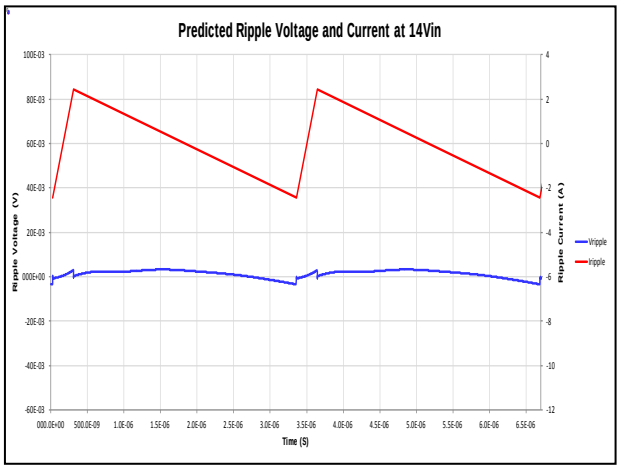
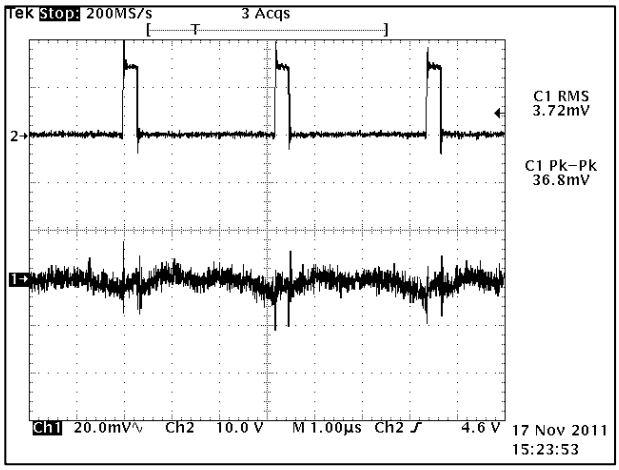
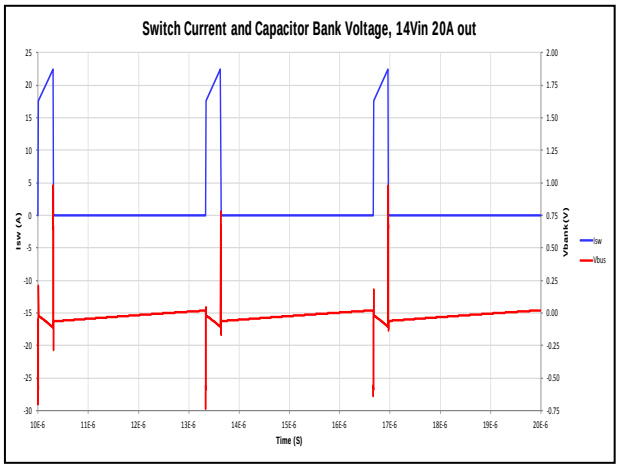
Calculated Ripple Current and Voltage	Measured Vsw and Ripple Voltage
	

Figure 12: **Calculated Output Ripple vs Measured Output Ripple**

6.1.2 Input Ripple, Measured Results

Calculated Switch Current and Input Ripple Voltage	Measured Vsw and Input Ripple Voltage
14Vin 20A Out	14Vin 20A Out



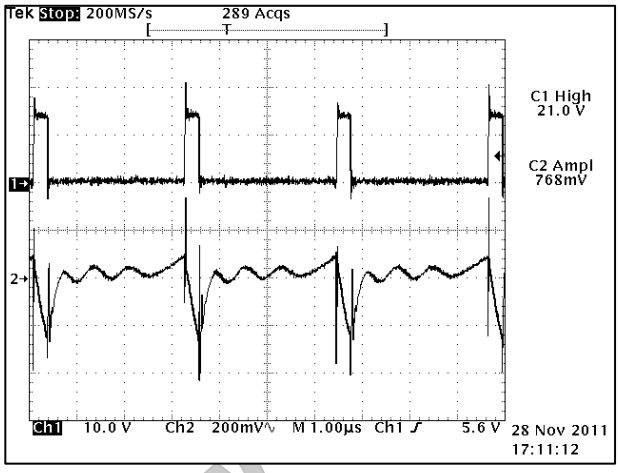


Figure 13: **Calculated Input Ripple vs Measured Input Ripple**

It is recommended that the supply line impedance be kept as low as possible by using short connections and sufficient wire gauge.

6.1.3 Measured Efficiency, 1.2V Output Only, Measured Results

Shown below is the measured efficiency of the EVM with only the 1.2V output operating. These measurements were taken with Vin measured at the input cap closest to the switching FETs, and Vout measured from the inductor pin to the same input cap return.

Figure 14: **Measured Efficiency of 1.2V Output Only**

6.1.4 Load Regulation, 1.2V Output Only

Shown below is the load regulation of the EVM of the 1.2V output.

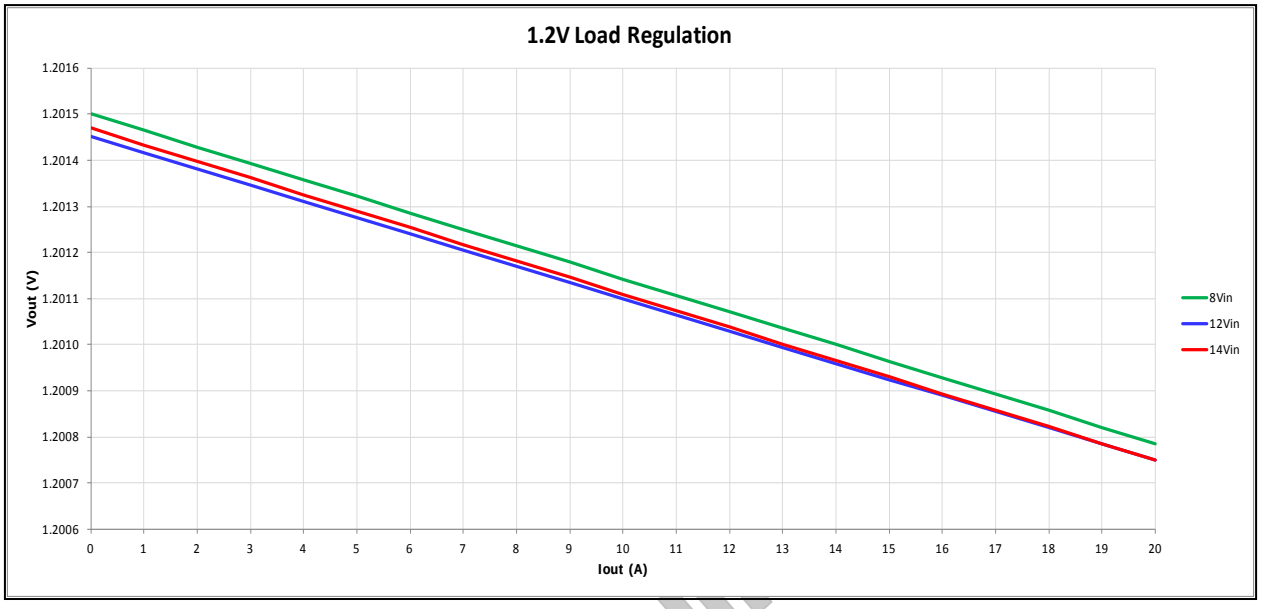


Figure 15: **Load Regulation of 1.2V Output**

6.1.5 Measured Loop Bode, 1.2V Output

Shown below is the measured and calculated Loop Bode response of the EVM for the 1.2V output.

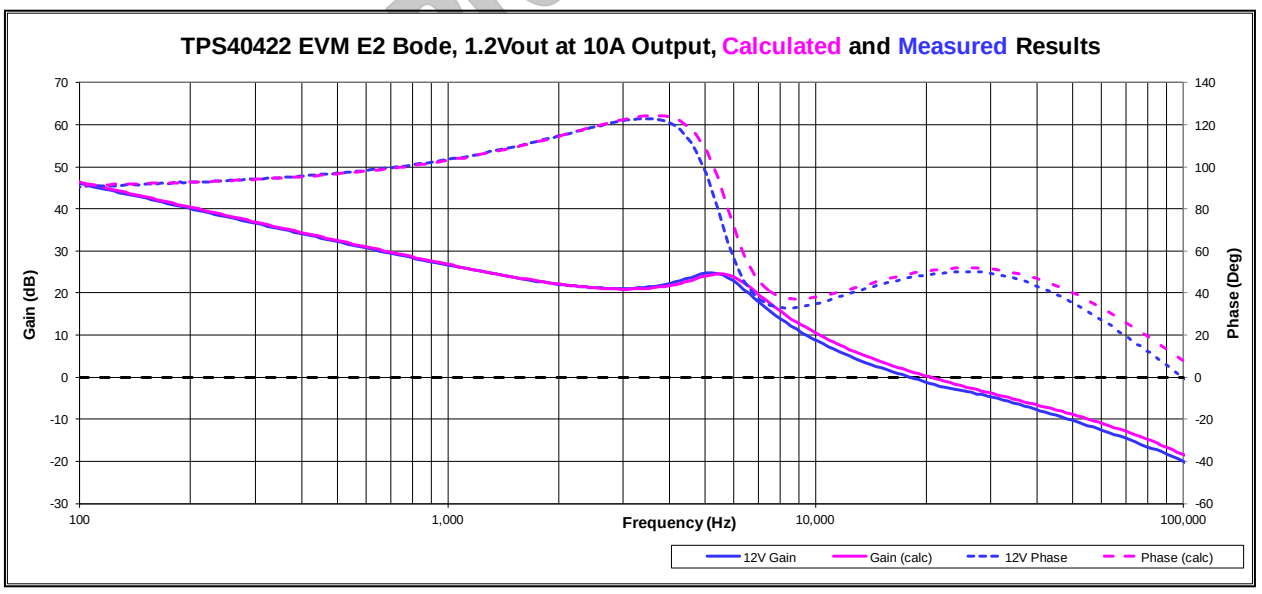


Figure 16: **Measured Closed Loop Bode**

6.1.6 **Startup Waveform, 1.2V Output**

Shown below is the measured startup of the 1.2V output.

Input	**Output**	**Iout**	
12V	1.2V	20A	
Ch1	**Ch2**	**Ch3**	
Vout1 at 200mV/box	Iout1 at 5A/box	Vin at 5V/box	
Ch2 is inverted to better display V and I.			

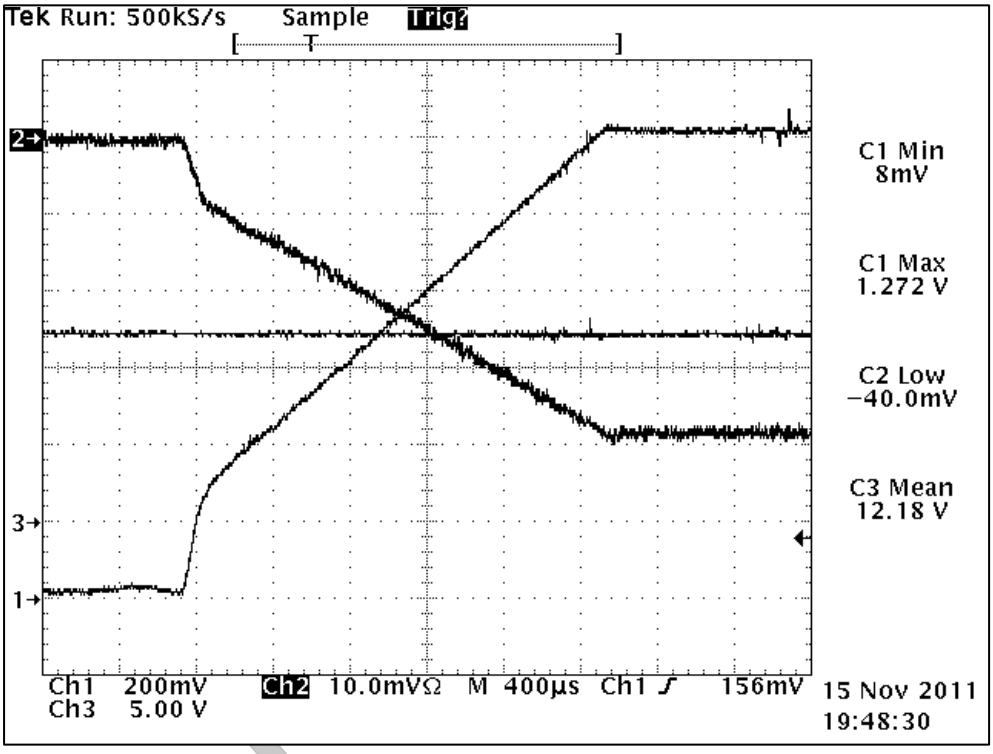


Figure 17: **Measured Startup Waveform**

6.1.7 Transient Response, 1.2V Output

Shown below is the measured transient response of the 1.2V output.

Output	Input	Transient	Ch1	Ch2
1.2V	12V	5A-11A-5A	Vout at 50mV/box	Iout at 5A/box

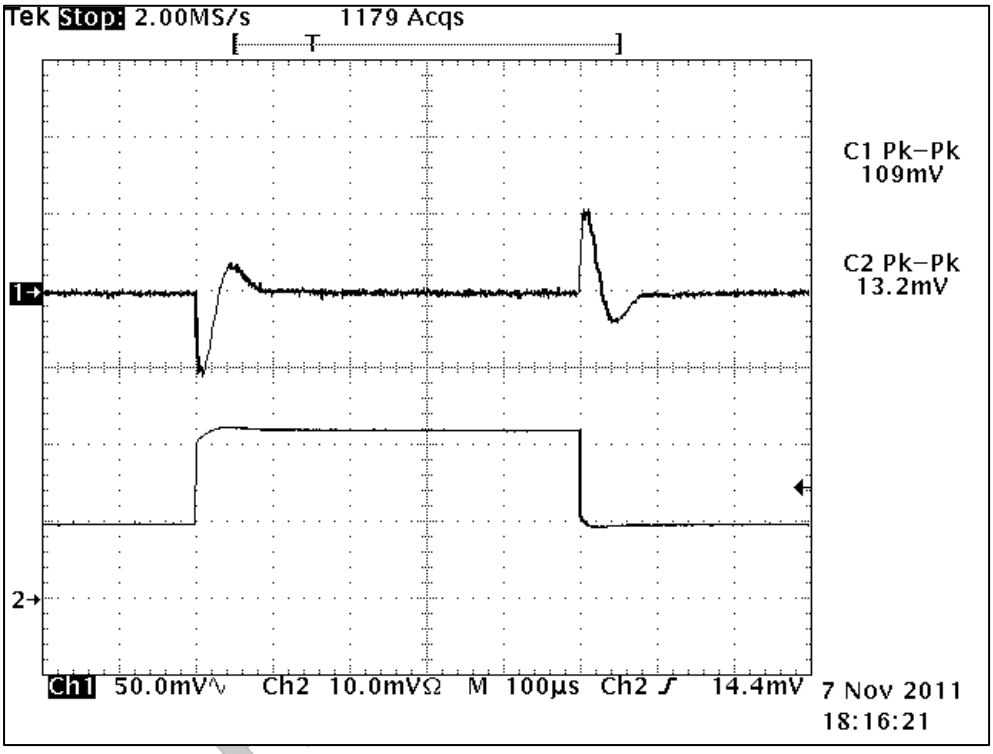


Figure 18: **Measured Pulse Response**

7 Electrical Performance Specifications, 3.3V at 15A

Table 3: **3.3V Design Electrical Parameters**

Parameter	Symbol	Notes and Conditions	Min	Nom	Max	Units
INPUT CHARACTERISTICS						
Input Voltage	Vin		8	12	14	V
Input Current	Iin	Vin = 8V, Iout = 15A	-	6.5	-	A
No Load Input Current		Vin = 12V, Iout = 0A	-	60	-	mA
Vin Start Voltage	Vin_START		-	7	-	V
Vin Stop Voltage	Vin_STOP		-	5	-	V
OUTPUT CHARACTERISTICS						
Output Voltage	Vout	Vin = 12V, Iout = 15A	2.97	3.3	3.63	V
Line Regulation		Vin = 8V to 14V, Iout = 15A	-	-	0.5	%
Load Regulation (at sense points)		Vin = 12V, Iout = 0A to 15A	-	-	0.5	%
Output Ripple Voltage	Vout_ripple	Vin = 12V, Iout = 15A	-	-	50	mVpp
Output Current	Iout	Vin = 8V to 14V	0		20	A
Output Over Current Inception Point	IOCP	Vin = 12V	16	20	34	A
Soft-Start	SS	(default)	-	2.6	-	mSec
Transient Response						
Load Step	ΔI	Iout = 10A to 5A	-	5	-	A
Load Slew Rate			-	1	-	A/µS
Overshoot			-	100	-	mV
Settling Time			-	100	-	µS
SYSTEM CHARACTERISTICS						
Switching Frequency	Fsw			300		kHz
Peak Efficiency	η_{pk}	Vin = 12V, Iout = 0A to 20A	-	93	-	%
Full Load Efficiency	η	Vin = 12V, Iout = 20A	-	90	-	%
Operating Temperature Range	Toper	Vin = 8V to 14V, Iout = 0A to 20A	-40		60	°C

8 Design Calculations, 3.3Vout

Following are detailed design calculations of the components in the above Buck converter with the specifications in Table 3:.

8.1 Power Components: Output Inductor, Output Capacitor Bank, FETs, and Input Capacitor Bank

In an effort to simplify the BOM and the design itself, the same power components will be used. Not only does this simplify the calculations, but note that the EVM can be configured for different output voltages, so the selection of power components can be done on a case by case approach as needed. The majority of the following calculations are reduced to verifying that these components are also suited for the different voltage and power of Vout 2.

More details:

Parameter	Note	Value
Fsw	Switching Frequency	300kHz (defined)
Period	1/(Fsw)	3.33uSec
Duty Cycle (at Vin_max)	Vout/Vin = 3.3/14	23.57%
ON time (at Vin_max)	high-side FET ON = (8.57%)*3.33uSec	785.7nSec
OFF time (at Vin_max)	low-side FET ON = (100-8.57%)*3.33uSec	2.548uSec

For this design a 750nH inductor from Würth (part number 744355182) was selected. The actual ripple current should now be recalculated using the actual inductance value:

$$di = dt\frac{V_L}{L} = 2.547u\frac{3.3}{0.75u} = 11.21Ap\text{-}p$$

With this ripple current, the inductor RMS and Peak current values can be calculated.

$$RMS_{Triangle} = \frac{11.21(p\text{-}p)}{\sqrt{12}} = 3.236A_{RMS}$$

Equation 16 Inductor RMS Current, I_{RMS}

$$I_{RMS} = \text{Root of Sum of Squares of DC and AC Current} = \sqrt{(I_{DC})^2 + (I_{AC})^2}$$

At max load, this leads to:

$$I_{RMS} = \sqrt{(I_{DC})^2 + (I_{AC})^2} = \sqrt{15^2 + \left(\frac{11.21}{\sqrt{12}}\right)^2} = \sqrt{225 + 10.47} = 15.35\ A_{RMS}$$

At max load and max line, the peak inductor current is given by:

$$I_{Peak} = I_{DC} + \frac{(I_{p\text{-}p})}{2} = 15 + \frac{11.21}{2} = 20.6\ A_{Peak}$$

The conduction losses in the inductor can be calculated with RMS current and the DC resistance (DCR) of the inductor. The DCR of the selected inductor, from the datasheet, is:

$$DCR = 0.9m\Omega$$

This leads to:

Equation 17 Inductor Conduction Losses

$$P = I^2R = (I_{RMS})^2DCR = 15.35^2(0.9m\Omega) = 0.2119\ \text{Watts}$$

Using the TINA simulation tool and with the worst case ripple current previously calculated, the resulting ripple voltage for the parallel bank of output capacitors was obtained and is shown here:

8.1.1 Input Capacitance, Cin

The same capacitor bank is used for Vout 2: EEETK1E331UP from Panasonic, electrolytic 330uF, 25V capacitor with 200mΩ of ESR and 100nH ESL, ripple current rating of 270mA, and also the capacitor 22uF ceramic, 25V, 5.5mohm ESR, 0.99nH ESL device, three in parallel.

Shown below are the resulting currents in the input electrolytic and ceramic capacitors (Iceramic and I electro), assuming an infinitely large input inductance. Also shown is the resulting capacitor bank ripple voltage. Note that even with the large value electrolytic capacitor, the very low ESR ceramic capacitors carry the bulk of ripple current, and the resulting ripple in the electrolytic is still within its rating with a value of 220mA$_{rms}$ (calculated but not shown here).

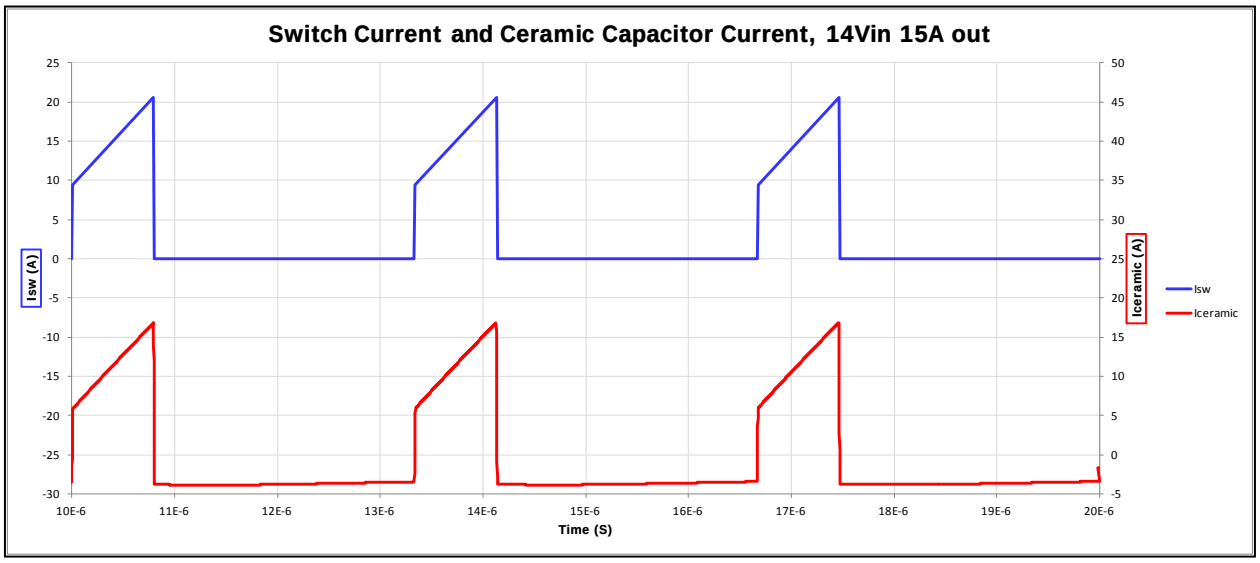


Figure 19: **Switch and Input Ceramic Capacitor Currents at 14Vin and 15A Out**

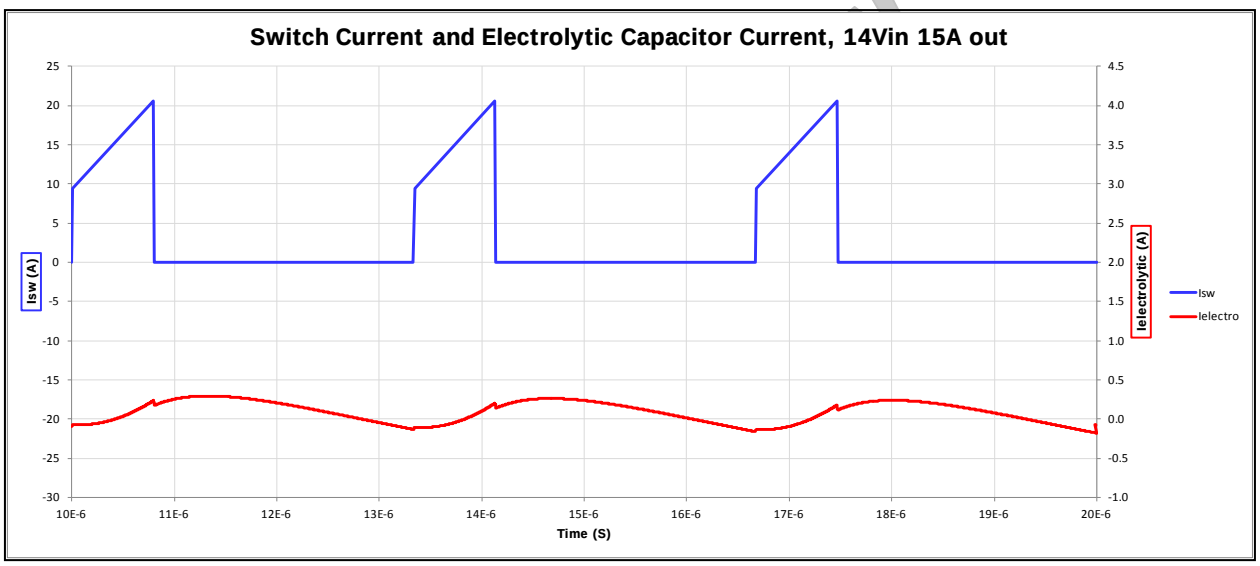


Figure 20: **Switch and Input Electrolytic Capacitor Currents at 14Vin and 15A Out**

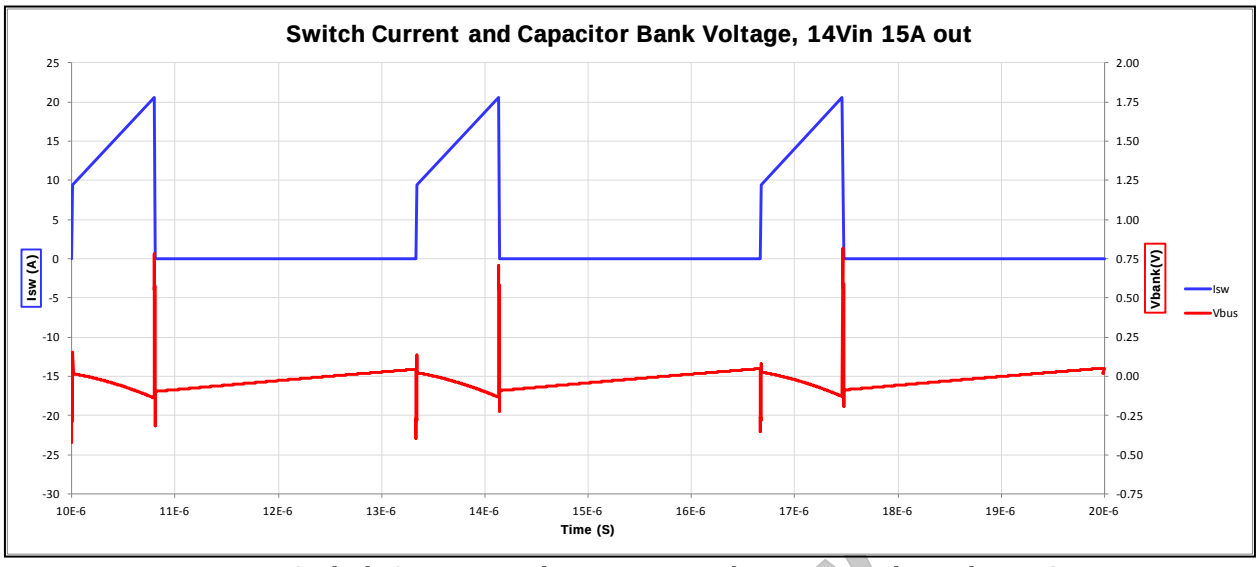


Figure 21: **Switch Current and Input Bus Voltage at 14Vin and 15A Out**

8.1.2 Loop Compensation Components

Since the output filter and PWM gain are the same, the plant is also the same except for the difference in damping resulting from the different load impedance. However, the differences are not significant so the compensation design is the same.

8.1.3 Output Voltage Set Point, Rbias

The output voltage can be set by choosing and calculating R1 and Rbias using Equation 15.

Equation 18 Vout Set Point

$$R_{bias} = \frac{V_{ref} \times R_1}{V_{out} - V_{ref}} \quad \text{or using the schematic Ref Des:} \quad R_{35} = \frac{V_{ref} \times R_{38}}{V_{out} - V_{ref}} = \frac{0.6 \times 47.5k}{3.3 - 0.6} = 10.55k$$

In this design R38 was chosen to be 47.5kΩ. R35 is calculated to be 10.55kΩ, use a standard value of 10.5kΩ.

8.1.4 Remote Sensing

Vout 2 does not offer remote sensing. The VSNS2 and GSNS2 lines are used for reporting purposes only, and should be connected exactly like remote sense lines.

9 Performance Data, 3.3Vout

9.1.1 Output Ripple, Measured Results

Shown below is the actual measured output ripple with the selected capacitors.

Measured Vsw and Output Ripple Voltage

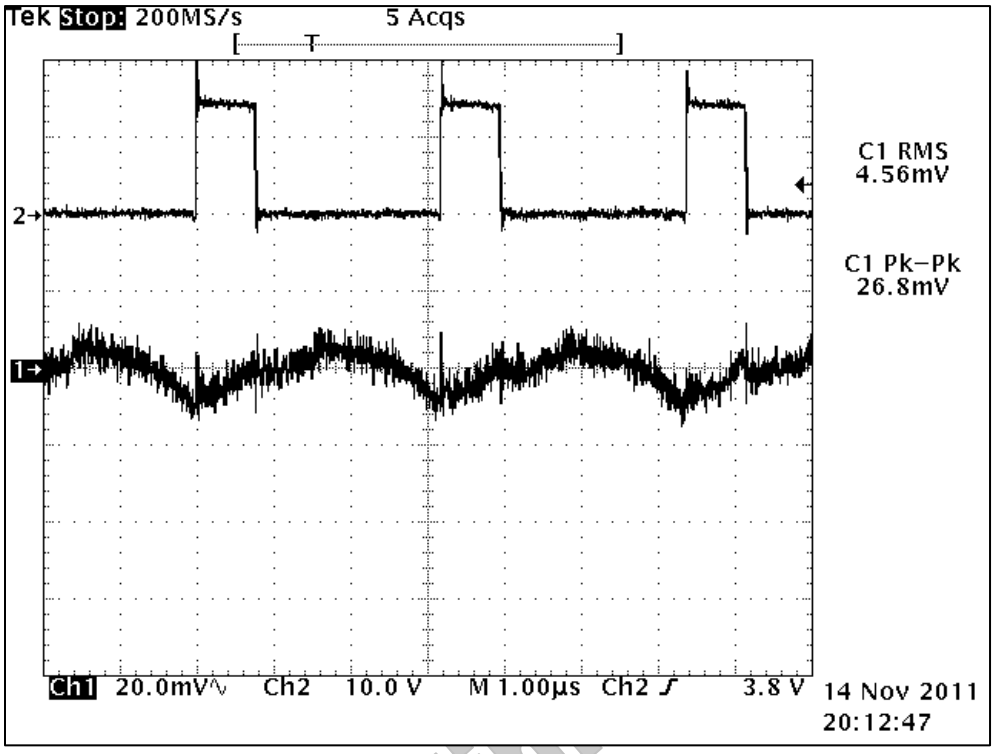


Figure 22: **Measured Output Ripple on 3.3V at 14Vin and 15A out**

9.1.2 Input Ripple, Measured Results

Calculated Switch Current and Input Ripple Voltage	Measured Vsw and Input Ripple Voltage
14Vin 15A Out	14Vin 15A Out

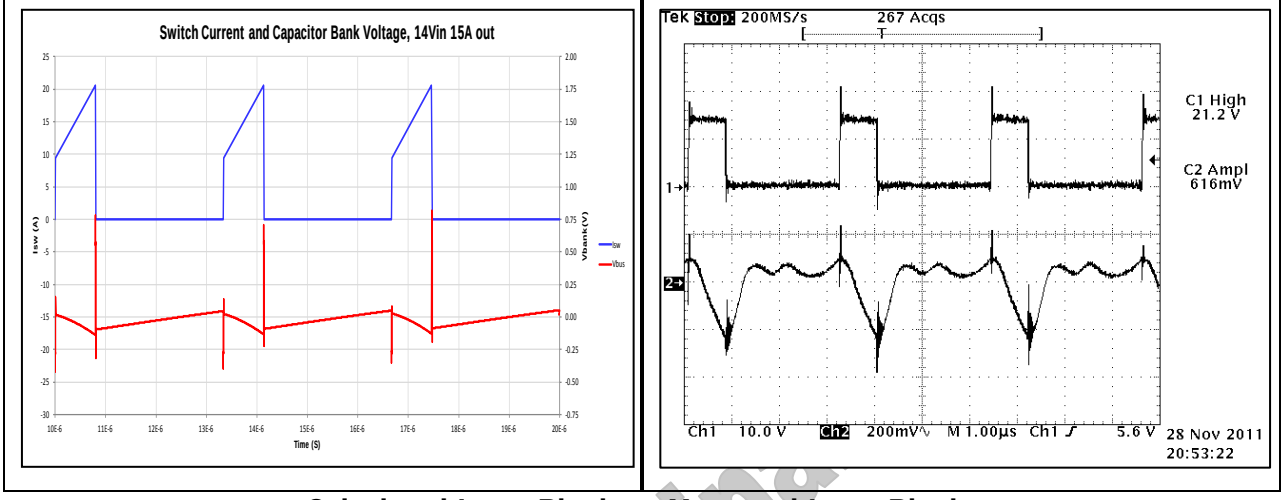


Figure 23: **Calculated Input Ripple vs Measured Input Ripple**

9.1.3 Measured Efficiency, 3.3V Output Only

Shown below is the measured efficiency of the EVM with only the 3.3V output operating. These measurements were taken with Vin measured at the input cap closest to the switching FETs, and Vout measured from the inductor pin to the same input cap return.

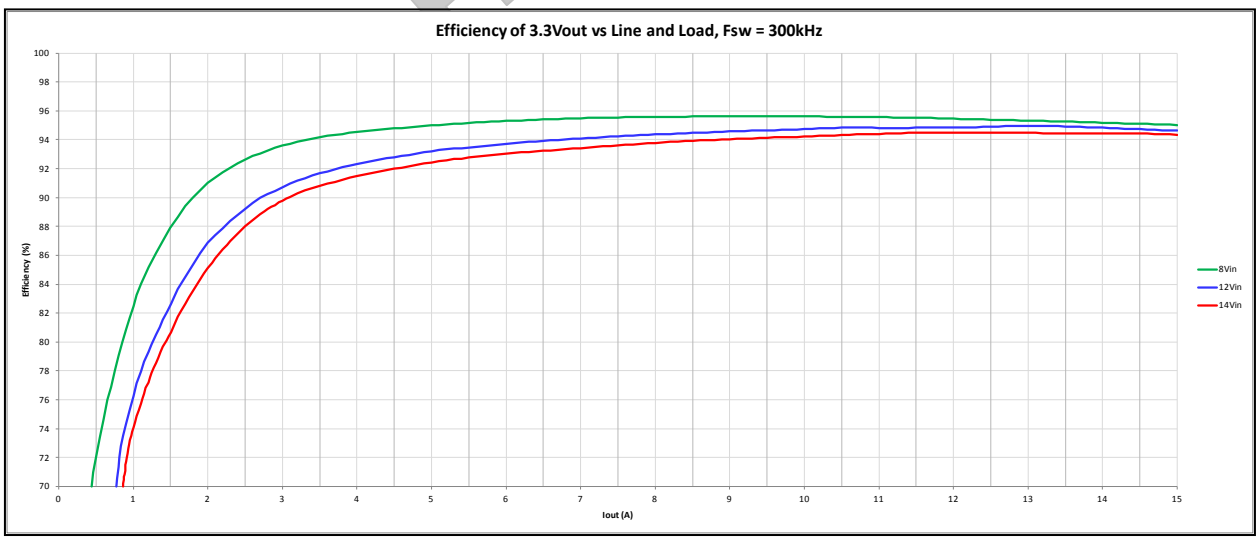


Figure 24: **Measured Efficiency of 3.3V Output Only**

9.1.4 Load Regulation, 3.3V Output Only

Shown below is the load regulation of the EVM of the 3.3V output.

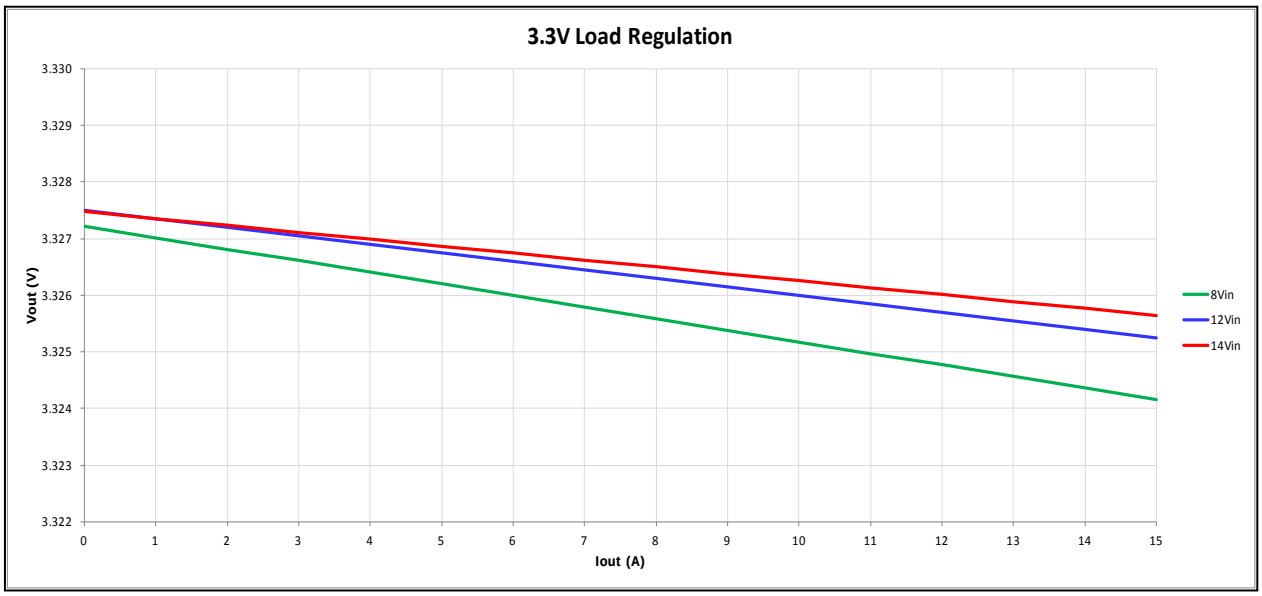


Figure 25: **Load Regulation of 3.3V Output**

9.1.5 Measured Loop Bode, 3.3V Output

Shown below is the measured and calculated Loop Bode response of the EVM for the 3.3V output.

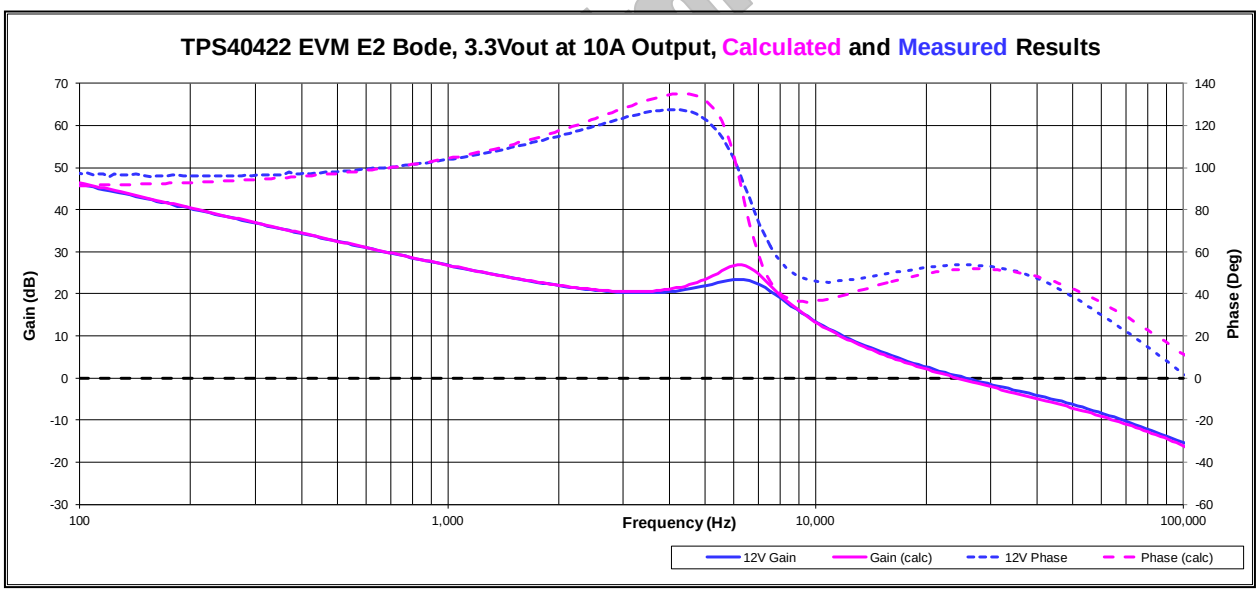


Figure 26: **Measured Closed Loop Bode**

9.1.6 Startup Waveform, 3.3V Output

Shown below is the measured startup of the 3.3V output.

Input	Output	Iout	
12V	3.3V	15A	
Ch1	**Ch2**	**Ch3**	
Vout2 at 500mV/box	Iout2 at 5A/box	Vin at 5V/box	
Ch2 is inverted to better display V and I.			

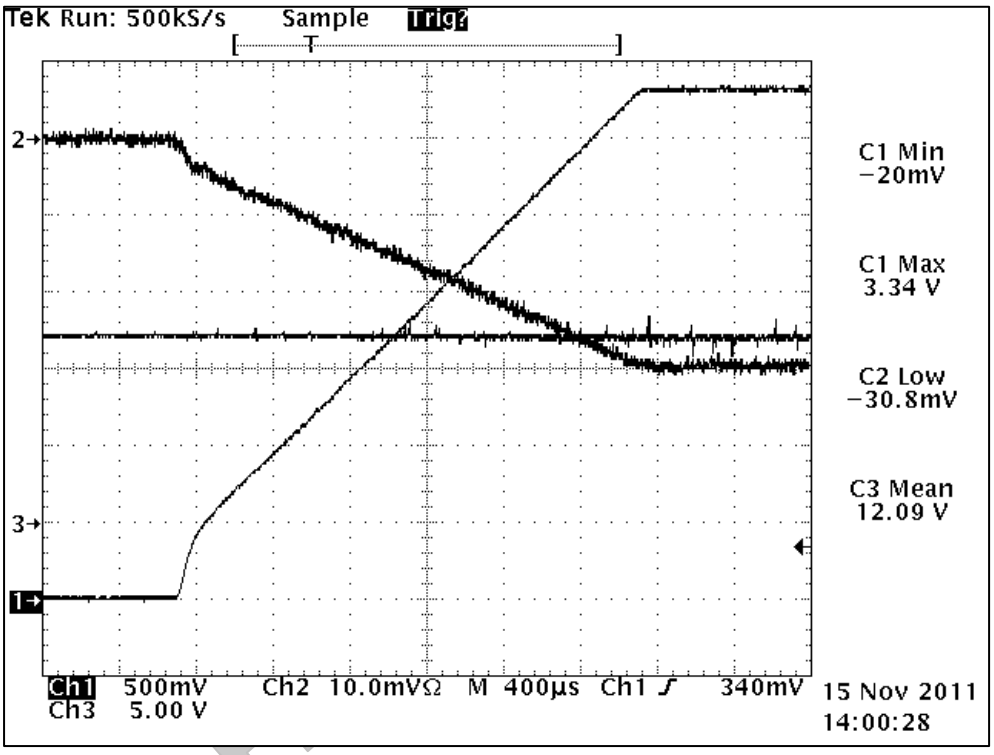


Figure 27: **Measured Startup Waveform**

9.1.7 **Transient Response, 3.3V Output**

Shown below is the measured transient response of the 3.3V output.

Output	Input	Transient	Ch1	Ch2
3.3V	12V	5A-9A-5A	Vout at 20mV/box	Iout at 5A/box

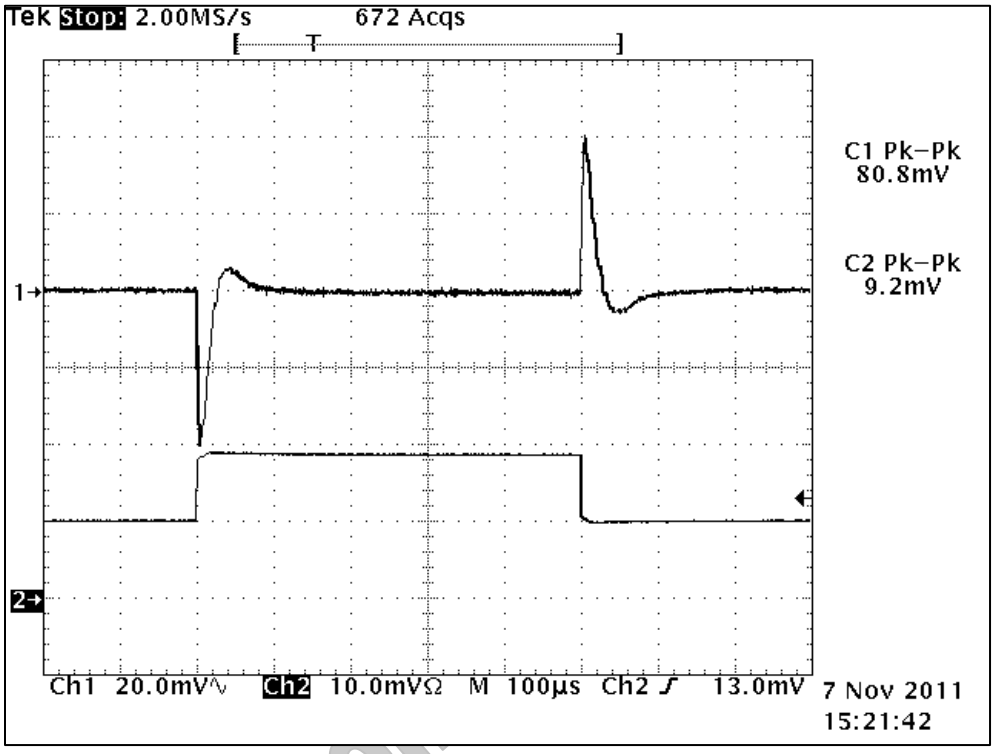


Figure 28: **Measured Pulse Response**

10 Device Configuration

The TPS40422 can be configured via the PMBus (pins CLK and DATA) and the Fusion Digital Power Designer (GUI interface). An example of the configuration window that is used to make internal configuration changes to the TSP40422 is shown below:

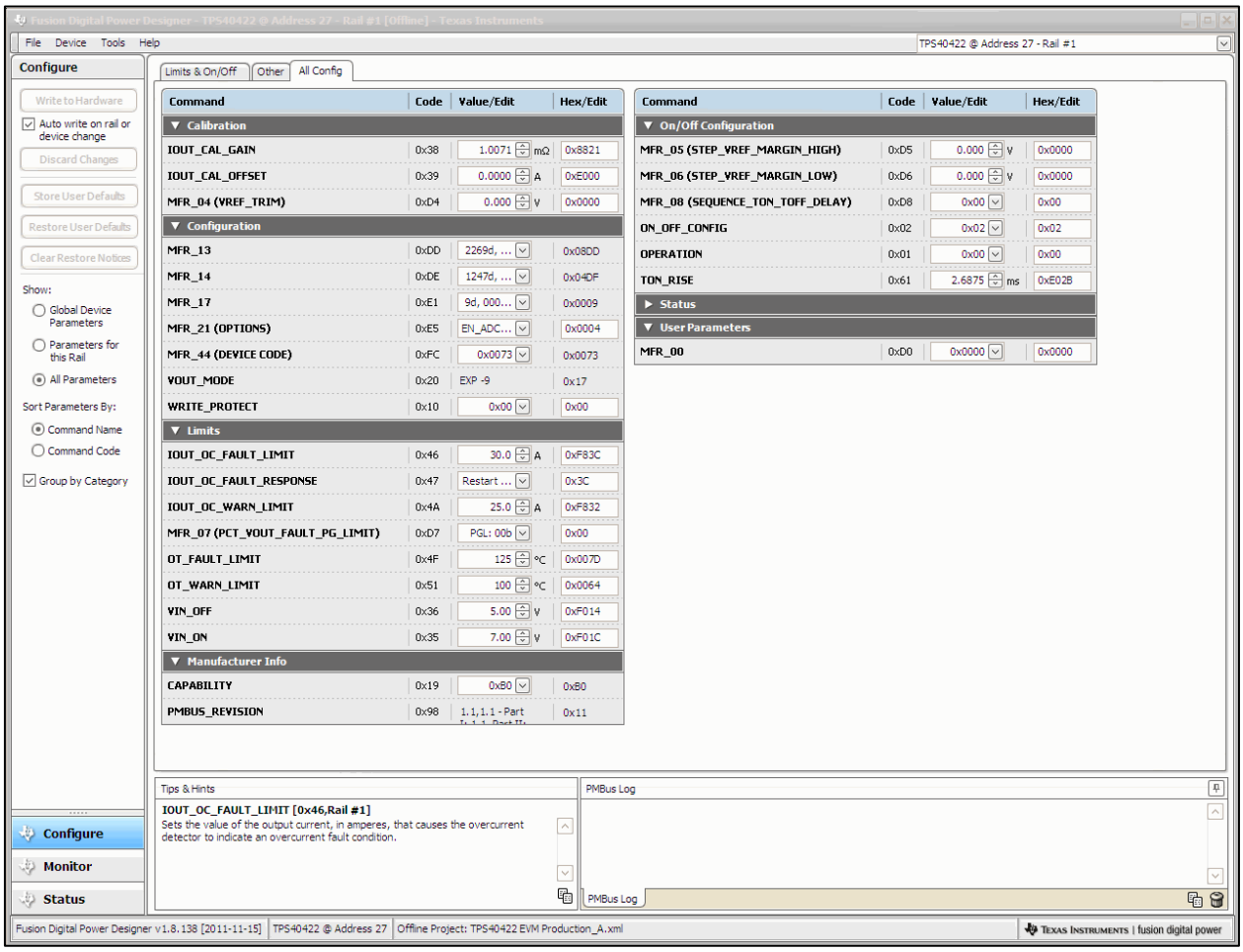


Figure 29: **Advanced Configuration Window**

The figure above shows some of the user configurable parameters of the TPS40422 and is made up of sections; Calibration, Configuration, Limits, and On/Off Configuration. The Status section is read only, and consists of data read from the TPS40422 such as Vout, Iout, Vin, and Status words. A full description of each command and status word is available in the Command Section of the TPS40422 datasheet.

Configuration changes can be implemented by changing the value in the Value/Edit box of each parameter. Most boxes allow direct parameter changes such as voltage or current, but some boxes such as IOUT_OC_FAULT_RESPONSE provide a pop-up configuration window as shown below, and others provide a pull-down menu. Select the appropriate radio buttons to make the desired changes.

Once a parameter has been modified, it must be written to the device in one of two ways. The changes can be saved to volatile memory or non-volatile memory. To commit the changes to volatile memory, click on the “Write to Hardware” button. This will store the changes to the device in but these changes will be lost when input power is

cycled. To commit the changes to non-volatile memory, click on the “Store User Defaults” button, or equivalently “Device: Store User Configuration to Flash Memory” pull-down menu.

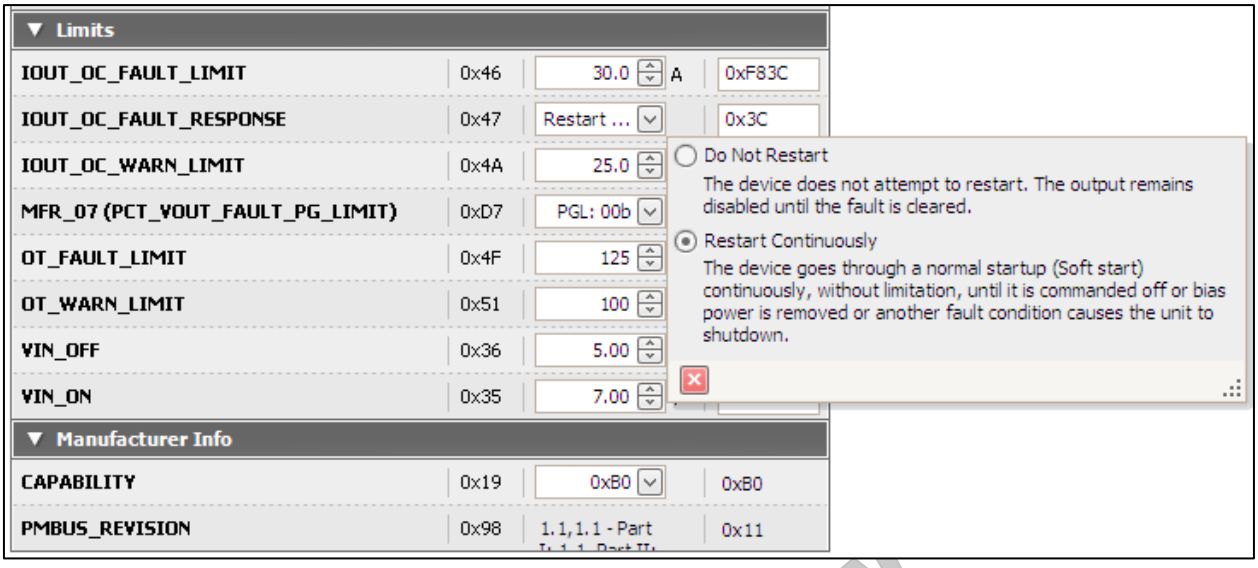


Figure 30: **IOUT_OC_FAULT_RESPONSE Configuration Window**

11 TPS40422 EVM PWR091 Assembly Drawing and PWB Layout

The following figures (Figure 32: through Figure 36:) show the design of the TPS40422 EVM PWR091 printed circuit board.

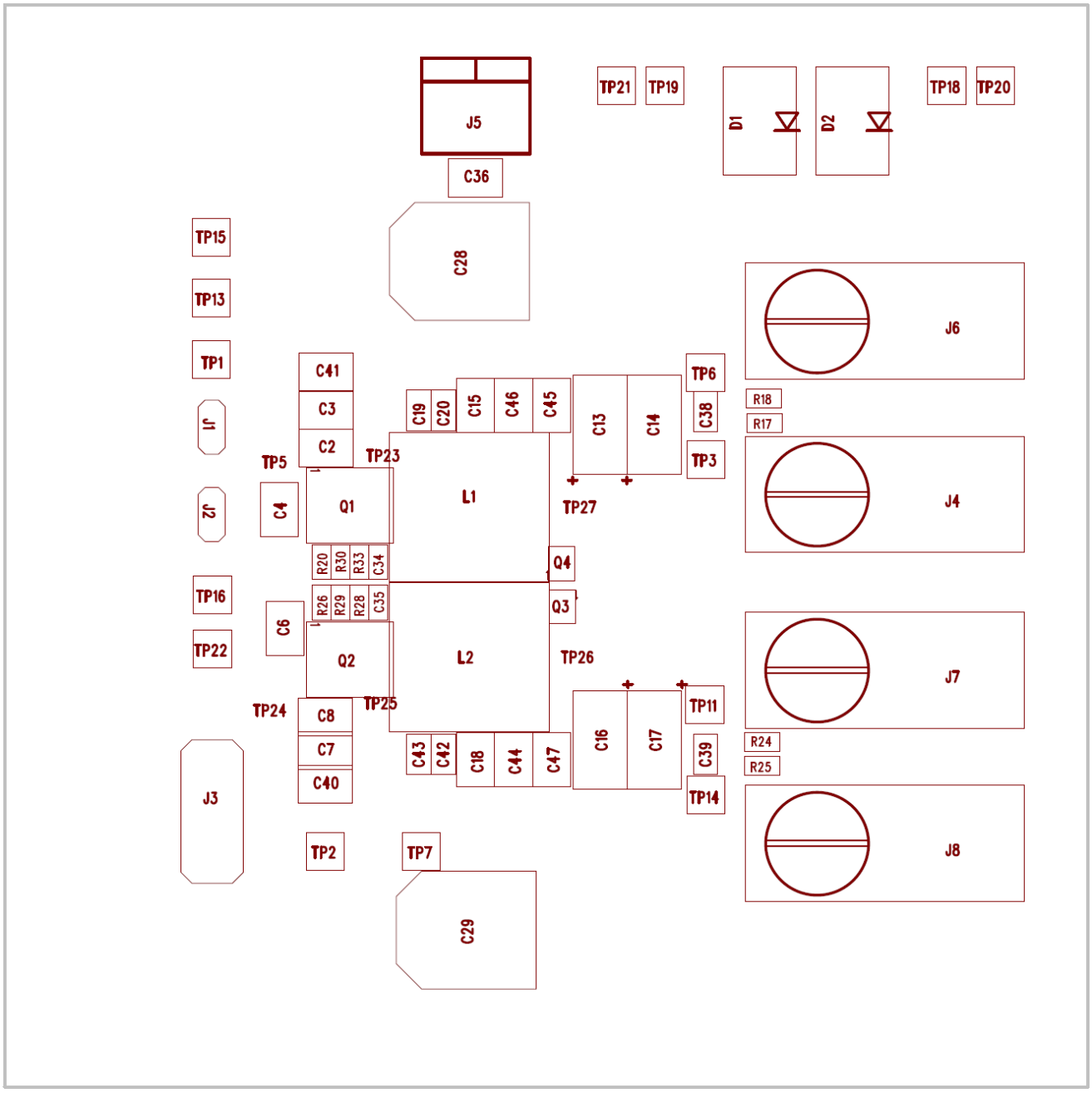


Figure 31: **PWR091 EVM Top Layer Assembly Drawing (Top View)**

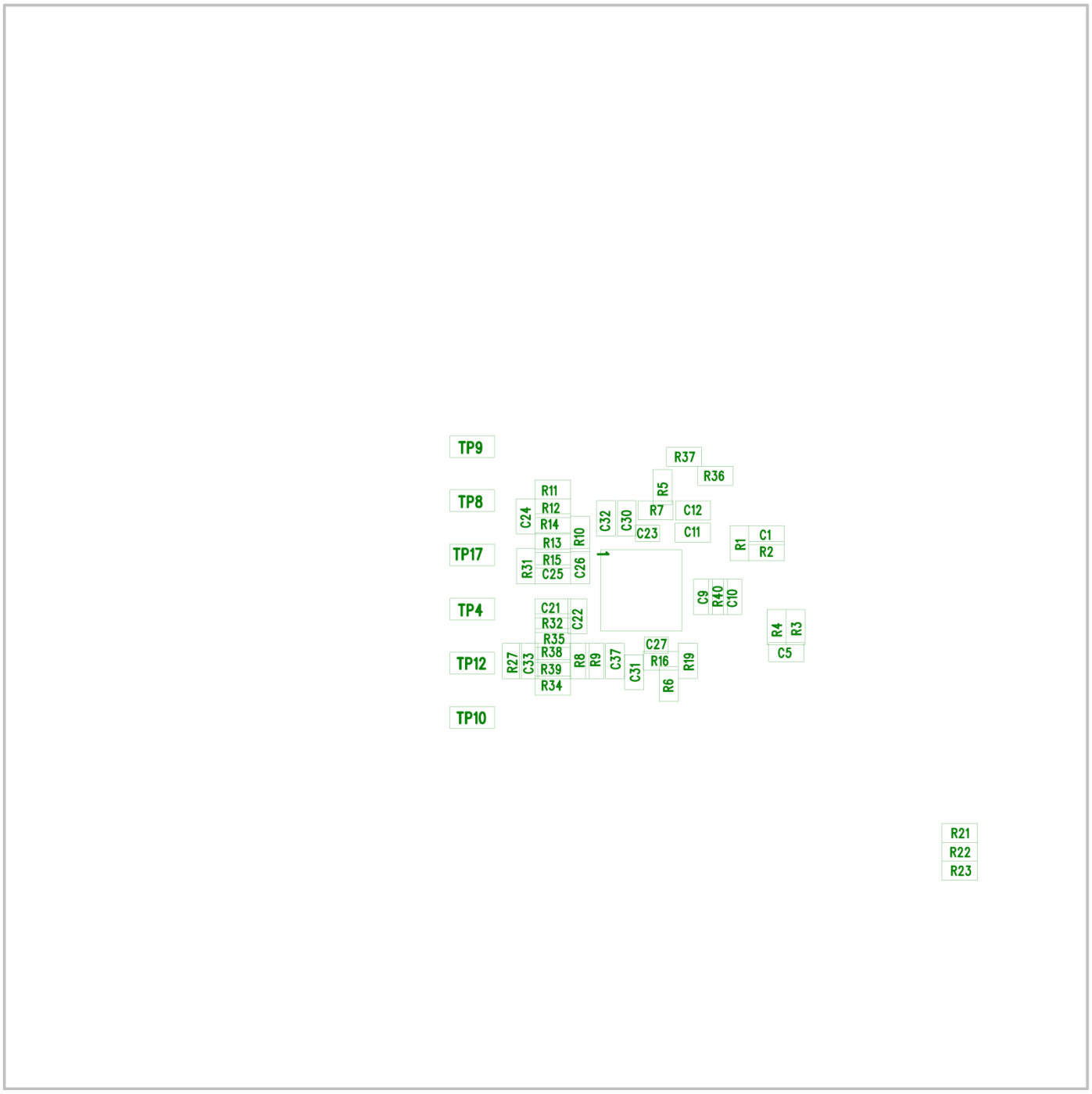


Figure 32: **PWR091 EVM Bottom Assembly Drawing (Bottom view)**

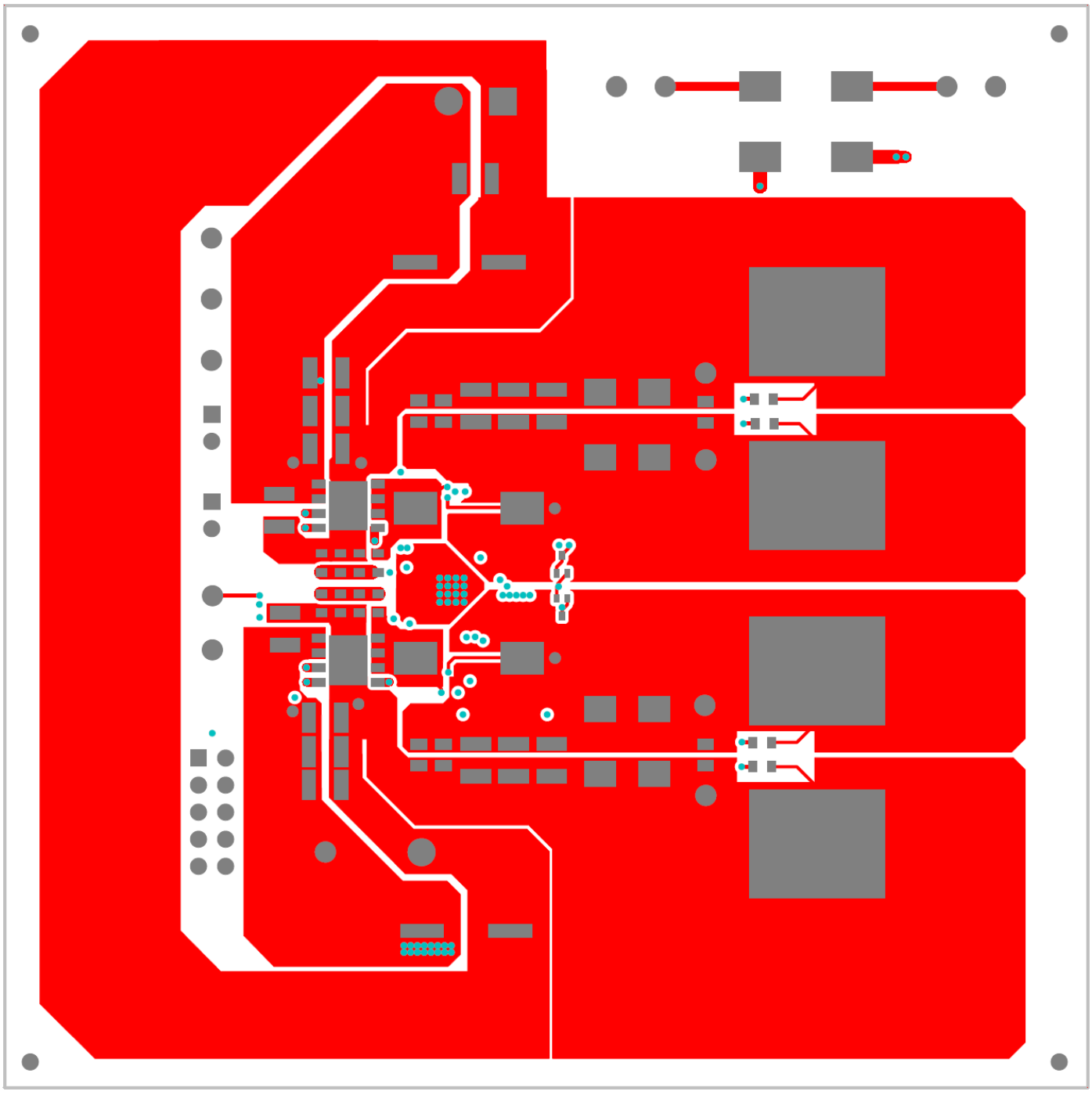


Figure 33: **PWR091 EVM Top Copper (Top View)**

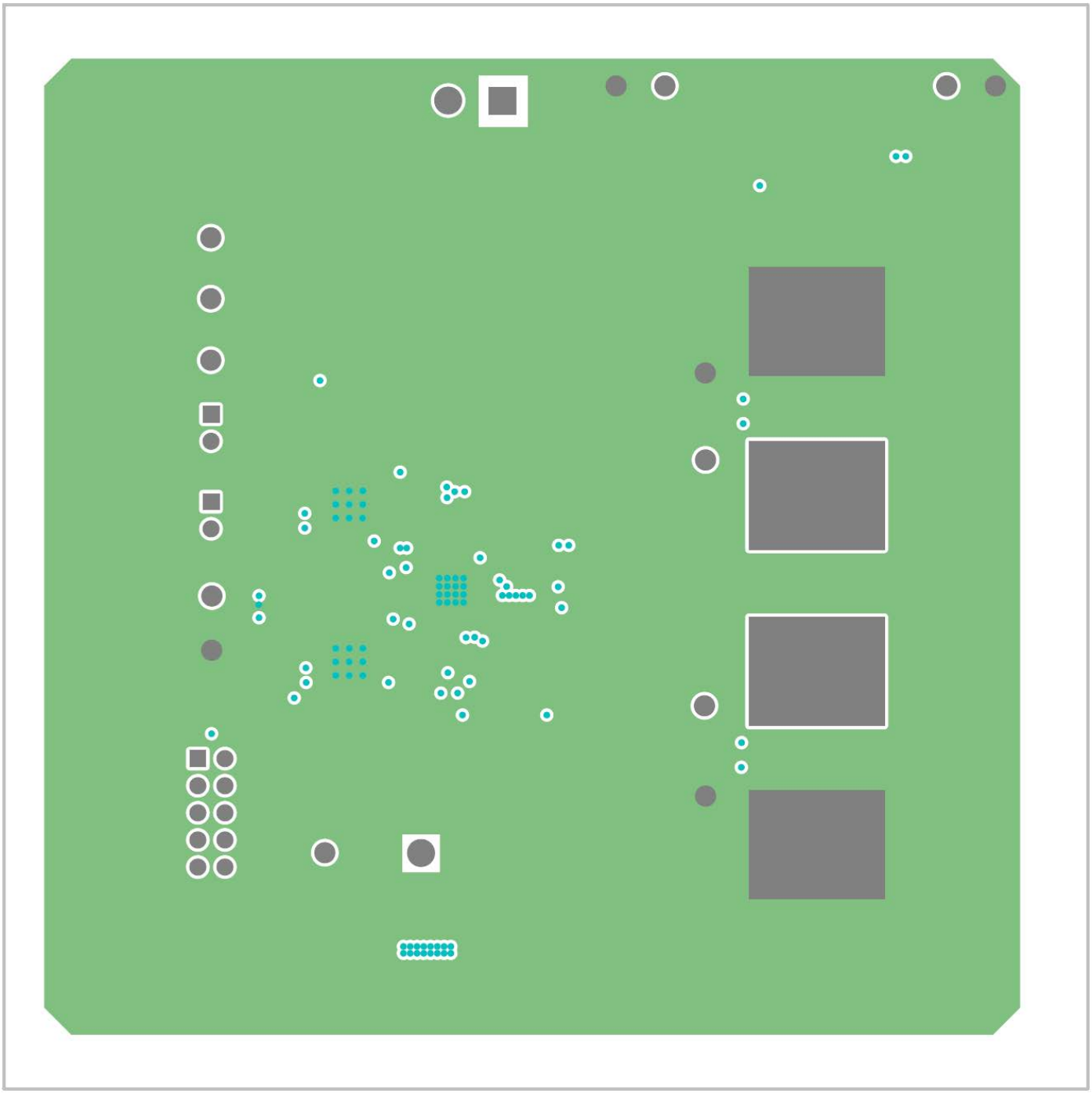


Figure 34: **PWR091 EVM Internal Layer 1 (Top View)**

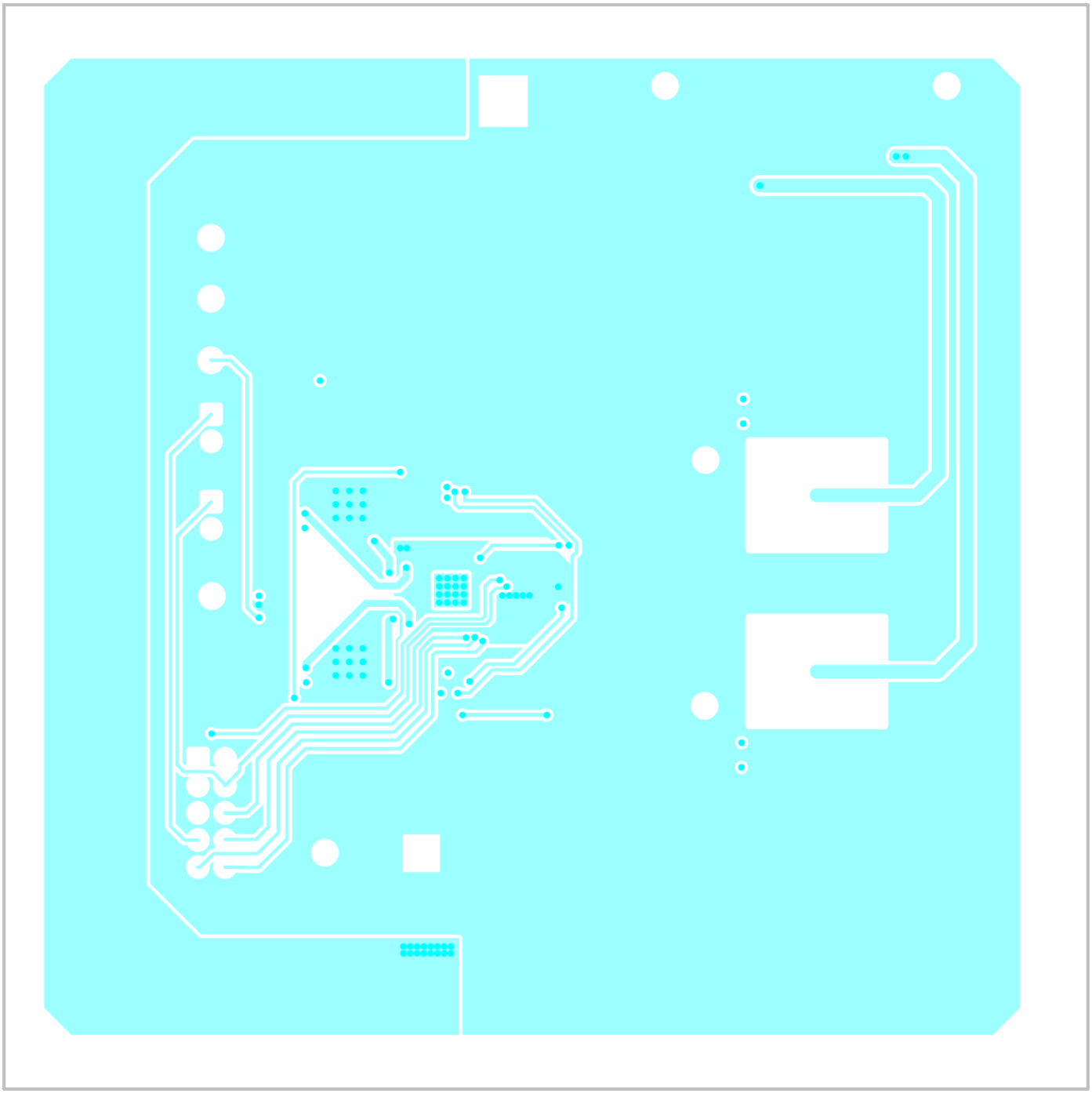


Figure 35: **PWR091 EVM Internal Layer 2 (Top View)**

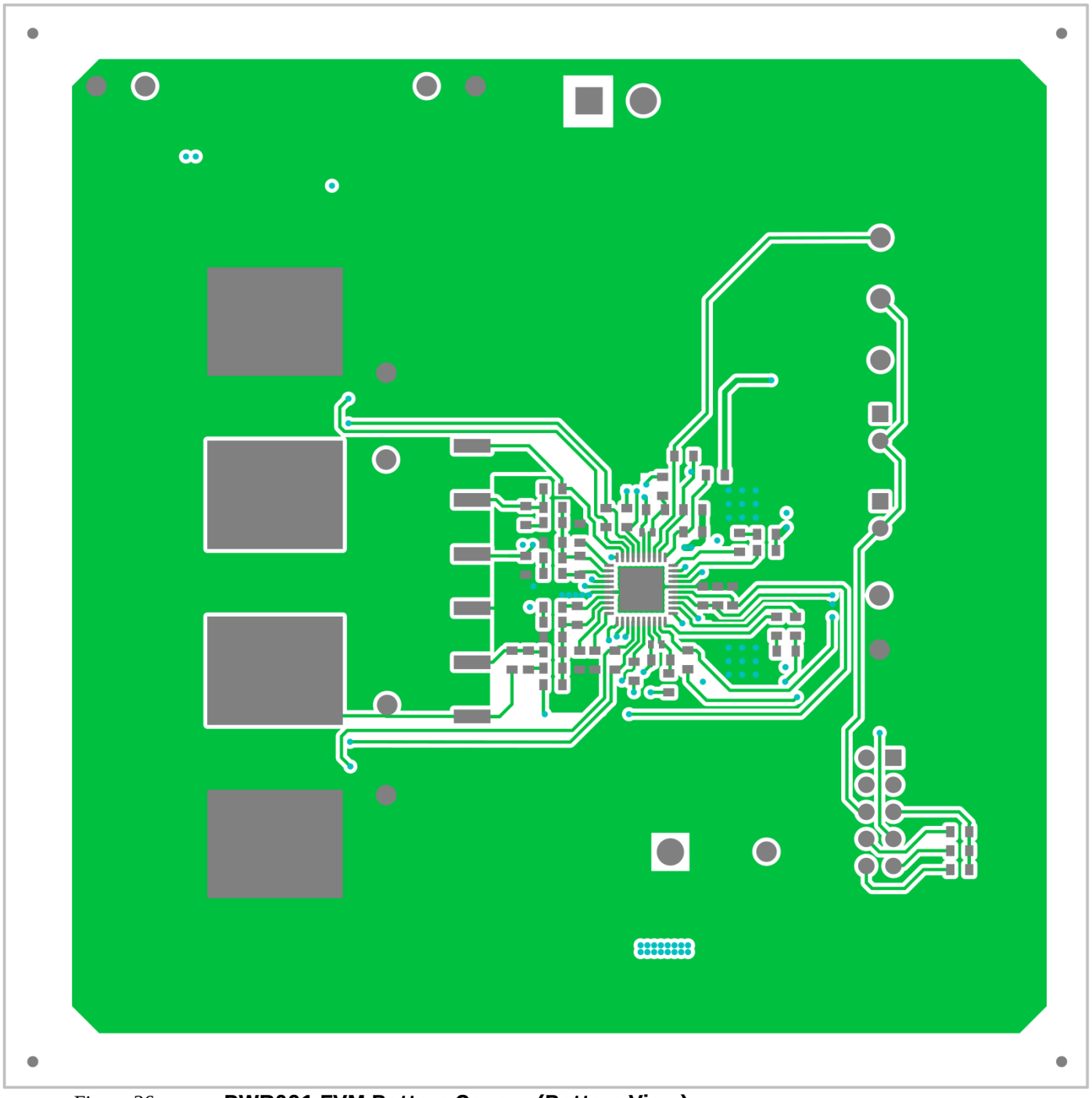


Figure 36: **PWR091 EVM Bottom Copper (Bottom View)**

12 Bill of Materials

Table 4: **EVM components list from the schematic shown in Figure 9:**

Qty	REFDES	Description	MFR	Part_Number
2	C23 C27	0.47uF, Ceramic, 16V, X5R, 10%, 0402	STD	STD
3	C1 C5 C9	0.1uF, Ceramic, 50V, X7R, 10%, 0603	STD	STD
3	C10-12	1.0uF, Ceramic, 25V, X7R, 10%, 0603	STD	STD
2	C21 C25	1.2nF, Ceramic, 50V, X7R, 10%, 0603	STD	STD
2	C24 C33	470pF, Ceramic, 50V, X7R, 10%, 0603	STD	STD
2	C26 C22	120pF, Ceramic, 50V, NP0, 5%, 0603	STD	STD
6	C31-32 C30 C34-35 C37	1000pF, Ceramic, 50V, X7R, 10%, 0603	STD	STD
4	C19-20 C42-43	22uF, Ceramic, 6.3V, X5R, 20%, 0805	STD	STD
2	C38-39	0.1uF, Ceramic, 6.3V, X5R, 20%, 0805	STD	STD
9	C2-4 C6-8 C36 C40-41	22uF, Ceramic, 25V, X5R, 20%, 1210	STD	STD
6	C18 C15 C44-47	100uF, Ceramic, 6.3V, X5R, 20%, 1210	STD	STD
2	C28-29	330uF, Electrolytic, Aluminum, 25V, 200mohm, 270mArms, 0.406 x 0.406	Panasonic	EEE-TK1E331UP
4	C13-14 C16-17	330uF, Polymer Cap, 330uF, 6.3V, 0.015 Ohms, 20%, 7343(D)	Kemet	T520D337M006ATE015
4	J4 J6-8	33457, Lug, Solderless, #10 - #10-12 AWG, Copper/Tin, Uninsulated, 0.375 x1.00"	Std	CX35-36-CY
2	D1-2	MBRS340, Diode, Schottky, 3A, 40V, SMC	Fairchild	MBRS340
2	J1-2	PEC02SAAN, Header, Male 2-pin, 100mil spacing,, 0.100" x 2	Sullins	PEC02SAAN
1	J3	AWHW10G, Header, Male 2x5-pin, 100mil spacing, 0.100" x 5 X 2	Assmann	AWHW10G-0202-T-R
2	L1-2	820nH, Inductor, SMT, 27A, Shielded, 20%, 0.9mOhm, 0.512" x 0.571"	Wurth	744355182
2	R1 R4	5.1, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
1	R3	0, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
1	R2	0, Resistor, Chip, 1/10W, 5%, 0603	STD	STD
2	R5-6	2.0k, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
0	R7 R16 R21-23 R34	Open, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
3	R12 R13 R38	47.5k, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
2	R8-9	36.5k, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
11	R17 R18 R20 R24-26 R28-30 R33 R36	10, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
1	R10	40.2k, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
3	R11 R27 R31	49.9, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
2	R15 R32	20k, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
1	R35	10.5k, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
3	R19 R37 R40	10.0k, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
2	R14 R39	4.75k, Resistor, Chip, 1/10W, 1%, 0603	STD	STD
1	J5	ED120/2DS, Terminal Block, 2-pin, 15-A, 5.1mm, 0.40" x 0.35"	OST	ED120/2DS
1	U1	TPS40422RHA, IC, PMBUS synchronous buck controller, QFN-40	TI	TPS40422RHA

2	Q1-2	CSD87350Q5D, MOSFET, Dual N-Chan, 30-V, 30-A, QFN-8 POWER	TI	CSD87350Q5D
2	Q3-4	MMBT3904, Bipolar, NPN, 40V, 200mA, 200mW, SC-75	On Semi	MMBT3904TT1G
1	PCB	PCB, FR-4, 0.062, 2oz Copper all layers., 4.00" x 4.00"	STD	STD

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