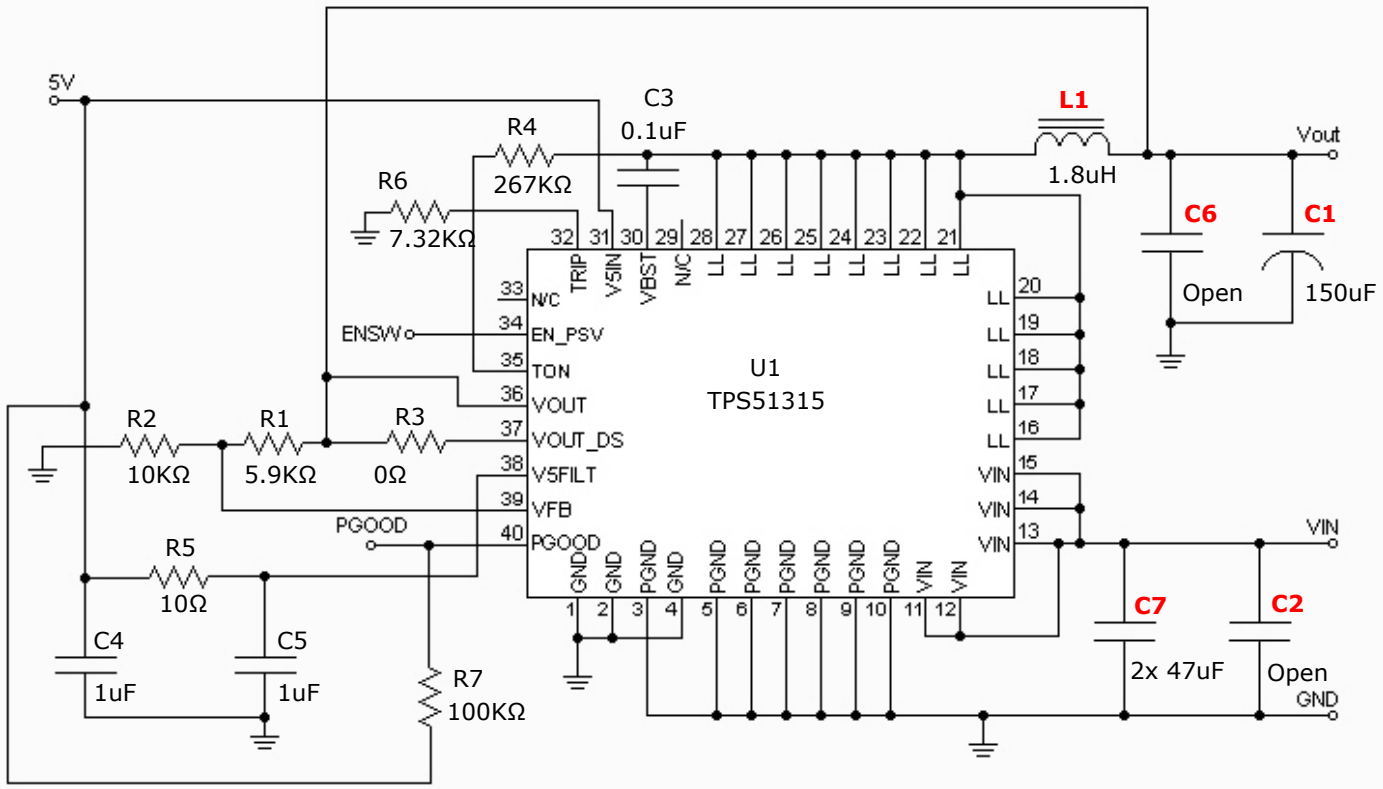
# SwitcherPro Design Report
## Schematic

**Design Name:** TPS51315 5.5-4.5V to 1.2V @ 7.7A. 01/31/2011 14:49 **Part:** TPS51315

**VinMin:** 4.5V **VinMax:** 5.5V **Vout:** 1.2V **Iout:** 7.7A



# SwitcherPro Design Report
## Analysis - Main

**Design Name:** TPS51315 5.5-4.5V to 1.2V @ 7.7A. 01/31/2011 14:49 **Part:** TPS51315

**VinMin:** 4.5V **VinMax:** 5.5V **Vout:** 1.2V **Iout:** 7.7A

| Parameter Units-Symbol | User Input Minimum | User Input Nominal | User Input Maximum | Default Input Minimum | Default Input Nominal | Default Input Maximum | Calculated Minimum | Calculated Nominal | Calculated Maximum |
|---|---|---|---|---|---|---|---|---|---|
| Input Voltage Volts - V | 4.50 | - | 5.50 | - | - | - | - | - | - |
| Input Ripple mVp-p - mVp-p | - | - | - | - | - | 110 | - | - | 88.2 |
| UVLO(Start) Volts - V | - | - | - | - | - | - | - | - | - |
| UVLO(Stop) Volts - V | - | - | - | - | - | - | - | - | - |
| Switching Frequency KHz - KHz | - | - | - | - | 250 | - | - | - | - |
| Slow Start ms - ms | - | - | - | - | 1.06 | - | - | - | - |
| Estimated PCB Area mm² - mm² | - | - | - | - | - | - | - | 531 | - |
| Max Component Height mm - mm | - | - | - | - | - | 25 | - | - | 10 |

# SwitcherPro Design Report
## Analysis - Output1

**Design Name:** TPS51315 5.5-4.5V to 1.2V @ 7.7A. 01/31/2011 14:49 **Part:** TPS51315

**VinMin:** 4.5V **VinMax:** 5.5V **Vout:** 1.2V **Iout:** 7.7A

| Parameter Units-Symbol | User Input Minimum | User Input Nominal | User Input Maximum | Default Input Minimum | Default Input Nominal | Default Input Maximum | Calculated Minimum | Calculated Nominal | Calculated Maximum |
|---|---|---|---|---|---|---|---|---|---|
| Output Voltage Volts - V | - | 1.200 | - | - | - | - | 1.175 | - | 1.214 |
| Output Ripple mVp-p - mVp-p | - | - | - | - | - | 24 | - | - | 59 |
| Output Current Amps - A | - | - | 7.700 | 0.100 | - | - | - | - | - |
| Inductor Peak to Peak Current Amps - A | - | - | - | - | - | - | 2.221 | - | 2.368 |
| Current Limit Threshold Amps - A | - | - | - | - | 11.550 | - | - | - | - |
| Gain Margin dB - dB | -- | - | - | -- | - | - | - | - | - |
| Phase Margin Deg. - Deg. | -- | - | - | -- | - | - | - | - | - |
| Upper FET RDSon mOhms - mΩ | - | - | - | - | - | - | 27 | - | 27 |
| Lower FET RDSon mOhms - mΩ | - | - | - | - | - | - | 5 | - | 5 |
| Duty Cycle % - % | - | - | - | - | - | - | 24.4 | - | 30.0 |
| On Time Min (switch) ns - ns | - | - | - | - | - | - | - | - | - |
| Cross Over Frequency KHz - KHz | - | - | - | - | - | - | - | - | - |

# SwitcherPro Design Report
## Stress Results

**Design Name:** TPS51315 5.5-4.5V to 1.2V @ 7.7A. 01/31/2011 14:49 **Part:** TPS51315

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| Device | Rated Voltage | Calculated Voltage | Rated Current (RMS) | Calculated Current (RMS) | Error Message | Power | Calculated Max Temp |
|---|---|---|---|---|---|---|---|
| C7 (High Freq. Input Cap) | 16V | 5.53V | 4.16A | 1.72A | - | 9mW | - |
| C1 (Bulk Output Cap) | 6.3V | 1.21V | 2.4A | 0.68A | - | 12mW | - |
| L1 (Output Inductor) | - | - | 10.2A | 7.73A | - | 448mW | - |
| U1 (Converter) | 20V | 5.53V | 11A | 7.73A | - | 1W | 60°C |

# SwitcherPro Design Report

## Efficiency

**Design Name:** TPS51315 5.5-4.5V to 1.2V @ 7.7A. 01/31/2011 14:49 **Part:** TPS51315

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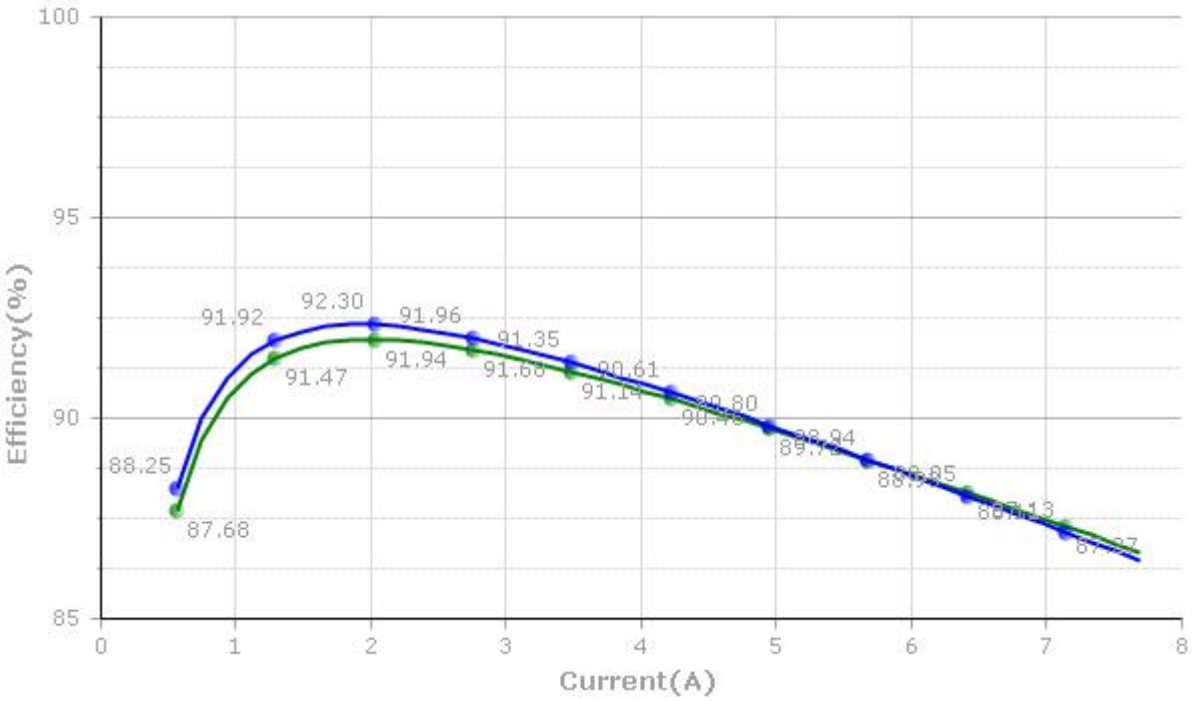


Efficiency For Vin Max
Efficiency For Vin Min

# SwitcherPro Design Report
## Bill of Materials

**Design Name:** TPS51315 5.5-4.5V to 1.2V @ 7.7A. 01/31/2011 14:49 **Part:** TPS51315

**VinMin:** 4.5V **VinMax:** 5.5V **Vout:** 1.2V **Iout:** 7.7A

| Name | Quantity | Part Number | Description | Manufacturer | Package | Area(mm²) | Height(mm) |
|---|---|---|---|---|---|---|---|
| C1 | 1 | 6TPE150MPC | Capacitor, POSCAP, 150uF, 6.3V, 20% | Sanyo | TPE-C3 | 19 | 2 |
| C3 | 1 | Standard | Capacitor, Ceramic, 0.1uF, 20V, 10% | Standard | 0805 | 3 | 1 |
| C4 | 1 | Standard | Capacitor, Ceramic, 1uF, 20V, 10% | Standard | 0805 | 3 | 1 |
| C5 | 1 | Standard | Capacitor, Ceramic, 1uF, 20V, 10% | Standard | 0805 | 3 | 1 |
| C7 | 2 | C5750X5R1C476M | Capacitor, Ceramic, 47uF, 16V, 20% | TDK | C5750 2220 | 31 | 2 |
| L1 | 1 | SRR1210-1R8Y | Inductor, 1.8uH, 10.2A, 7.5mΩ | Bourns | SRR1210 | 144 | 10 |
| R1 | 1 | Standard | Resistor, SurfaceMount, 5.9KΩ, 100mW, 1% | Standard | 0603 | 2 | 1 |
| R2 | 1 | Standard | Resistor, SurfaceMount, 10KΩ, 100mW, 1% | Standard | 0603 | 2 | 1 |
| R4 | 1 | Standard | Resistor, SurfaceMount, 267KΩ, 100mW, 1% | Standard | 0603 | 2 | 1 |
| R5 | 1 | Standard | Resistor, SurfaceMount, 10Ω, 100mW, 5% | Standard | 0603 | 2 | 1 |
| R6 | 1 | Standard | Resistor, SurfaceMount, 7.32KΩ, 100mW, 1% | Standard | 0603 | 2 | 1 |
| R7 | 1 | Standard | Resistor, SurfaceMount, 100KΩ, 100mW, 5% | Standard | 0603 | 2 | 1 |
| U1 | 1 | TPS51315 | IC, Converter, 40 pins | Texas Instruments, Inc. | VQFN(RGF) | 37 | 1 |

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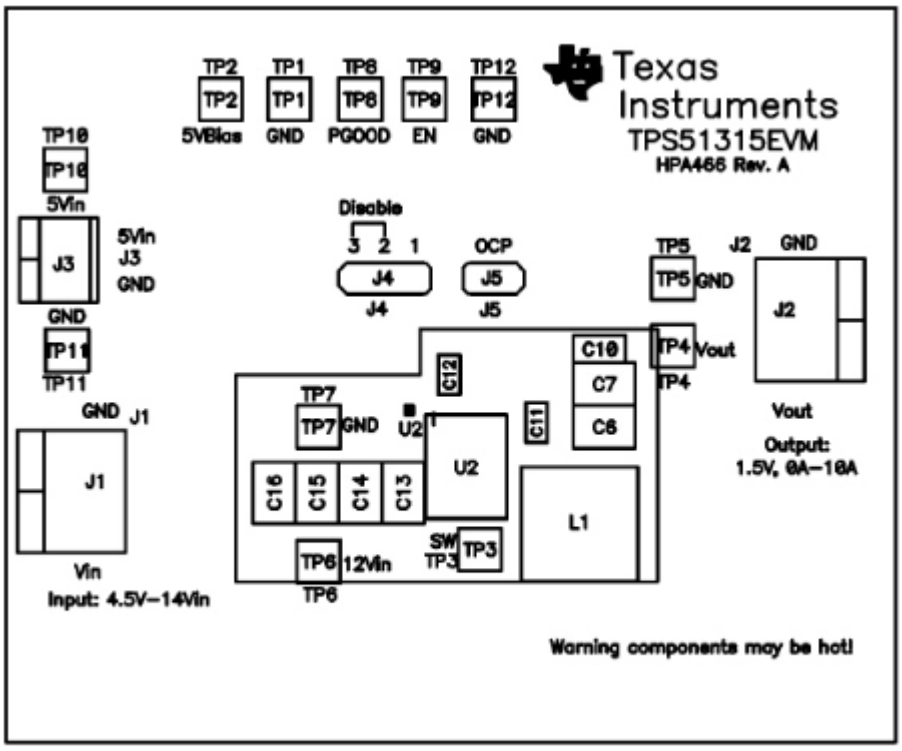


Figure 14. Top Layer Assembly Drawing (Top View)

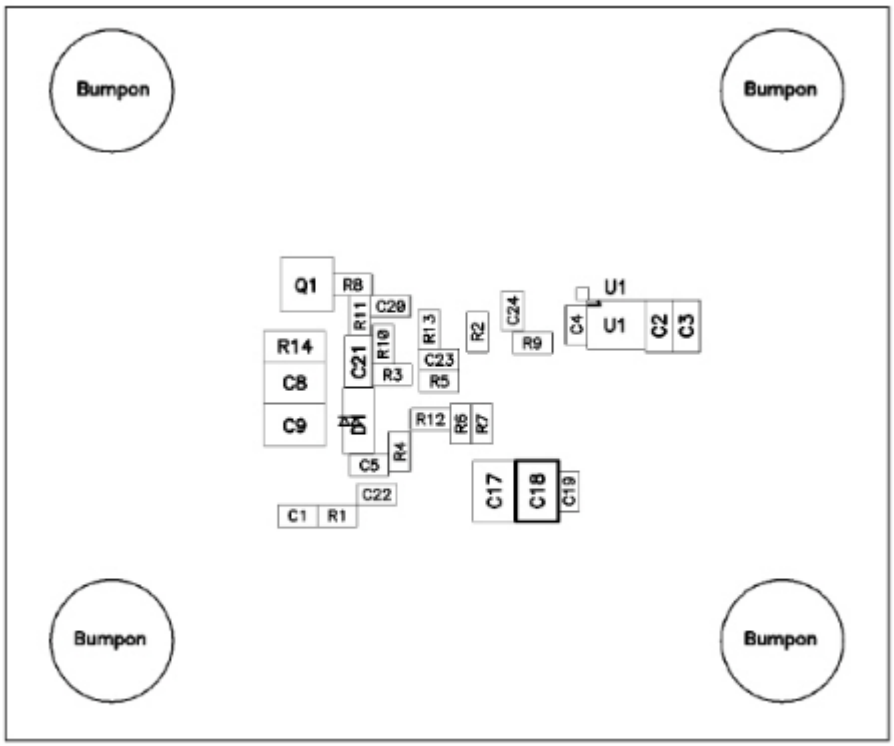


Figure 15. Bottom Assembly Drawing (Bottom View)

TPS51315
Certain concepts must be considered before starting printed curcuit board (PCB) layout work using the TPS51315.
Connect the R-C low-pass filter from the 5-V supply to the V5FILT pin. A filter resistance of 10 O and a filter capacitance of 1 mF is recommended. Place the filter capacitor close to the device, within 12 mm (0.5 inches) if possible.
Connect the overcurrent setting resistors from TRIP to GND close to the device if possible. The trace from TRIP to the resistor and from the resistor to GND should avoid coupling to a high-voltage switching node.The discharge path (VOUT_DS) should have a dedicated trace to the output capacitor(s); separate from the output voltage sensing trace, and use a 1,5 mm (60 mils) or wider trace with no loops. Make sure the feedback current setting resistor (the resistor between VFB to GND) is tied close to the device GND. The trace from this resistor to the VFB pin should be short and narrow. Place the trace on the component side and avoid vias between this resistor and the device.All sensitive analog traces and components such as VOUT, VFB, GND, EN_PSV, PGOOD, TRIP, V5FILT, and TON should be placed away from high-voltage switching nodes such as LL or VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback traces from power traces and components.Gather the ground terminals of the VIN capacitor(s), VOUT capacitor(s), and the PGND as close as possible. GND (signal ground) and PGND (power ground) should be connected strongly together near the device. The PCB trace defined as LL node, which connects to the source of the upper MOSFET, the drain of the lower MOSFET, and the high-voltage side of the inductor, should be as short and wide as possible.