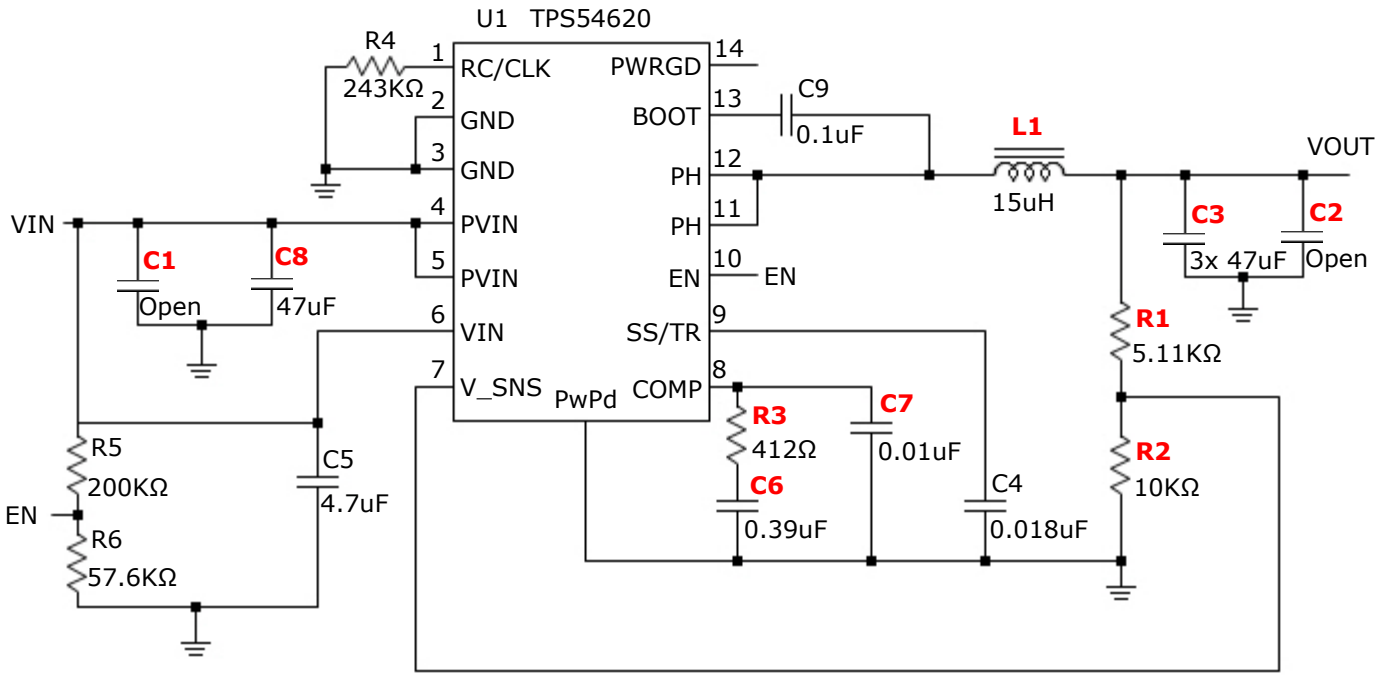
SwitcherPro Design Report
Schematic

Design Name: Squire 1V2 Impl **Part:** TPS54620

VinMin: 5V **VinMax:** 5V **Vout:** 1.2V **Iout:** 1.5A



SwitcherPro Design Report
Analysis - Main

Design Name: Squire 1V2 Impl **Part:** TPS54620

VinMin: 5V **VinMax:** 5V **Vout:** 1.2V **Iout:** 1.5A

Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Input Voltage Volts - V	5.00	-	5.00	-	-	-	-	-	-
Input Ripple mVp-p - mVp-p	-	-	-	-	-	100	-	-	49.9
UVLO(Start) Volts - V	-	-	-	-	-	-	-	5.00	-
UVLO(Stop) Volts - V	-	-	-	-	-	-	-	4.50	-
Switching Frequency KHz - KHz	-	200	-	-	-	-	180	200	220
Slow Start ms - ms	-	-	-	-	6.00	-	-	-	-
Estimated PCB Area mm² - mm²	-	-	-	-	-	-	-	396	-
Max Component Height mm - mm	-	-	-	-	-	25	-	-	6

SwitcherPro Design Report
Analysis - Output1

Design Name: Squire 1V2 Impl **Part:** TPS54620

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Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Output Voltage Volts - V	-	1.200	-	-	-	-	1.189	-	1.229
Output Ripple mVp-p - mVp-p	-	-	20	-	-	24	-	-	1.9
Output Current Amps - A	-	-	1.500	0.100	-	-	-	-	-
Inductor Peak to Peak Current Amps - A	-	-	-	-	-	-	0.351	-	0.351
Current Limit Threshold Amps - A	-	-	-	-	10.000	-	-	-	-
Gain Margin dB - dB	-	-	-	-10	-	-	-	-18	-
Phase Margin Deg. - Deg.	-	-	-	60	-	-	-	64	-
Upper FET RDSon mOhms - mΩ	-	-	-	-	-	-	25	-	25
Lower FET RDSon mOhms - mΩ	-	-	-	-	-	-	19	-	19
Duty Cycle % - %	-	-	-	-	-	-	25.4	-	25.4
On Time Min (switch) ns - ns	-	-	-	-	-	-	1153.0	-	1409.2
Cross Over Frequency KHz - KHz	-	-	-	-	-	-	-	5	-

SwitcherPro Design Report
Stress Results

Design Name: Squire 1V2 Impl **Part:** TPS54620

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Device	Rated Voltage	Calculated Voltage	Rated Current (RMS)	Calculated Current (RMS)	Error Message	Power	Calculated Max Temp
C8 (High Freq. Input Cap)	10V	5.03V	3.5A	0.65A	-	1mW	-
C3 (Bulk Output Cap)	10V	1.2V	3.5A	34mA	-	10uW	-
L1 (Output Inductor)	-	-	3.75A	1.5A	-	57mW	-
U1 (Converter)	20V	5.03V	11A	1.5A	-	89mW	28°C

SwitcherPro Design Report

Efficiency

Design Name: Squire 1V2 Impl **Part:** TPS54620

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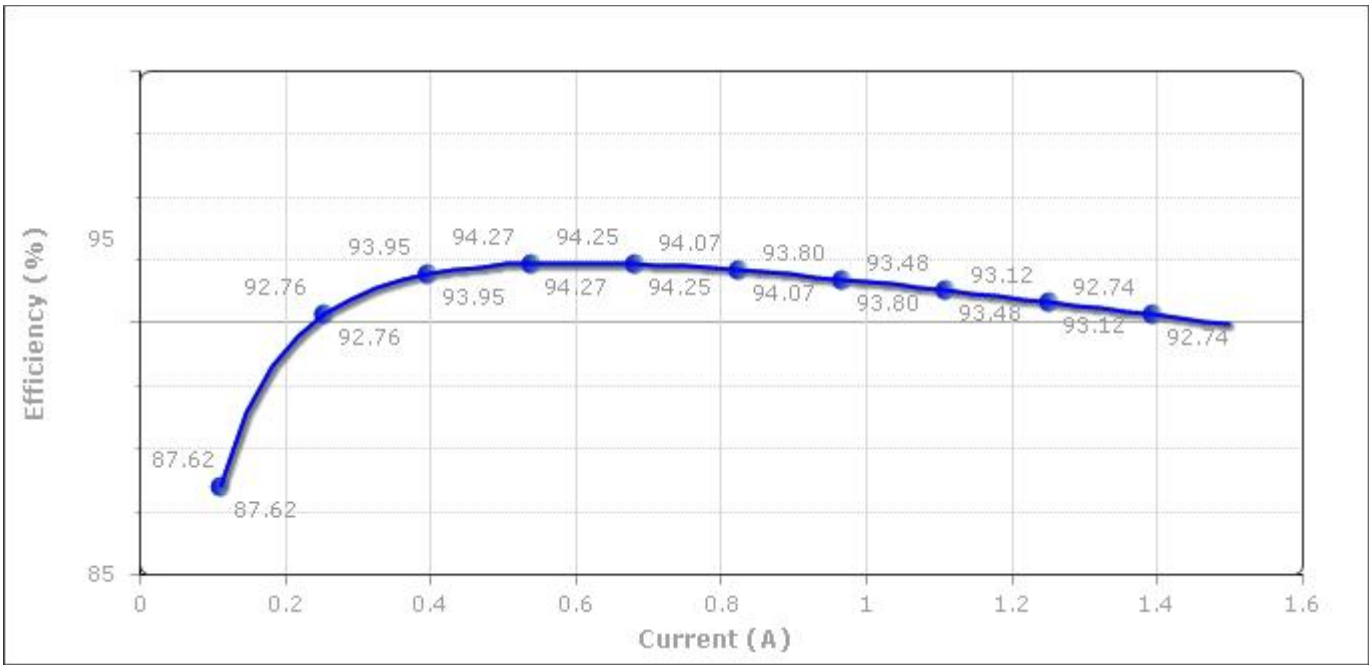
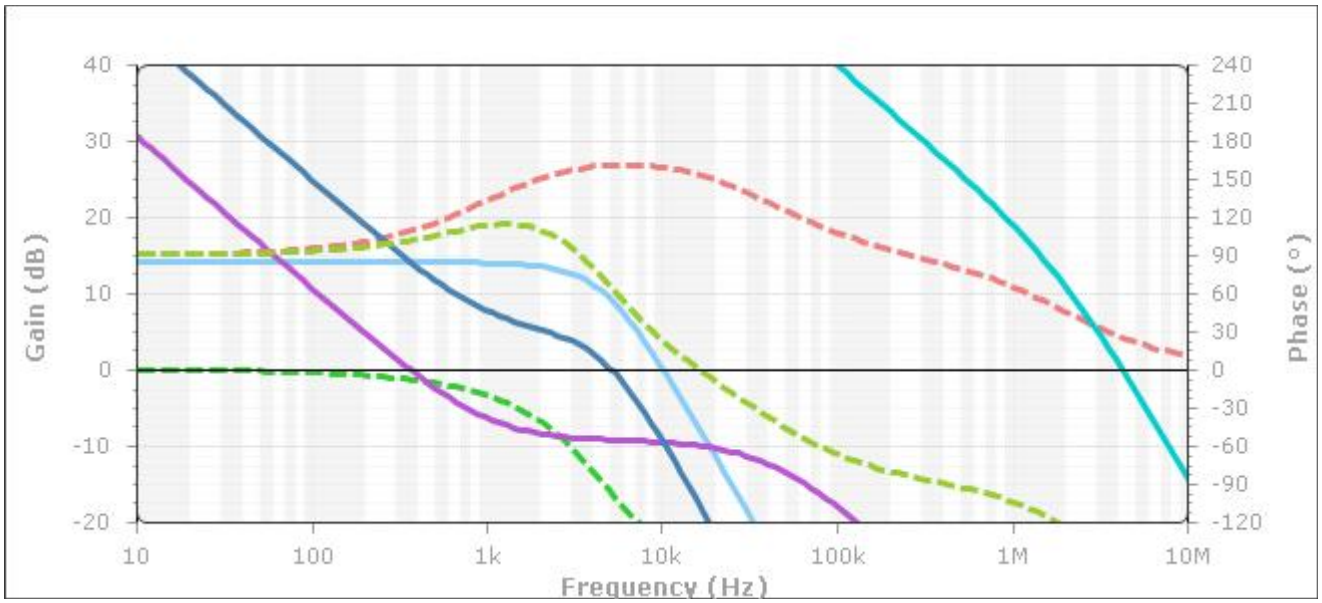


Efficiency For Vin Max
Efficiency For Vin Min

SwitcherPro Design Report
Loop Response

Design Name: Squire 1V2 Impl **Part:** TPS54620

VinMin: 5V **VinMax:** 5V **Vout:** 1.2V **Iout:** 1.5A



- Power Stage Gain
- Power Stage Phase
- Compensation Gain
- Compensation Phase
- Error Amp Gain
- Total Gain
- Total Phase

SwitcherPro Design Report
Bill of Materials

Design Name: Squire 1V2 Impl **Part:** TPS54620

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Name	Quantity	Part Number	Description	Manufacturer	Package	Area(mm²)	Height(mm)
C3	3	GRM32ER71A476KE15L	Capacitor, Ceramic, 47uF, 10V, 10%	MURATA	1210	8	2
C4	1	Standard	Capacitor, Ceramic, 0.018uF, 10V, 20%	Standard	0603	2	1
C5	1	Standard	Capacitor, Ceramic, 4.7uF, 10V, 10%	Standard	0603	2	1
C6	1	Standard	Capacitor, Ceramic, 0.39uF, 4V, 20%	Standard	0603	2	1
C7	1	Standard	Capacitor, Ceramic, 0.01uF, 4V, 20%	Standard	0603	2	1
C8	1	GRM32ER71A476KE15L	Capacitor, Ceramic, 47uF, 10V, 10%	MURATA	1210	8	2
C9	1	Standard	Capacitor, Ceramic, 0.1uF, 4V, 10%	Standard	0603	2	1
L1	1	744771115	Inductor, 15uH, 3.75A, 25mΩ	wurth	inductor 12x12	144	6
R1	1	Standard	Resistor, SurfaceMount, 5.11KΩ, 100mW, 1%	Standard	0603	2	1
R2	1	Standard	Resistor, SurfaceMount, 10KΩ, 100mW, 1%	Standard	0603	2	1
R3	1	Standard	Resistor, SurfaceMount, 412Ω, 100mW, 1%	Standard	0603	2	1
R4	1	Standard	Resistor, SurfaceMount, 243KΩ, 100mW, 1%	Standard	0603	2	1
R5	1	Standard	Resistor, SurfaceMount, 200KΩ, 100mW, 1%	Standard	0603	2	1
R6	1	Standard	Resistor, SurfaceMount, 57.6KΩ, 100mW, 1%	Standard	0603	2	1
U1	1	TPS54620	IC, Converter, 14 pins	Texas Instruments, Inc.	QFN-Power PAD	13	1

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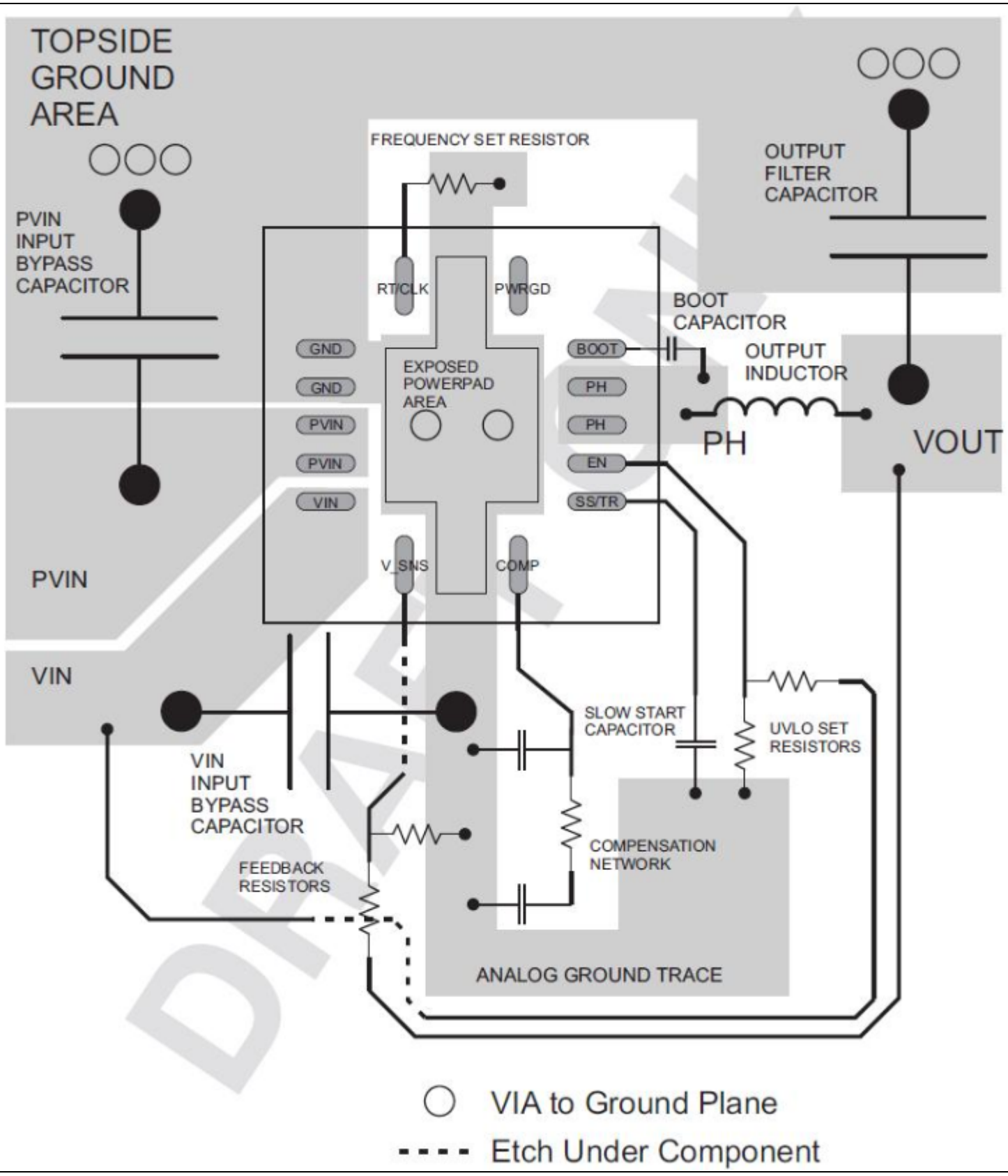

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TPS54620

Layout is a critical portion of good power supply design.The top layer contains the main power traces for VIN, VOUT, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54620 and a large top side area filled with ground. The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter cpacitor and directly under the TPS54620 device to provide a thermal path from the PowerPAD land to ground. The GND pin should be tied directly to the power pad under the IC and the power pad. For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections. The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric. Make sure to connect this capacitor to the quite analog ground trace rather than the power ground trace of the PVIn bypass capacitor. Since the PH connection is the switching node, the output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components should be grounded to the analog ground path as shown. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.