

## LM96080 - Enhanced Version of the LM80


The LM96080 is an enhanced version of the LM80. It is pin and software compatible with the LM80. The design of the LM96080 is based on our newest high volume production hardware monitor on an advanced process incorporating 10 years of learning since the LM80 design.

Summary of enhancements:

<b>LM96080</b>	<b>LM80</b>
<b>10-Bit</b> ADC for Analog Inputs	8-Bit ADC for Analog Inputs
<b>Noise-Immune</b> Bus Inputs & SMBus type of Timeout	Schmitt-Triggered Bus Inputs
<b>Improved Access of data</b> – completes conversion during bus access (write or read)	Aborts conversion during bus access (write or read)
<b>Pin and software compatible to LM80 in TSSOP-24</b>	TSSOP-24
<b>ESD: 2kV HBM / 200V MM / 1000V CDM (find out standard)</b>	ESD: 2kV HBM / 125V MM

### 10-Bit ADC for Analog Inputs

The delta-sigma ADC resolution for voltage measurement has been expanded to 10-bits. The register locations for the voltage readings are in the same locations as in the LM80 and are supported by double-byte reads. The extended resolution of the temperature reading is available as in the LM80 but additionally it is available as a double byte read at location 27h.



<b>Address A7-A0</b>	<b>Description</b>
20h	IN0 reading (10-bit)
21h	IN1 reading (10-bit)
22h	IN2 reading (10-bit)
23h	IN3 reading (10-bit)
24h	IN4 reading (10-bit)
25h	IN5 reading (10-bit)
26h	IN6 reading (10-bit)
27h	Temperature reading (9-bit or 12-bit for easy read-back)

**Figure 1 LM96080 Voltage and Temperature Readings**

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The following table details out the voltage monitoring data format for 8-bit access and 10-bit access. The 8-bit access is identical to the LM80:

LM80 and LM96080 IN0-IN6																
Format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0								
8-bit	128	64	32	16	8	4	2	1								
Weight	1.28V	0.64V	0.32V	0.16V	80mV	40mV	20mV	10mV								
LM96080 Only IN0-IN6																
Format	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16-bit	512	256	128	64	32	16	8	4	2	1	0	0	0	0	0	0
Weight	1.28V	0.64V	0.32V	0.16V	80mV	40mV	20mV	10mV	5mV	2.5mV	0	0	0	0	0	0

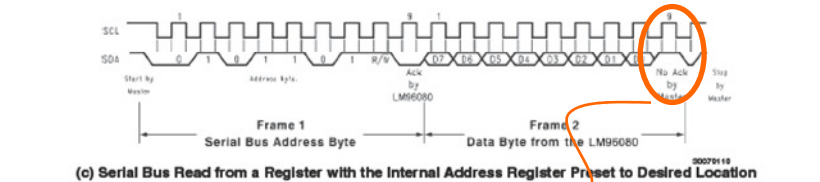
The following table describes the data format for temperature monitoring for 8-bit single byte access and 9-bit or 12-bit double byte access:

LM80 and LM96080 8-bit Temperature																
Format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0								
8-bit	128	64	32	16	8	4	2	1								
Weight	SIGN	64°	32°	16°	8°	4°	2°	1°								
LM96080 9-bit Temperature																
Format	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16-bit	256	128	64	32	16	8	4	2	1	0	0	0	0	0	0	0
Weight	SIGN	64°	32°	16°	8°	4°	2°	1°	0.5°	0	0	0	0	0	0	0
LM96080 12-Bit Temperature																
Format	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16-bit	4096	1024	512	256	128	64	32	16	8	4	2	1	0	0	0	0
Weight	SIGN	64°	32°	16°	8°	4°	2°	1°	1/2°	1/4°	1/8°	1/16°	0	0	0	0

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Double byte access has been implemented in the LM96080 and the following timing diagrams detail the differences between single byte and double byte. In the case for a single-byte read with the internal register address pointer preset there is a NoACK by the master after the first byte, as described in Figure 2. The NoACK signals to the LM96080 that the communication is over and that a stop will follow. In the case for a double-byte read where the second byte will be transmitted the master will drive an ACK. At the end of the second byte the master will NoACK to signal that the communication is over and that a stop will follow.

**Supported by  
LM80 and  
LM96080**



**Supported by  
LM96080  
only**

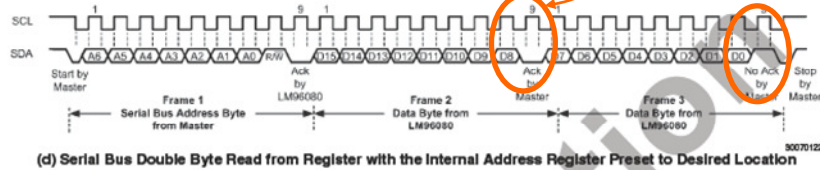
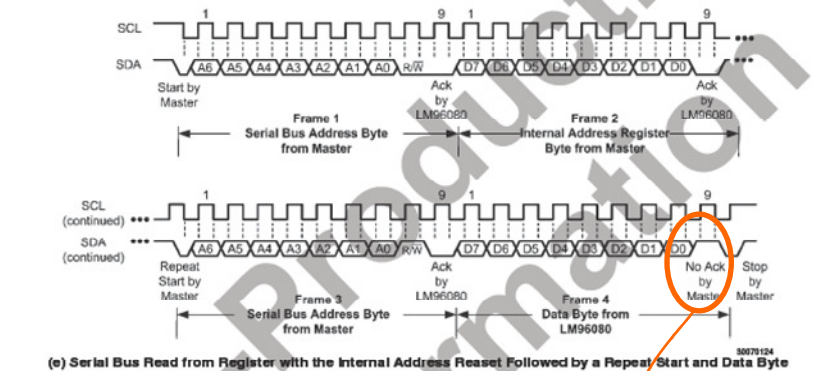


Figure 2 Single or Double Byte Data Access with Preset Internal Address

In the case of a repeat start a similar change in the protocol is followed as described in Figure 3.

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LM80 and  
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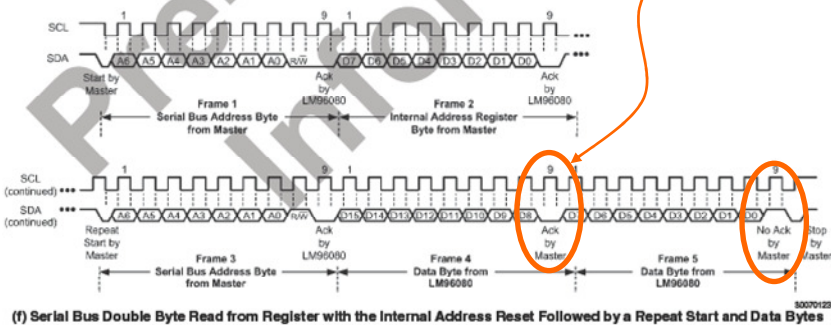
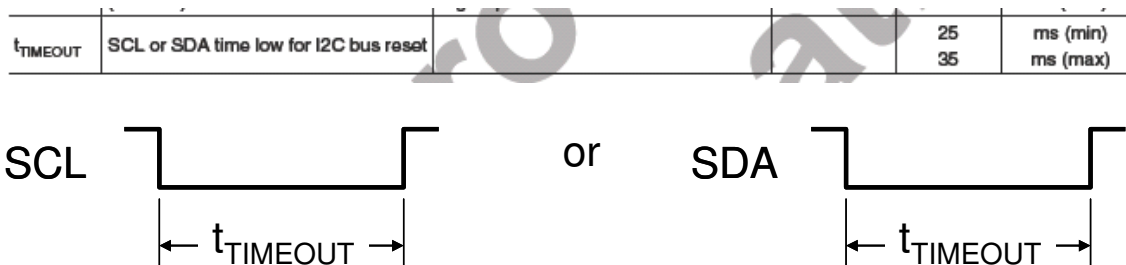


Figure 3 Single or Double Byte Read followed by a Repeat Start

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### I2C Bus Enhancements

The LM96080 has improved Hysteresis and filtering added to the clock input. In addition TIMEOUT is supported by the LM96080 in order to simplify return to full operation in the case of a soft reset. If the soft reset were to occur while the LM96080 is transmitting a LOW on the data line the bus would “hang” until enough clock are supplied to the device to release it. TIMEOUT simplifies this in that if the SCL or SDA are held LOW for more than 35ms (see Figure 4) the I2C state-machine inside the LM96080 resets and readies itself for a new communication. In order to support the TIMEOUT function the shutdown current of the LM96080 (300µA) is



**Figure 4 SMBus like TIMEOUT**

greater than the shutdown current of the LM80 (15µA).

The LM96080 also includes improved access of data. The LM80 will abort the current conversion when a communication is initiated on the bus and it recognizes its device address. This is not the case for the LM96080 since its register data can be accessed at any time without any need to wait for a round robin cycle or an individual channel to complete a communication.

### Software Compatibility and Enhancements

The LM96080 is software compatible with the LM80. The LM96080 has four new registers for improved performance yet still maintains backwards compatibility:

1. Conversion Rate Register – allows faster system data update
2. Manufacturers ID and Stepping/Die Revision Code Registers – allows discriminating between the LM80 and LM96080
3. Channel Disable Register – disabling unused inputs allows faster system data update of used channels since unused channel conversions are skipped

The new registers are assigned to addresses that were marked reserved in the LM80 as shown in Figure 5.

Register	LM96080 Internal Hex Address (This is the data to be written to the Address Register)	Power on Value	Notes
Configuration Register	00h	0000 1000	
Interrupt Status Register 1	01h	0000 0000	
Interrupt Status Register 2	02h	0000 0000	
Interrupt Mask Register 1	03h	0000 0000	
Interrupt Mask Register 2	04h	0000 0000	
Fan Divisor/RST_OUT/OS Register	05h	0001 0100	FAN1 and FAN2 divisor = 2 (count of 153 = 4400 RPM)
OS/ Configuration and Temperature Resolution Register	06h	0000 0001	
<b>New</b> Conversion Rate Register	07h	0000 0000	
<b>New</b> Channel Disable Register	08h	0000 0000	Allows voltage monitoring inputs to be disabled.
Value RAM	20h-3Dh		
Value RAM	3Eh	0000 0001	Manufacturer's ID
Value RAM	3Fh	0000 1000	Stepping/Die Revision Code

**Figure 5 LM96080 New Registers**

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The **Conversion Rate register** resides at address 07h. The power on default value is 0000 0000 and sets the LM96080 round-robin conversion rate to 728ms. The LM80 round-robin conversion rate is 1sec for 9-bit temperature conversions. Bit 0 of this register controls the conversion rate as described in Figure 6.

Bit	Name	Read/Write	Description
0	CR1	Read/Write	Controls conversion rate: 0=728ms (typical) 1= continuous conversion (approximately 73 ms typical, dependent on fan tach input frequency) Note: — Each voltage channel conversion takes 3ms typical — Temperature conversion takes 12ms typical for 9-bit resolution and 96ms typical for 12-bit resolution — Each fan tach input is monitored for 2 pulses, the time interval for two pulses is added to the round robin time for each fan tach input that is enabled.
1-7	Reserved	Read only	Reserved — will always report zero.

Figure 6 Conversion Rate register

The **Channel Disable register** resides at address 08h. Its power on default value is 0000 0000 or all channels enabled. Figure 7 describes the function of the bits in this register.

Bit	Name	Read/Write	Description
0	IN0	Read/Write	When set to '1', IN0: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
1	IN1	Read/Write	When set to '1', IN1: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
2	IN2	Read/Write	When set to '1', IN2: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
3	IN3	Read/Write	When set to '1', IN3: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
4	IN4	Read/Write	When set to '1', IN4: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
5	IN5	Read/Write	When set to '1', IN5: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
6	IN6	Read/Write	When set to '1', IN6: conversions are skipped and disabled value register reading will be 0 error events will be suppressed
7	Temp	Read/Write	When set to '1', Temperature: conversions are skipped and disabled value register readings will be 0 error events will be suppressed

Figure 7 Channel Disable register

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The last two registers, **Manufacturer's ID and Stepping/Die Revision Code registers** are used to identify an LM96080 via software. They are at addresses 3Eh and 3Fh and power up with values 0000 0001 and 0000 1000, respectively. The LM80 powers up with random values at these register addresses, so there is nothing to guarantee that the values of the LM80's registers do not power up with the LM96080 default values. Since these registers are writable a sequence can be followed in order to ensure that the device can be identified as an LM96080. First write a value to these registers other than the default as described in Figure 8. Then set the INITIALIZATION bit in the Configuration register. In the LM96080 this will reset the values of these registers to the default value while in the LM80 it has no effect on these registers.

3Eh	Manufacturer's ID always defaults to 0000 0001; this register is writable and can be reset to the default value by the INITIALIZATION bit in the Configuration Register.
3Fh	Stepping/Die Revision code always defaults to 0000 1000; this register is writable and can be reset to the default value by the INITIALIZATION bit in the Configuration Register.

Figure 8 Manufacturer's ID and Stepping/Die Revision Code Registers

### Power Supply Voltage Range and ESD

- The LM96080 is on a newer smaller geometry process that has a lower breakdown voltage than for the process used for the LM80. Therefore, the absolute maximum ratings are different. The absolute maximum rating of the LM80 is 6.5V, while the LM96080 is 6.0V.
- The LM80-3 and LM80-5 have wider power supply tolerance. The LM96080 was released as only one device that covers both power supply voltage ranges (no dash options for the LM96080) with a single power supply range of +3.0V to +5.5V.
- Power dissipation comparison:  
Note, the shutdown power supply current for the LM96080 is greater than LM80 because the LM96080 supports TIMEOUT which requires the internal clock to run continuously during shutdown.

	LM80	LM96080
Shutdown	0.015 mA (typ)	0.33 mA (typ)
Operating (average)	0.2 mA (typ)	0.37 mA (typ)

#### ■ ESD

The LM96080 will at minimum meet National's newest ESD standards of:

- Human Body Model = 3000V
- Machine Model = 300V
- CDM = 1000V

The LM80 met:

- Human Body Model = 2000V
- Machine Model = 125V
- No rating for CDM