User Guide
ADS5263 EVM with TSW1250
LCLK Phase Programmability

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ADS5263 – LCLK Phase Programmability

In the ADS5263, the phase of the output bit clock LCLK can be programmed as shown in adjacent figure.

This is controlled using register bits PHASE_DDR<1:0>.
The default value of PHASE_DDR = 10.

The TSW1250 capture code works ***only*** with PHASE_DDR<1:0> = 00.

So, when using the TSW1250, the PHASE_DDR bits must be set to 00.

Next slide shows how this can be done using the ADS5263 GUI

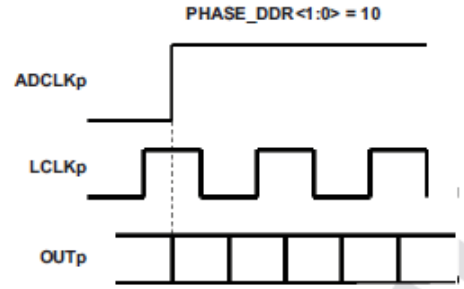

Figure 42. Default Phase of LCLK

The phase of LCLK can be programmed relative to the output frame clock and data using bits PHASE_DDR<1:0>. The LCLK phase modes are shown in Figure 43.

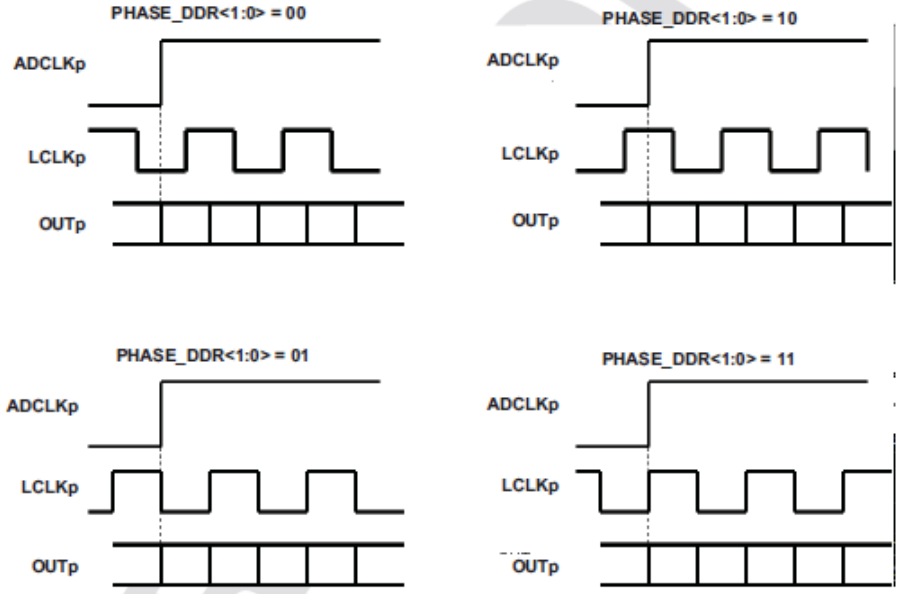

Figure 43. Phase Programmability Modes for LCLK