



# User Guide

## ADS5263 EVM with TSW1250

### LCLK Phase Programmability

Oct-2011  
v1.0



## ADS5263 – LCLK Phase Programmability

In the ADS5263, the phase of the output bit clock LCLK can be programmed as shown in adjacent figure.

This is controlled using register bits PHASE\_DDR<1:0>.

The default value of PHASE\_DDR = 10.

**The TSW1250 capture code works *only* with PHASE\_DDR<1:0> = 00.**

So, when using the TSW1250, the PHASE\_DDR bits must be set to 00.

**Next slide shows how this can be done using the ADS5263 GUI**

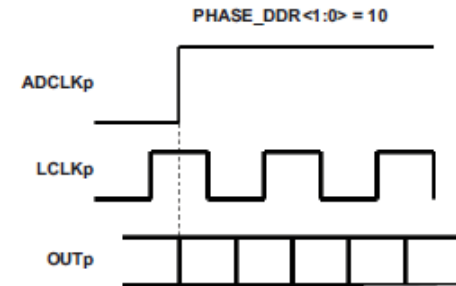


Figure 42. Default Phase of LCLK

The phase of LCLK can be programmed relative to the output frame clock and data using bits PHASE\_DDR<1:0>. The LCLK phase modes are shown in Figure 43.

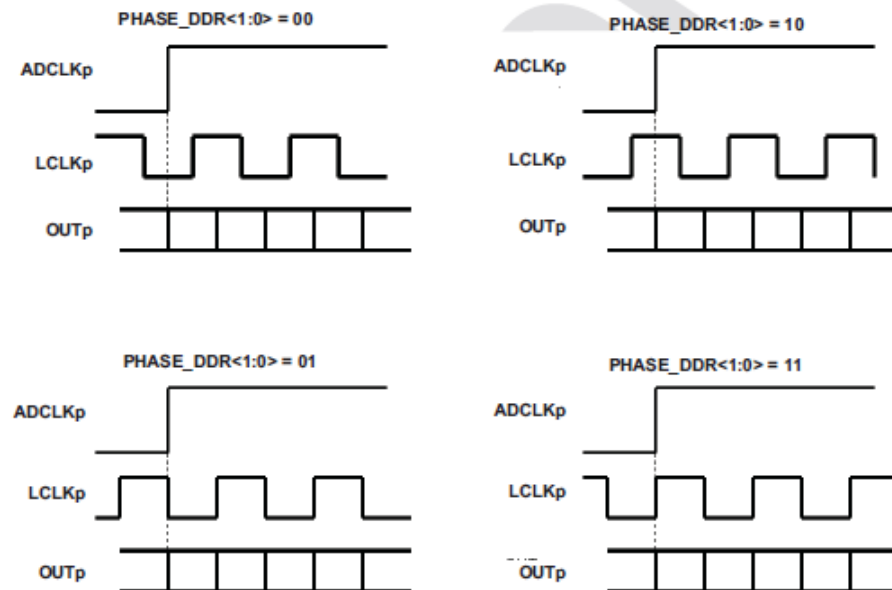
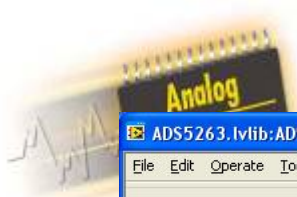


Figure 43. Phase Programmability Modes for LCLK



ADS5263.lvlib:ADS5263.vi

File Edit Operate Tools Window Help

TEXAS INSTRUMENTS

# ADS 5263 GUI

Read Me

AD55263 Features

SAVE COMMAND SEQUENCE

COMMAND SEQUENCE PLAY BACK

Top Level/Pin Ctl Interface/Test Pattern Dig Sig Proc Dig Sig Proc FILTER I/O Mapping **Debug**

**Custom Write Register**

Write Address: x 42

Write Data: x 8000

Write Custom Register

**Custom Read Register**

Read Address: x 0

Read Data: x 0

Read Custom Register

Use the "Debug" tab. In the Custom Write register, set Write Address = 0x42 Write Data = 0x8000

address: x 46 Data: x 0 Last Data: x 8

**Digital Waveform Graph - Write**

SCLK - [Square Wave]

SDATA - [0 0 1 0]

SEN - [0]

Error Out

status code: [Green Checkmark] 00

source

Version 2.0 - 5/10/2010 Build date - 05/09/2011 10/4/2011 3:14:36 PM READY