The kit should be connected to a network to verify that the LEDs toggle according to the connection and data traffic. The LED1 output is driven active whenever a valid link is detected, and blinks whenever the link is transmitting or receiving data. The LED2 output is driven active when the operating speed is 100Mbit/s; LED2 will go inactive when the operating speed is 10Mbit/s or during line isolation.

Test-035: RMII Ethernet Outputs

Description	Criteria	Notes	Result
		No changes. No testing required	Not Tested

4.6.2.4 Network Test

Connect the kit to a network and obtain an IP address. Transfer several files over Ethernet to ensure proper operation.

Test-037: RMII Network Test

Description	Criteria	Notes	Result
		No changes. No testing required	Not Tested

4.6.2.5 Throughput Test

Ethernet through-put should be recorded. Large files should be transferred over Ethernet and the transfer rate should be recorded for several iterations.

Test-038: RMII Throughput Test

Description	Criteria	Notes	Result
		No changes. No testing required	Not Tested

4.7 USB

The following tests do not constitute USB compliance testing. Compliance testing is the responsibility of the end user. This test is intended to verify correct design and performance of an engineering development kit only.

For Low and Full speed testing, use an Eye Pattern Diagram comparison. Using a Tektronix TDS 754C scope or comparable with Tektronix P6243 voltage probes, use the following setup:

Connect CH1 -> D-

Connect CH2 -> D+

Set CH1 to 500mV/div, set CH2 to 500mV/div

Set horizontal scale to 25nS/div

Set the trigger to 1.50V, mode to Normal

Set Horizontal Menu -> trigger position = 32%

Set Display -> Persistence = infinite

Set Zoom to on, CH1/CH2 to 500mV/div, Horizontal scale to 12.5nS/div

Set Cursors -> paired, Time Unit -> seconds

With active probes applied at the connector, perform an “eye-test” and record the scope shot at the end of each section for comparison.

4.7.1 OTG Port

The PHY for this port is located on the processor. The port should be tested by connecting to a device and performing data reads and writes. This port should be tested in host mode as well as device mode.

Test-039: USB OTG Port

Description	Criteria	Notes	Result
		Ran USB test in CCSv4.1.1. It found the host machine. Also transferred files from RAM disk to USB flash disk and back. Used the U-boot and linux kernel provided as part of DaVinci-PSP-SDK-03.20.00.11	PASS

4.7.1.1 Host Mode

4.7.1.1.1 Low Speed

Signal Name	Measured at pin # of device	Rise Time (ns)				Fall Time (ns)				Jitter (for single transition) (nS)			
		Min	Meas.	Max	Fig	Min	Meas.	Max	Fig	Min	Meas.	Max	Fig
D+	J6.3												
D-	J6.2												

Table 13 - OTG Port, Host Mode: Low Speed Rise, Fall, Jitter

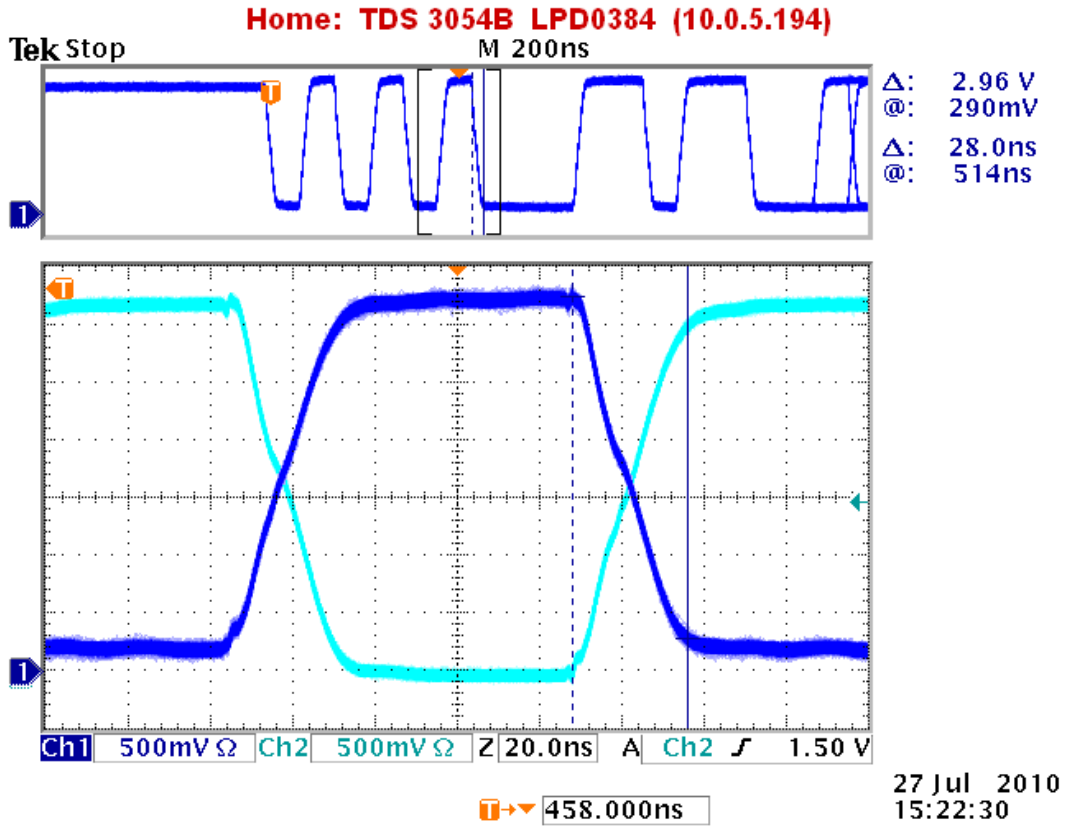
Test-057: OTG Port, Host Mode: Low Speed Rise, Fall, Jitter

Description	Criteria	Notes	Result
	Measurements (see table above) are within acceptable limits.	Could not find a slow speed device suitable for testing. Assume that if the higher speeds are good the low speeds will also work.	Not Tested

4.7.1.1.2 Full Speed

Signal Name	Measured at pin # of device	Rise Time (ns)				Fall Time (ns)				Jitter (for single transition) (nS)			
		Min	Meas.	Max	Fig	Min	Meas.	Max	Fig	Min	Meas.	Max	Fig
D+	J6.3	4	20.8	20		4	22.8	20		-3.5	2	+3.5	
D-	J6.2	4	22.4	20		4	24.4	20		-3.5	1.2	+3.5	

Table 14 - OTG Port, Host Mode: Full Speed Rise, Fall, Jitter



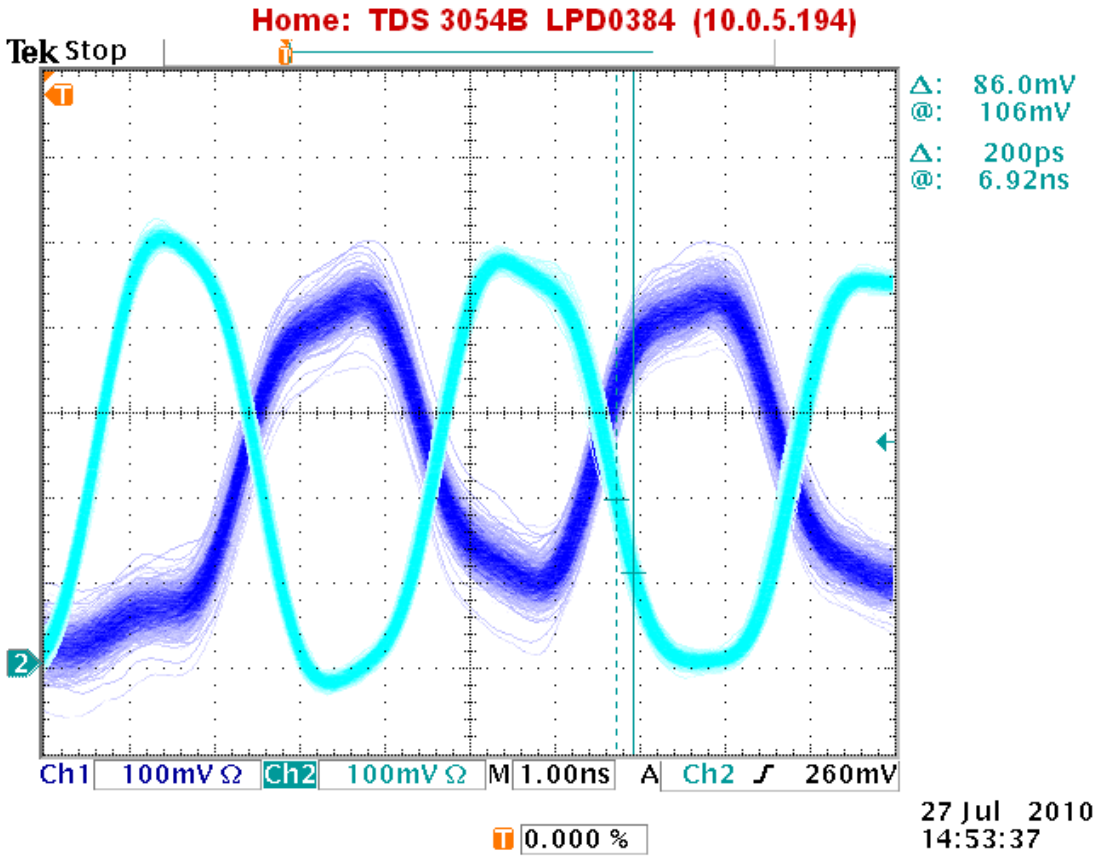
Full Speed Eye Diagram

Test-058: OTG Port, Host Mode: Full Speed Rise, Fall, Jitter

Description	Criteria	Notes	Result
	Measurements (see table above) are within acceptable limits.	Rise-times a little out of spec. But the USB spec is based around a 50pf load and allows a downstream facing transceiver to have a load up to 150pf. So some margin beyond the 20ps should be allowed. In addition the eye diagram is really clean.	PASS

4.7.1.1.3 High Speed

Signal Name	Measured at pin # of device	Rise Time (ns)				Fall Time (ns)				Jitter (for single transition) (nS)			
		Min	Meas.	Max	Fig	Min	Meas.	Max	Fig	Min	Meas.	Max	Fig
D+	J6.3		0.62				0.72				0.34		
D-	J6.2		0.82				0.74				0.2		



Eye diagram for high speed.

Description	Criteria	Notes	Result
	Measurements (see table above) are within acceptable limits.		PASS

4.7.1.2 Device Mode

4.7.1.2.1 Low Speed

Signal Name	Measured at pin # of device	Rise Time (ns)				Fall Time (ns)				Jitter (for single transition) (nS)			
		Min	Meas.	Max	Fig	Min	Meas.	Max	Fig	Min	Meas.	Max	Fig
D+	J6.3												
D-	J6.2												

Table 15 - OTG Port, Device Mode: Low Speed Rise, Fall, Jitter

Test-059: OTG Port, Device Mode: Low Speed Rise, Fall, Jitter

Description	Criteria	Notes	Result
	Measurements (see table above) are within acceptable limits.	Could not find a slow speed device suitable for testing.	Not Tested

		Assume that if the higher speeds are good the low speeds will also work.	

4.7.1.2.2 Full Speed

Signal Name	Measured at pin # of device	Rise Time (ns)				Fall Time (ns)				Jitter (for single transition) (nS)			
		Min	Meas.	Max	Fig	Min	Meas.	Max	Fig	Min	Meas.	Max	Fig
D+	J6.3	4		20		4		20		-3.5		+3.5	
D-	J6.2	4		20		4		20		-3.5		+3.5	

Table 16 - OTG Port, Device Mode: Full Speed Rise, Fall, Jitter

Test-060: OTG Port, Device Mode: Full Speed Rise, Fall, Jitter

Description	Criteria	Notes	Result
	Measurements (see table above) are within acceptable limits.	Electrical Tests covered as part of the Host Mode tests.	Not Tested

4.7.1.2.3 High Speed

Test-060: OTG Port, Device Mode: High Speed Rise, Fall, Jitter

Description	Criteria	Notes	Result
	Measurements (see table above) are within acceptable limits.	Electrical Tests covered as part of the Host Mode tests.	Not Tested

4.7.2 Type A Port

The PHY for this port is located on the processor. The port should be tested by connecting to a device and performing data reads and writes.

Test-040: USB Type A Port

Description	Criteria	Notes	Result
		Transferred files from RAM disk to USB and back. Used the U-boot and linux kernel provided as part of DaVinci-PSP-SDK-03.20.00.11	PASS

4.7.1 Host Port

4.7.1.1 Low Speed Testing

Signal Name	Measured at pin # of device	Rise Time (ns)				Fall Time (ns)				Jitter (for single transition) (nS)			
		Min	Meas.	Max	Fig	Min	Meas.	Max	Fig	Min	Meas.	Max	Fig
D+	J27.3												
D-	J27.2												

Table 17 - Host Port: Low Speed Rise, Fall, Jitter

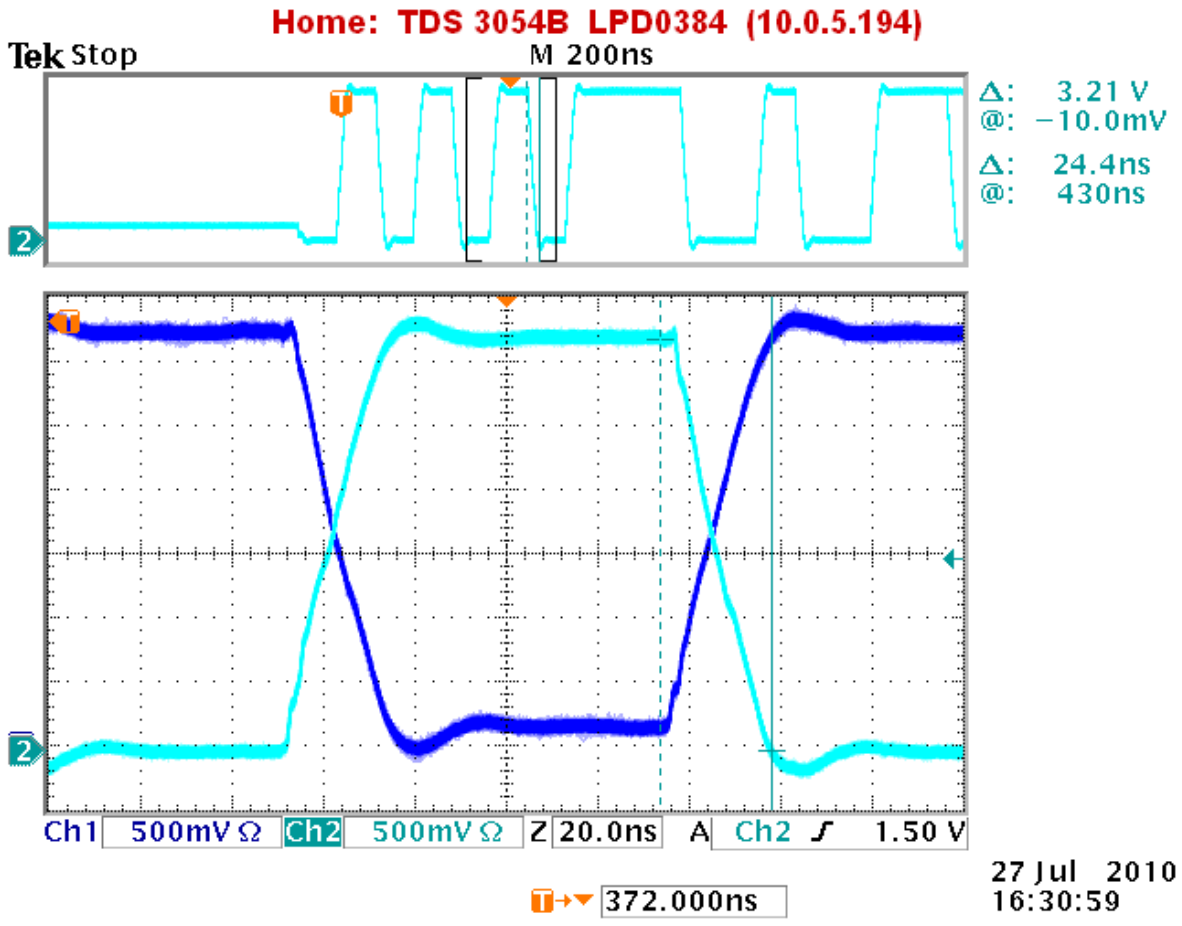
Test-061: Host Port: Low Speed Rise, Fall, Jitter

Description	Criteria	Notes	Result
	Measurements (see table above) are within acceptable limits.	Could not find a slow speed device suitable for testing. Assume that if the higher speeds are good the low speeds will also work.	Not Tested

4.7.1.2 Full Speed Testing

Signal Name	Measured at pin # of device	Rise Time (ns)				Fall Time (ns)				Jitter (for single transition) (nS)			
		Min	Meas.	Max	Fig	Min	Meas.	Max	Fig	Min	Meas.	Max	Fig
D+	J27.3	4	20	20		4	16.8	20		-3.5	0.2	+3.5	
D-	J27.2	4	20	20		4	18.8	20		-3.5	0.16	+3.5	

Table 18 - Host Port: Full Speed Rise, Fall, Jitter



Eye Diagram for full speed USB

Test-062: Host Port: Full Speed Rise, Fall, Jitter

Description	Criteria	Notes	Result
	Measurements (see table above) are within acceptable limits.		PASS

4.8 Video

4.8.1 LCD

A Logic 4.3" LCD display kit should be connected to the baseboard. A test graphic will be displayed on the LCD; proper image orientation, full screen accesses, and image quality will be verified through visual inspection.

Test-041: LCD Visual Inspection

Description	Criteria	Notes	Result
		Ran Test client 1-2-3 and ran display test "Display_test_OMAPL138_HEAD-1.0.9_RAM.elf"	PASS

4.8.1.1 LCD Backlight

The LCD backlight enable signal will be asserted and de-asserted to ensure that the LCD backlight turns on and off.

Test-042: LCD Backlight

Description	Criteria	Notes	Result
		Backlight came on as part of the Display test in the test client.. Used bootable test client 1-2-3 and test "Display_test_OMAPL138_HEAD-1.0.9_RAM.elf"	PASS

4.8.1.2 LCD Touch

A Logic 4.3" LCD display kit should be connected to baseboard. Firmware should read the X,Y location of several touches; X,Y coordinates for each touch should be printed to the RS-232 port.

Test-043: LCD Touch Here

Description	Criteria	Notes	Result
		Ran "test_touch" bsl test in CCSv4	Unsure PASS

4.8.2 S-Video In

A Logic 4.3" LCD display kit should be connected to baseboard. A test image input will be provided from a suitable source such as: VHS player, DVD player, test image generator. The test image will be VGA resolution. The image should be displayed on the LCD; proper image orientation, full screen accesses, and image quality will be verified through visual inspection.

Test-044: S-Video In

Description	Criteria	Notes	Result