Using Spansion Flash Devices with TI Sitara™ – AM3517 based

Version 1.0

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Spansion LLC

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Table of Contents

Table of Figures

1 Introduction

TI Sitara™ Processors are designed with ARM architecture solutions from ARM9™ to ARM® Cortex™-A8. It supports NAND, NOR, pSRAM, and DDR to run application. Code shadowing into DDR RAM is commonly used for fast code execution. General memory combinations are as below.

- NAND / DDR
- NOR / DDR
- NOR / NAND / DDR

This Application Note explains Memory Controllers in TI Sitara™ Processors, memory interface to Spansion NOR devices, and register setting parameters for timing interface. All of register setting parameters explained here in chapter 3 are only for reference.

1.1 Reference

R1) **AM35x ARM Microprocessor Technical Reference Manual Version B (Rev. B)**

- Chapter 2 : Memory Mapping
- Chapter 9 : Memory Subsystem
- Chapter 24 : Applications Processor Initialization

R2) AM3517/05 ARM Microprocessor (Rev. B)

- Chapter 6 : Timing requirements and switching characteristics

R3) Spansion S29GL-P NOR Device

R4) Spansion S29AL-J NOR Device

R5) Spansion S29VS-R NOR Device

R6) Spansion S29WS-P NOR Device

1.2 Abbreviations

ADP Address Data Parallel known as Demux Interface

ADM Address Data Multiplex known as Mux Interface

1.3 Revision History

Revision	Date	Comments
v1.0.0	06/Oct/2010	Initial Draft

2 Sitara™ Processors

The Sitara™ microprocessor family features are shown as below.

- ARM® Cortex™-A8 and ARM9™-based solutions with performance ranging from 375 MHz to 1 GHz
- Highly reusable software code bases that allow designers to easily scale within the product family by utilizing ARM processors and common peripheral sets
- Multiple operating frequencies, 3-D graphics acceleration, multiple packaging options and temperature operating points to further provide optimal flexibility to fit most application requirements.
- Low-cost development tools and free Linux and Windows® Embedded CE software baseports to accelerate both software and hardware development

It is suitable for a wide variety of applications such as portable data terminals, portable medical equipment, home and building automation, navigation systems, smart displays and human machine interaction (HMI) industrial interfaces and other applications which require high-performance, low-power processing capabilities.

AM37x: Cortex-A8 processors

- 800 MHz and 1 GHz processors delivering up to 2000 Dhrystone MIPS – AM3703 and AM3715
- Memory : SDRAM – LPDDR1, Flash – NOR/NAND/OneNAND

AM35x: Coretex-A8 Processors

- 600 MHz ARM Cortex-A8 core providing 1200 Dhrystone MIPS – AM3503 and AM3517
- Memory : SDRAM – DDR2/LPDDR1, Flash – NOR/NAND/OneNAND

AM17x and AM18x processors

- 375 MHz and 450 MHz ARM9 processors – AM1705 and AM1808
- Memory : SDRAM – DDR/DDR2/mDDR, Flash – NOR/NAND

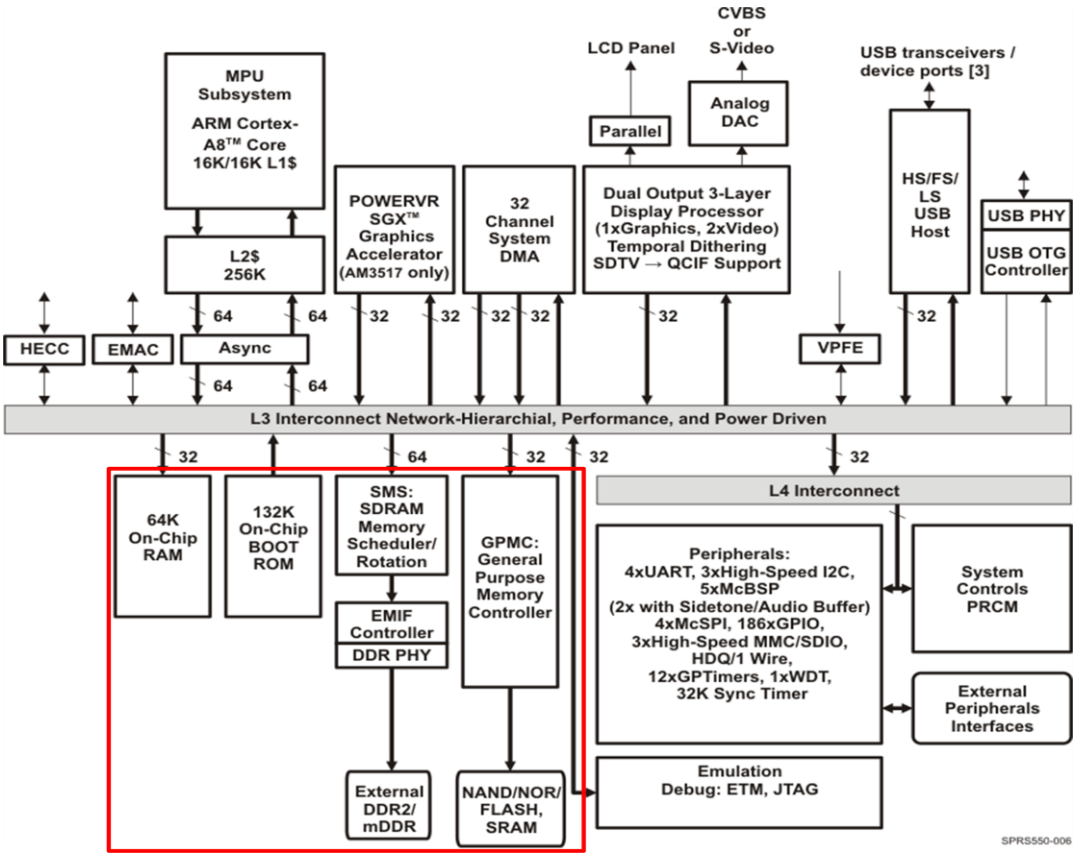

Figure 1. AM35x Block Diagram and Memory Block

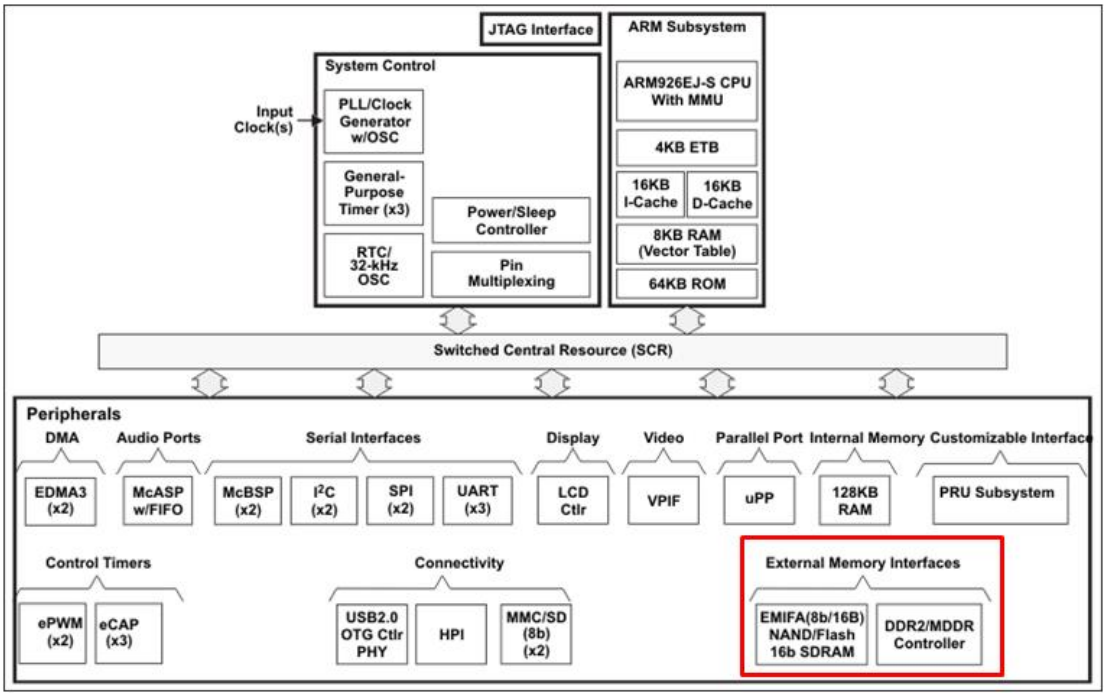

Figure 2. AM18x Block Diagram and Memory Block

2.1 Memory Subsystem in Sitara™

Memory system consists of On-chip memory (OCM) and two dedicated memory controllers – GPMC and SDRC.

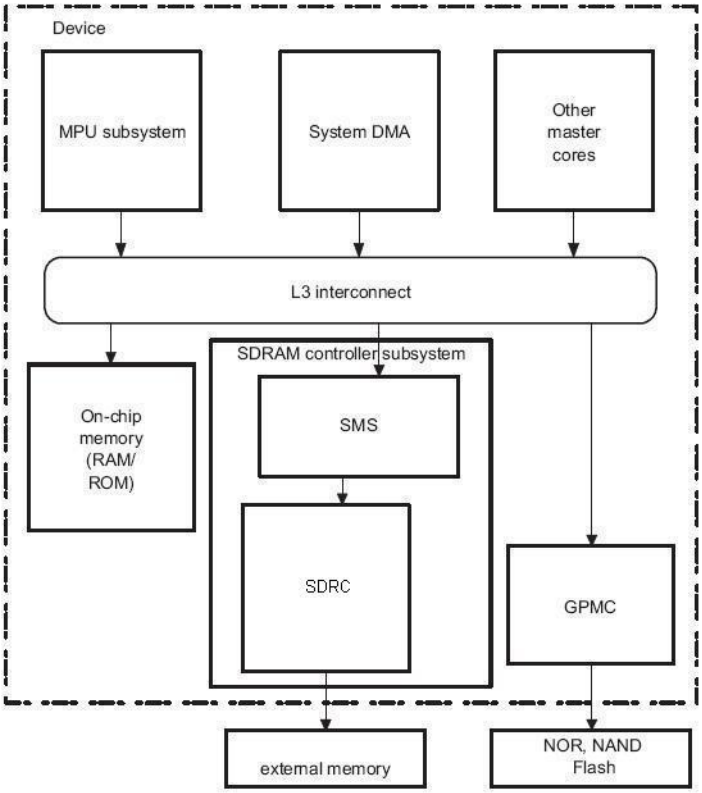

Figure 3. Memory Subsystem in Sitara™

On-chip memory (OCM) Subsystem

The On-chip memory subsystem consists of two separate on-chip memory controllers connected to on-chip ROM and on-chip RAM. These allow transactions between the system initiators and the multiple memories on booting time. Boot code and stack are placed here to run on booting sequence.

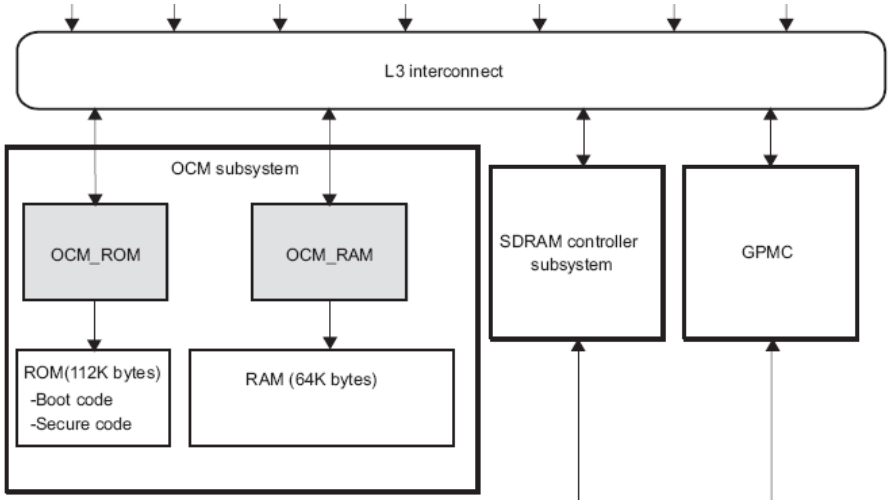

Figure 4. On-chip Memory Subsystem

SDRC – SDRAM Controller Subsystem

The SDRC subsystem provides connectivity between the processor and external discrete DDR SDRAM and high-performance interface to a variety of fast memory devices. It supports DDR2 and LPDDR1 device.

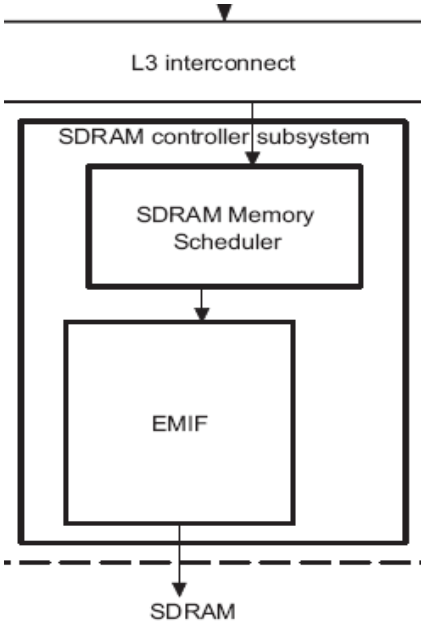

Figure 5. SDRC

Sitara™ Processor	SDRC	Interface
AM37x	LPDDR	1.8V, 16 or 32-bit, 1GB address
AM35x	DDR2, LPDDR1	1.8V, 16 or 32-bit, 1GB address

In AM17x and AM18x architecture, there is DDR2/mDDR controller instead of SDRC. Also SDRAM can be connected through EMIFA which is originally dedicated to NAND and NOR Flash.

Sitara™ Processor	DDR controller / EMIF	Interface
AM17x, AM18x	DDR2, mDDR	1.8V, 16-bit, 512MB(DDR2), 256MB(mDDR)
	SDRAM	3V, 16-bit

GPMC – General Purpose Memory Controller

The general-purpose memory controller (GPMC) is dedicated for interfacing external memory devices like SRAM-like memories, ASIC, NAND and NOR Flash and PSRAM.

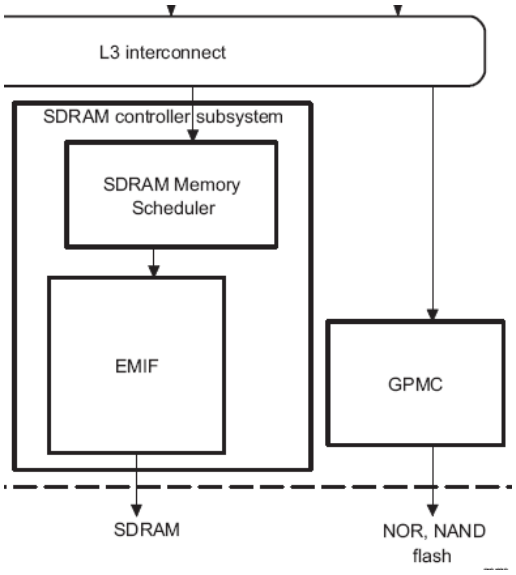

Figure 6. GPMC

3 General –Purpose Memory Controller (GPMC)

3.1 Understanding of GPMC

Memory Access Type

The GPMC is a 16-bit external memory controller. It provides a flexible programming model for communication with all standard memories and supports various accesses:

Access Type	Features
Asynchronous	Read / Write
Page	Read access with 4, 8, 16 Word
Synchronous	Read / Write access with and without Wrap Capability (4, 8, 16 Word)
Address Data Access	Address/Data Multiplexed Access
Endian	Little- and Big-endian

1.8V and 3V device can be applied by connecting supply voltage to GPMC IO voltage plane. It supports up to 100MHz for Synchronous access. There is load capacitance limit. To reach maximum frequency, do not connect many devices on GPMC.

GPMC/NOR Flash Synchronous Mode Timing Conditions

TIMING CONDITION PARAMETER		1.8V, 3.3V		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	0.3	1.8	ns
t_F	Input signal fall time	0.3	1.8	ns
Output Conditions				
C_{LOAD}	Output load capacitance	30		pF

GPMC/NOR Flash Interface Switching Characteristics Synchronous Mode

NO.	PARAMETER		1.8V, 3.3V		UNIT
			MIN	MAX	
F0	$t_{c(CLK)}$	Cycle time(1), output clock gpmc_clk period	10		ns

Figure 7. Synchronous Mode Timing Conditions for NOR Flash Device

Chip Selects and Memory Mapping Address

The system has two level memory mapping – Level 1 and Level 2.

- Level 1: 4 quarters labeled Q0, Q1, Q2, and Q3 and each quarter has 1GB address space.
- Level 2 : each quarter is divided into 8 blocks of 128MB

Quarter	Device Name	Start Address (HEX)	End Address (HEX)
Q0 (1GB)	Boot and GPMC	0x0000 0000	0x3FFF FFFF
Q1 (1GB)	On-Chip memory, L3, L4, SGX, IPSS	0x4000 0000	0x7FFF FFFF
Q2 (1GB)	EMIF4/SMS (SDRAM)	0x8000 0000	0xBFFF FFFF
Q3 (1GB)	RSVD	0xC000 0000	0xFFFF FFFF

GPMC is located in Q0 with 1GB access size. It has 8 independent GPMC chip selects (gpmc_ncs0 - 7) for NOR / NAND Flash and PSRAM memories. The chip-selects have a programmable start address and programmable size (16MB, 32MB, 64MB, or 128MB) in a total memory space of 1GB. In power up sequence, CS0 is only available to use. Spansion devices are connected to CS0-7 on 1GB size Q0.

External Device Example

External Devices to communicate are as below.

List of devices
8 bit Asynchronous / Synchronous devices
16 bit Asynchronous / Synchronous devices
16-bit Asynchronous / synchronous devices with ADP interface – 2KB limited address range
16-bit Asynchronous / synchronous devices with ADP interface adding latch circuit to cover max address
16-bit NOR device with ADM Interface
8-bit and 16-bit NAND Flash device
16-bit pseudo SRAM (pSRAM) devices

Summary of GPMC Features and Settings

Items	Descriptions
Device Type	Up to eight NOR or NAND protocol external memories or devices
Operating Voltage	1.8V preferred and 3V possible
Max Op. Frequency	Up to 100MHz (single device) with an L3-clock of 100MHz. Up to 83MHz (L3-clock divided by two) with an L3-clock of 166MHz
Addressing Capability	1GB divided into eight chip-selects
Max Memory Size	128MB
Min Memory Size	16MB. Aliasing occurs when addressing smaller memories
Data width	8-bit and 16-bit wide
Burst and Page Access	Burst of 4-8-16 Word
Others	Bus keeping and bus turn around

Power Domains

There are many power domains to apply. VDDSHV is power supply to Memory and Peripherals. It supports both 1.8V and 3.3V.

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
VDD_CORE	Core and oscillator macros power supply		1.152	1.20	1.248	V
	Noise (peak-peak)				24.00	mVpp
VDDS_SRAM_MPU	MPU SRAM LDO analog power supply		1.71	1.80	1.89	V
	Noise (peak-peak)				50.00	mVpp
VDDS_SRAM_CORE_BG	Core SRAM LDO and BandGap analog power supply		1.71	1.80	1.89	V
	Noise (peak-peak)				50.00	mVpp
VDDS_DPLL_MPU_USBHOST	MPU and USBHOST DPLL analog power supply		1.71	1.80	1.89	V
	Noise (peak-peak)				35.00	mVpp
VDDS_DPLL_PER_CORE	Peripherals and Core DPLLs analog power supply		1.71	1.80	1.89	V
	Noise (peak-peak)				35.00	mVpp
VDDA_DAC	DAC analog power supply		1.71	1.80	1.89	V
	Noise (peak-peak)				30.00	mVpp
VSSA_DAC	DAC analog ground			0.00		V
VDDA3P3V_USBPHY	Analog power supply for 3.3-V USB transceiver		3.14	3.30	3.47	V
	Noise (peak-peak)				70.00	mVpp
VDDA1P8V_USBPHY	Power Supply for 1.8-V USB transceiver		1.71	1.80	1.89	V
	Noise (peak-peak)				50.00	mVpp
VDDSHV	3.3-/1.8-V power supply	1.8 V Mode	1.71	1.80	1.89	V
		3.3 V Mode	3.14	3.30	3.47	V
VDDS	1.8-V power supply		1.71	1.80	1.89	V

Figure 8. Recommended Power Suppliers

Level shifters are used for signal conversion if multi-level signals need to be applied in system as below.

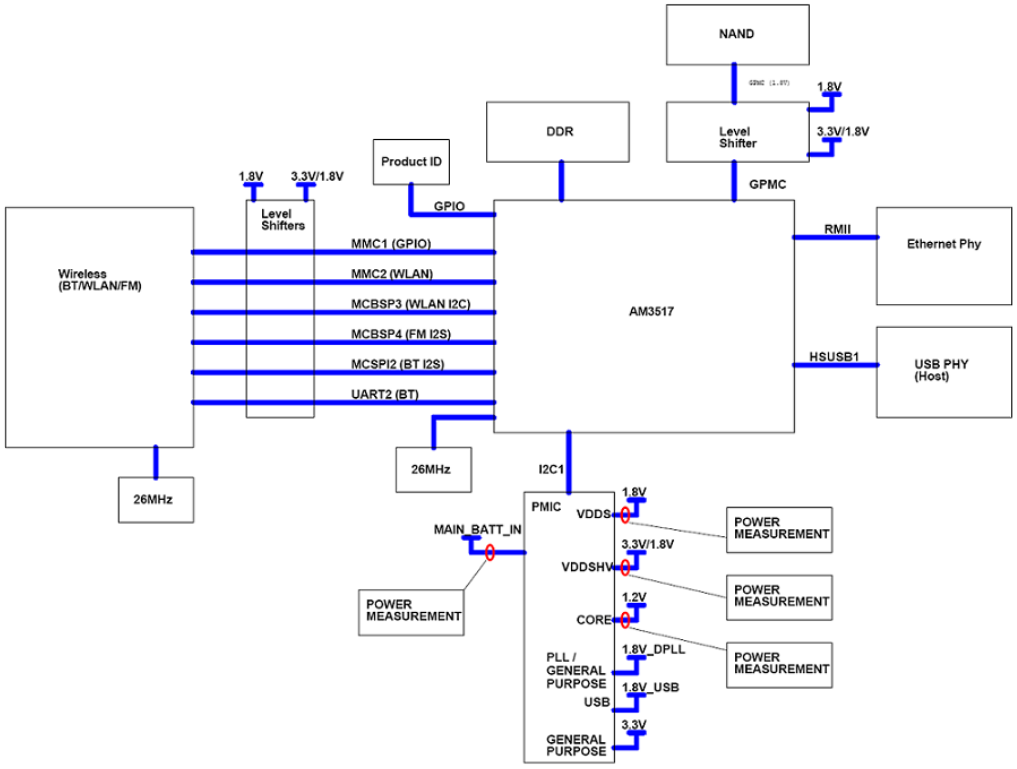

Figure 9. Example of Level Shifters for multi-level signals application

Memory Booting Configuration for NOR devices

Memory Booting Configuration Pins after POR

sys_boot [4:0]	Booting Sequence When SYS.BOOT[5] = 0 Memory Booting Preferred Order			
	First	Second	Third	Fourth
0b00000	*OneNAND*	EMAC	USB	
0b00001	*NAND*	EMAC	USB	
0b00010	*OneNAND*	EMAC	USB	MMC1
0b00011	*MMC2*	EMAC	USB	MMC1
0b00100	*OneNAND*	USB		
0b00101	*MMC2*	USB		
0b00110	*MMC1*	USB		
0b00111	*XIP*	EMAC	USB	
0b01000	*XDOC*	EMAC	USB	
0b01001	*MMC2*	EMAC	USB	
0b01010	*XIP*	EMAC	USB	MMC1
0b01011	*XDOC*	EMAC	USB	MMC1
0b01100	*NAND*	EMAC	USB	MMC1
0b01101	*XIP*	USB	UART	MMC1
0b01110	*XDOC*	USB	UART	MMC1
0b01111	*NAND*	USB	UART	MMC1
0b10000	*OneNAND*	USB	UART	MMC1
0b10001	*MMC2*	USB	UART	MMC1
0b10010	*MMC1*	USB	UART	
0b10011	*XIP*	UART		
0b10100	*XDOC*	UART		
0b10101	*NAND*	UART		
0b10110	*OneNAND*	UART		
0b10111	*MMC2*	UART		
0b11000	*MMC1*	UART		
0b11001	*XIP*	USB		
0b11010	*XDOC*	USB		
0b11011	*NAND*	USB		
0b11100	*SPI*	UART		
0b11101			Reserved(1)	
0b11110				
0b11111	*Fast XIP booting wait monitoring OFF*	USB	UART3	

(1) Must not be selected

Figure 10. sys_boot pin[4:0] configuration for NOR boot

In this memory booting configuration, XIP is used for NOR Flash memory booting.

3.2 Spansion Devices and Read Setting Parameters

Spansion Device Families are shown as below.

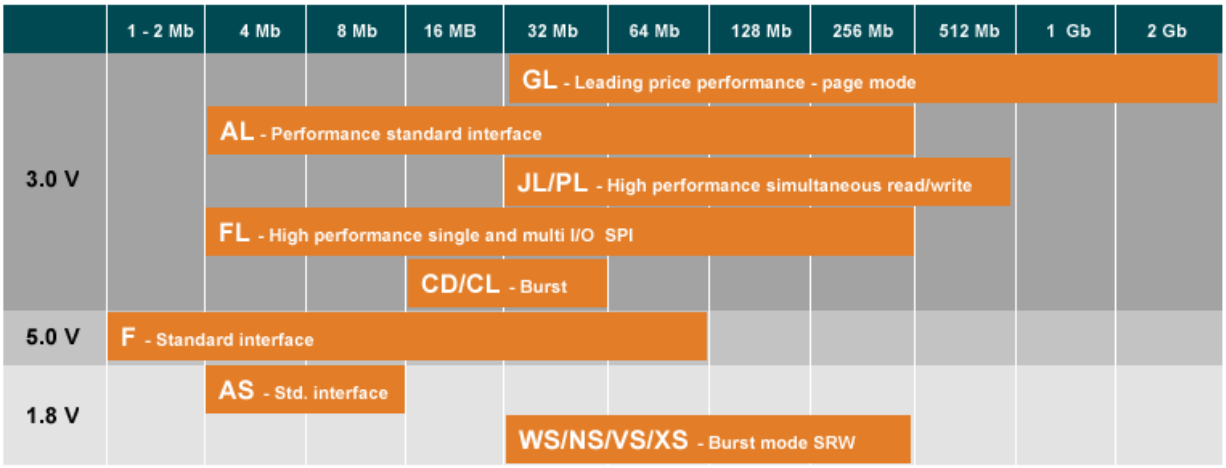

Figure 11. Spansion Device Families

Spansion Target devices for TI Sitara™ processors are as below.

- GL / PL can be used for asynchronous page read / asynchronous single write
- AL / JL can be used for asynchronous single read / asynchronous single write
- WS/NS/VS can be used for synchronous burst read / asynchronous single write

Device Group	Density (bit)	Data Interface	Bank	Voltage
S29GL-P	32Mb – 2Gb	16-bit, ADP, Asynch Page	1	3V
S29AL-J/D	4Mb – 256Mb	8/16-bit, ADP, Asynch	1	3V
S29PL-N	128Mb	16-bit, ADP, Asynch Page	4	3V
S29JL-J/H	32Mb – 512Mb	8/16-bit, ADP, Asynch	4	3V
S29WS-P	128Mb – 512Mb	16-bit, ADP, Synch Burst	16	1.8V
S29VS-R	64Mb – 256Mb	16-bit, ADM, Synch Burst	4, 8	1.8V
S92NS-R	512Mb	16-bit, ADM, Synch Burst	8	1.8V

Synchronous Multiple Read Timing Setup Parameters in TI Sitara™ Processors

Signal	Parameter	Description
CLK	GPMCFCLKDIVIDER	GPMC_CLK divider ratio ➔ 0 = 1:1, 1 = 1:2, 2 = 1:4
	CLKACTIVATIONTIME	GPMC_CLK output delay count
Read Op	RDCYCLETIME	Read Op. Cycle Count : RDCYCLETIME0 + RDCYCLETIME1
	RDACCESSTIME	Initial Access Time to 1st Data Out
nCS	CSONTIME	nCS Active Count
	CSRDOFFTIME	nCS De-active Count
nADV	ADVONTIME	nADV Asserted Count
	ADVOFFTIME	nADV De-asserted Count
nOE	OEONTIME	nOE Asserted Count
	OEOFFTIME	nOE De-asserted Count : OEOFFTIME0 + OEOFFTIME1
PageBurstAccess	PAGEBURSTACCESSTIME	Delay between successive data reads in burst operation
WAIT Monitor	WAITMONITORINGTIME	WAIT pin de-asserted time with valid data 0 : same cycle as valid data / 1 : one cycle before valid data
WAIT Polarity	WAITxPINPOLARITY	Indicate valid data is not ready on bus ➔ 0/1 : Active Low/ High
Wrap Burst	WRAPBURST	Synchronous wrapping feature ➔ 0/1 : Disable/Enable
Page Length	ATTACHEDDEVICEPAGELENGTH	Page (burst) Size ➔ 0/1/2 : 4/8/16 words

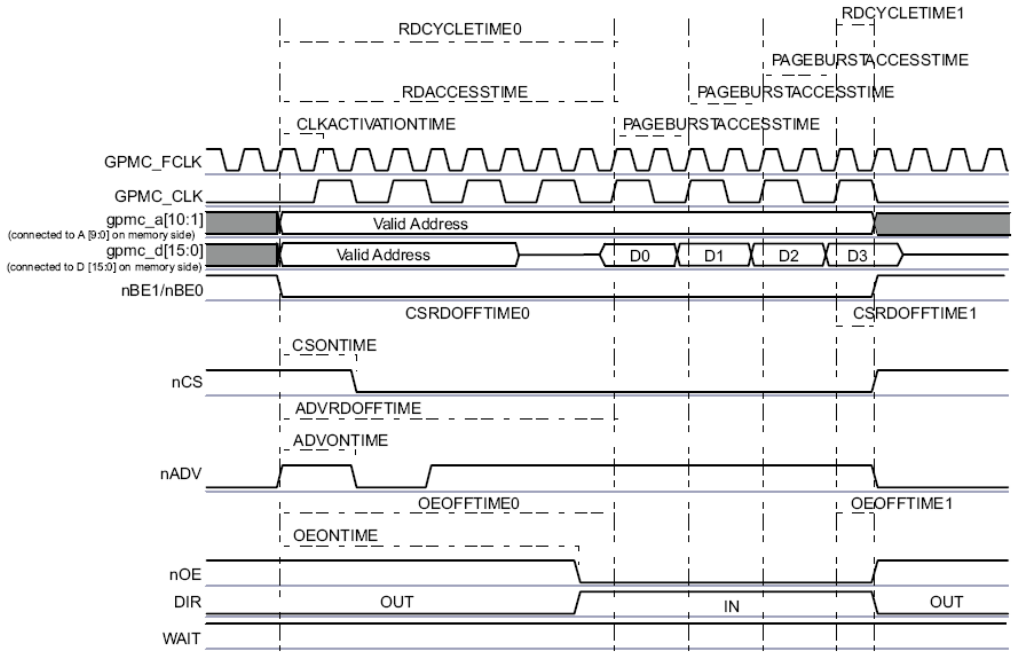

Figure 12. Synchronous READ Timing Parameters

Asynchronous Single/Page Read Timing Setup Parameters in TI Sitara™ Processors

Signal	Parameter	Description
CLK	~~GPMCFCLKDIVIDER~~	
	~~CLKACTIVATIONTIME~~	
Read Op	RDCYCLETIME	Read Op. Cycle Count
	RDACCESSTIME	Initial Access Time to Data Out
nCS	CSONTIME	nCS Active Count
	CSRDOFFTIME	nCS De-active Count
nADV	ADVONTIME	nADV Asserted Count
	ADVOFFTIME	nADV De-asserted Count
nOE	OEONTIME	nOE Asserted Count
	OEOFFTIME	nOE De-asserted Count : OEOFFTIME0 + OEOFFTIME1
PageBurstAccess	PAGEBURSTACCESSTIME	Delay between successive data reads in burst operation
WAIT Monitor	~~WAITMONITORINGTIME~~	
WAIT Polarity	~~WAITxPINPOLARITY~~	
Wrap Burst	~~WRAPBURST~~	
Page Length	ATTACHEDDEVICEPAGELENGTH	Page (burst) Size ➔ 0/1/2 : 4/8/16 words

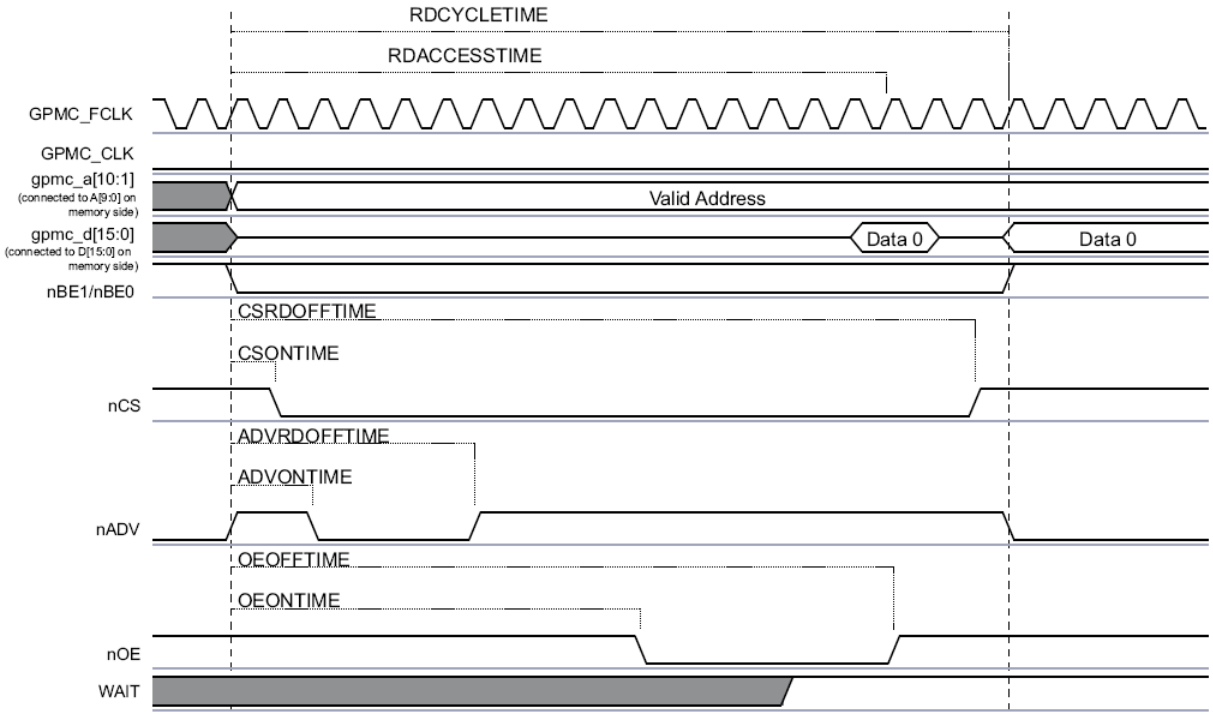

Figure 13. Asynchronous Single READ Timing Parameters

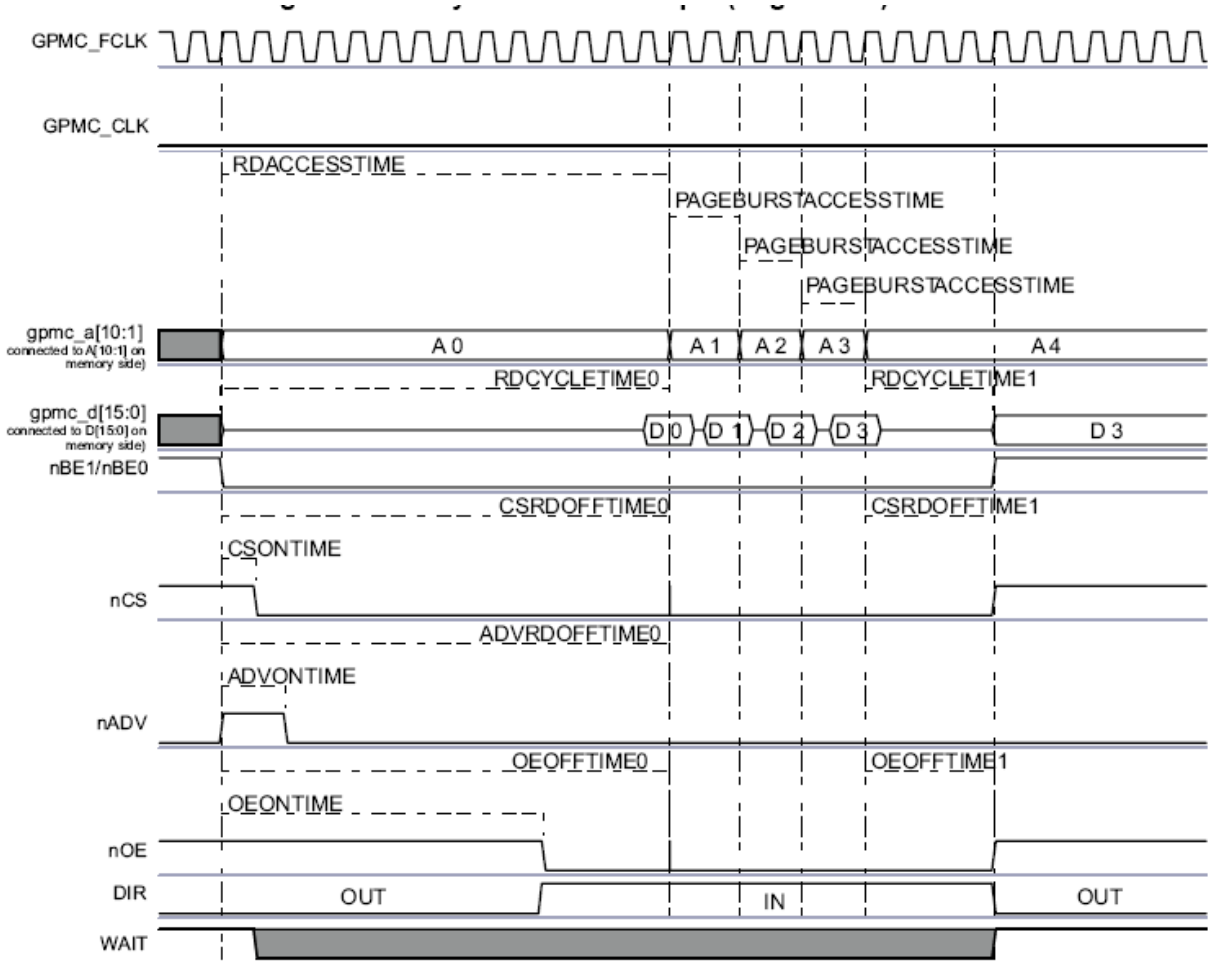

Figure 14, Asynchronous Page READ Timing Parameters

All of register setting parameters explained here after are only for reference and need to test on target board.

3.3 GPMC Interface to 16-bit, ADP, Asynchronous NOR Flash

Below shows interface between GPMC and Spansion ADP Asynchronous NOR devices

- S29GL-N/P : 32Mbit, 64Mbit, 128Mbit, 256Mbit, 512Mbit, 1Gbit, 2Gbit
- S29AL-J/D : 8Mbit, 16Mbit, 32Mbit
- S29PL-N : 128Mbit
- S29JL-J : 32Mbit, 64Mbit

Features	**S29GL-N/P**	**S29AL-J/D**	S29PL-N	**S29JL-J**
Voltage	3V			
Initial Access Time	90ns	55ns	65ns	55ns
Page Access Time	25ns	N/A	25ns	N/A
Bank #	1	1	4	4
Boot Mode	Uniform : GL-N/P Top/Bottom : GL-N	Top and Bottom	Dual Boot	Top and Bottom
Erase Block Size	64KB : Main 8KB : Boot (GL-P)	64KB : Main 8/16/32KB : Boot	256KB : Main 64KB : Boot	64KB : Main 8KB : Boot
Burst Length	8 words	Single	8 words	Single
Write Protection Pin (WP#)	Available	Available	Available	Available

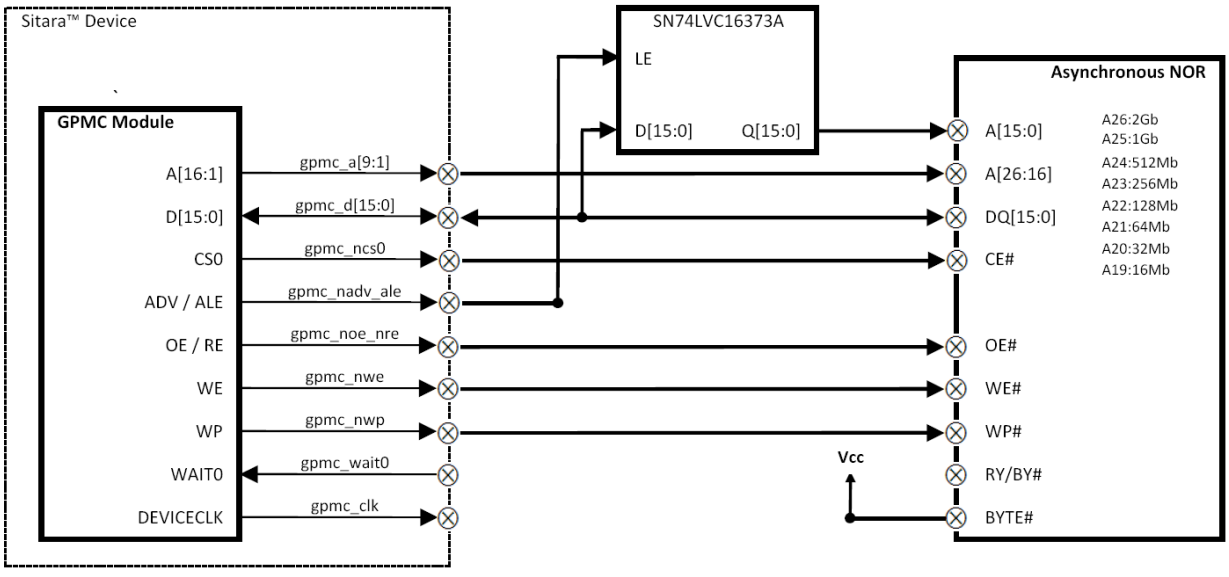

Figure 15. GPMC Interface to Spansion ADP Asynchronous Devices

Asynchronous Page Read Device Timing Configuration based on GL-P

Parameter JEDEC	Parameter Std.	Description (Notes)		Test Setup		Speed Options 90	100	110	120	130	Unit
t_{AVAV}	t_{RC}	Read Cycle Time		$V_{IO} = V_{CC} = 2.7$ V	Min	–	100	110	120	–	ns
				$V_{IO} = 1.65$ V to V_{CC}, $V_{CC} = 3$ V		–	–	110	120	130	
				$V_{IO} = V_{CC} = 3.0$ V		90	100	110	–	–	
t_{AVQV}	t_{ACC}	Address to Output Delay (1)		$V_{IO} = V_{CC} = 2.7$ V	Max	–	100	110	120	–	ns
				$V_{IO} = 1.65$ V to V_{CC}, $V_{CC} = 3$ V		–	–	110	120	130	
				$V_{IO} = V_{CC} = 3.0$ V		90	100	110	–	–	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay (2)		$V_{IO} = V_{CC} = 2.7$ V	Max	–	100	110	120	–	ns
				$V_{IO} = 1.65$ V to V_{CC}, $V_{CC} = 3$ V		–	–	110	120	130	
				$V_{IO} = V_{CC} = 3.0$ V		90	100	110	–	–	
	t_{PACC}	Page Access Time			Max	25					ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25					ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (3)			Max	20					ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (3)			Max	20					ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0					ns
	t_{OEH}	Output Enable Hold Time (3)	Read		Min	0					ns
			Toggle and Data# Polling		Min	10					ns
	t_{CEH}	Chip Enable Hold Time	Read		Min	35					ns

Figure 16. GL-P AC Characteristics for Asynchronous Page Read

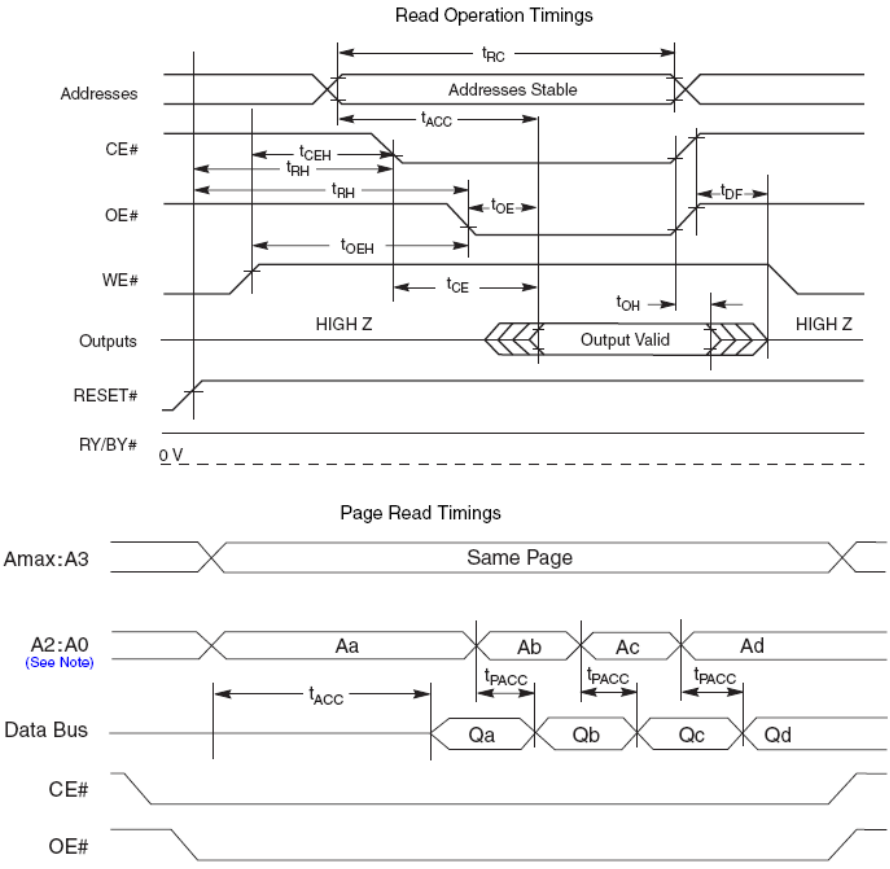

Figure 17. GL-P Asynchronous Read Waveform

We can find below register settings to run, given 104MHz GPMC_FCLK (9.615ns clock duration).

Signal	Parameter	Value and Description
CLK	~~GPMCFCLKDIVIDER~~	
	~~CLKACTIVATIONTIME~~	
Read Op	RDCYCLETIME	0x0F : ReadAccessTime + DataHolding(1Clk) + tDF(2Clk) = 15 clocks
	RDACCESSTIME	0x0B : AddressLatch (2Clk) + InitialAccessTime(90ns) >> 12 clocks to make 115.4ns
nCS	CSONTIME	0x2 : Assert after address latch
	CSRDOFFTIME	0x0C : ReadAccessTimg + DataHolding(1CLK)
nADV	ADVONTIME	0x0 : Immediate Assert with Read Cycle
	ADVOFFTIME	0x01 : Provide AVD assertion duration with 1 cycle
nOE	OEONTIME	0x2 : Assert after address latch
	OEOFFTIME	0x0C : ReadAccessTimg + DataHolding(1CLK)
PageBurstAccess	PAGEBURSTACCESSTIME	0x03 : tPACC = 25ns >> 3 Clk access time
WAIT Monitor	~~WAITMONITORINGTIME~~	
WAIT Polarity	~~WAITxPINPOLARITY~~	
Wrap Burst	~~WRAPBURST~~	
Page Length	ATTACHEDDEVICEPAGELENGTH	1 : 8 words burst size

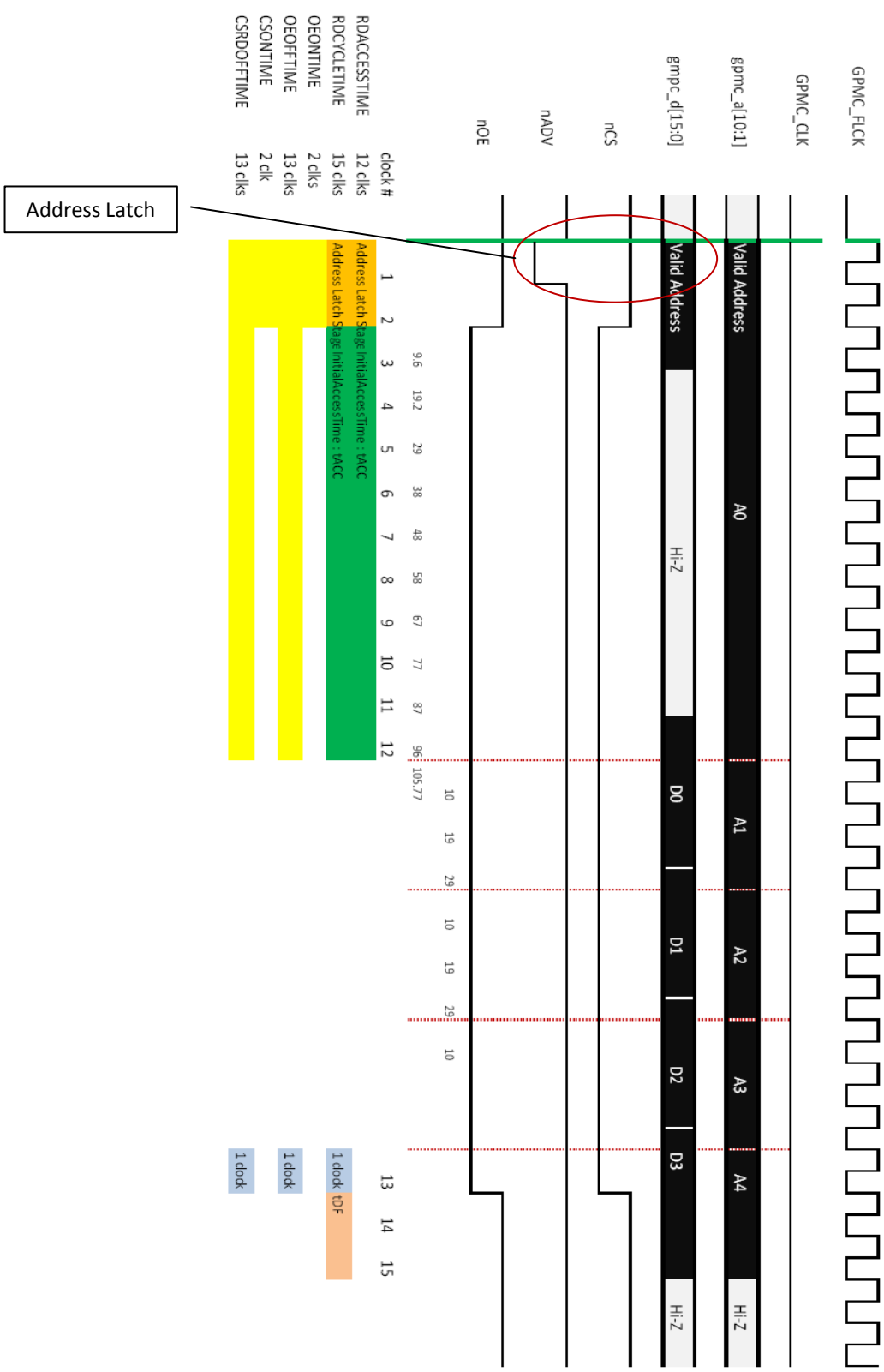

Figure 18. GL-P Asynchronous Page Read Waveform Generation

Asynchronous Single Read Device Timing Configuration based on AL-J

Parameter		Description		Test Setup		Speed Options		Unit
JEDEC	Std					70	55	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	55	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		$CE\# = V_{IL}$ $OE\# = V_{IL}$	Max	70	55	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		$OE\# = V_{IL}$	Max	70	55	
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	30	
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	16		
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	16		
	$t_{SR/W}$	Latency Between Read and Write Operations			Min	20		
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0		
			Toggle and Data# Polling		Min	10		
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0		

Figure 19. AL-J AC Characteristics for Asynchronous Single Read

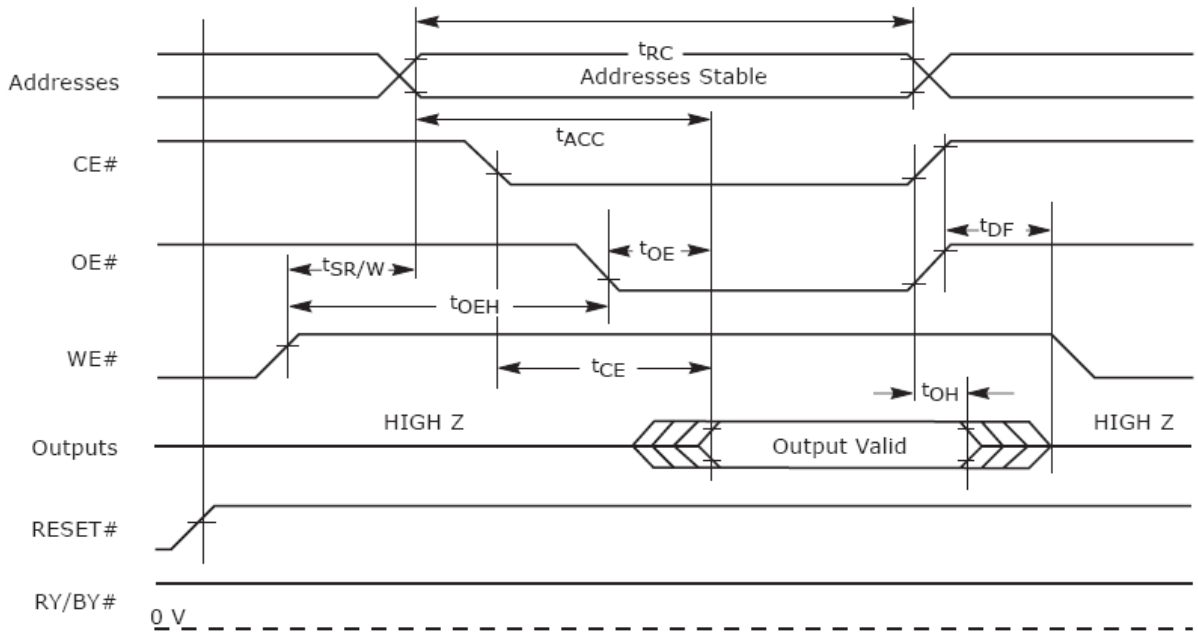

Figure 20. AL-J Asynchronous Read Waveform

We can find below register settings to run, given 104MHz GPMC_FCLK (9.615ns clock duration).

Signal	Parameter	Value and Description
CLK	~~GPMCFCLKDIVIDER~~	
	~~CLKACTIVATIONTIME~~	
Read Op	RDCYCLETIME	0x0C : ReadAccessTime + DataHolding(1Clk) + tDF(2Clk) = 13 clocks
	RDACCESSTIME	0x0A : AddressLatch (2Clk) + InitialAccessTime(70ns) >> 10 clocks to make 96.2ns
nCS	CSONTIME	0x2 : Assert after address latch
	CSRDOFFTIME	0x0B : ReadAccessTimg + DataHolding(1CLK)
nADV	ADVONTIME	0x0 : Immediate Assert with Read Cycle
	ADVOFFTIME	0x01 : Provide AVD assertion duration with 1 cycle
nOE	OEONTIME	0x2 : Assert after address latch
	OEOFFTIME	0x0B : ReadAccessTimg + DataHolding(1CLK)
PageBurstAccess	~~PAGEBURSTACCESSTIME~~	
WAIT Monitor	~~WAITMONITORINGTIME~~	
WAIT Polarity	~~WAITxPINPOLARITY~~	
Wrap Burst	~~WRAPBURST~~	
Page Length	ATTACHEDDEVICEPAGELENGTH	3 : Single Word

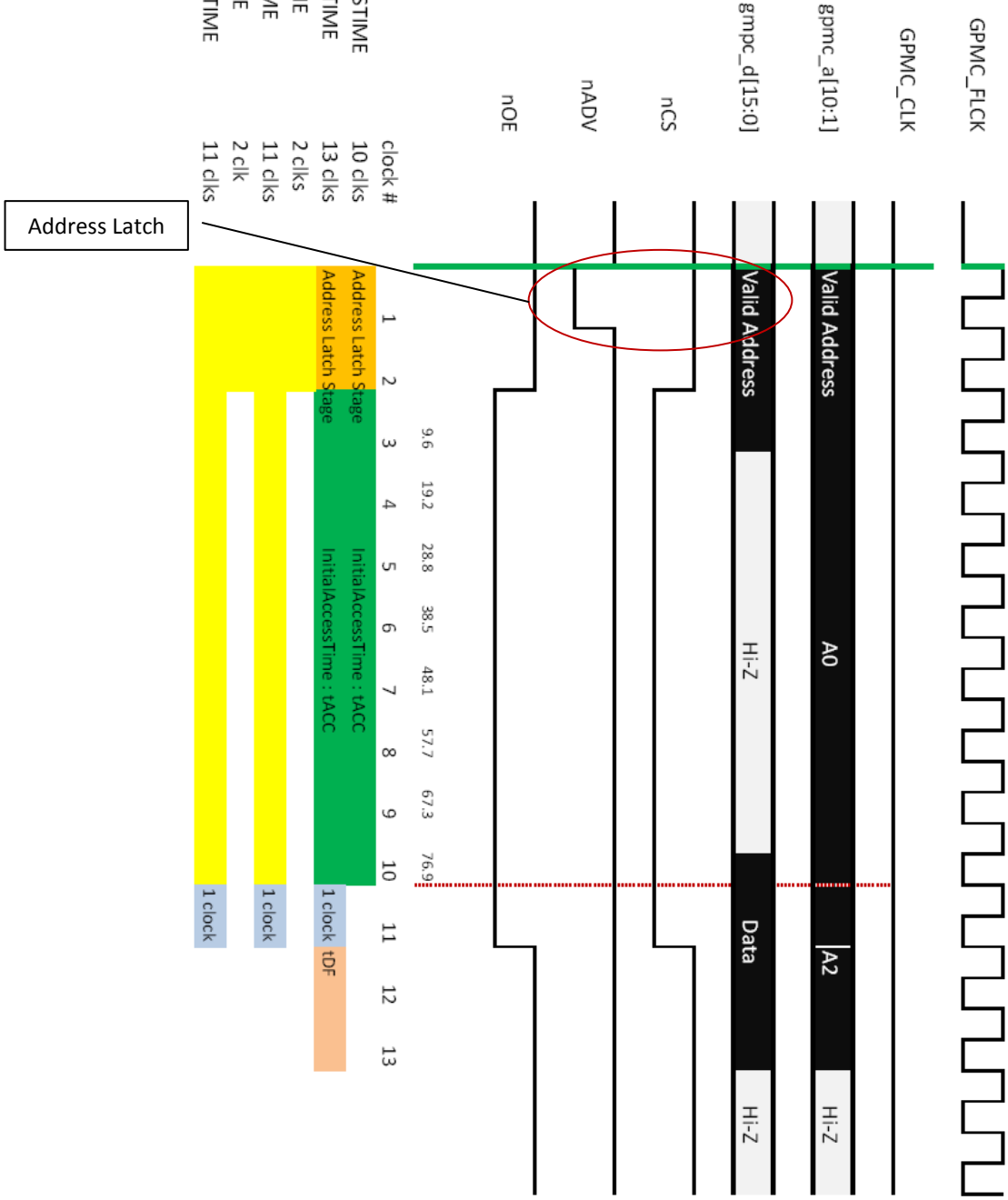

Figure 21. AL-J Asynchronous Single Read Waveform Generation

3.4 GPMC Interface to 16-bit, ADM, Synchronous NOR Flash

Below shows interface between GPMC and Spansion ADM Synchronous NOR Flash devices

- S29VS-R (256Mbit, 128Mbit, 64Mbit)
- S29NS-R (512Mbit) devices.

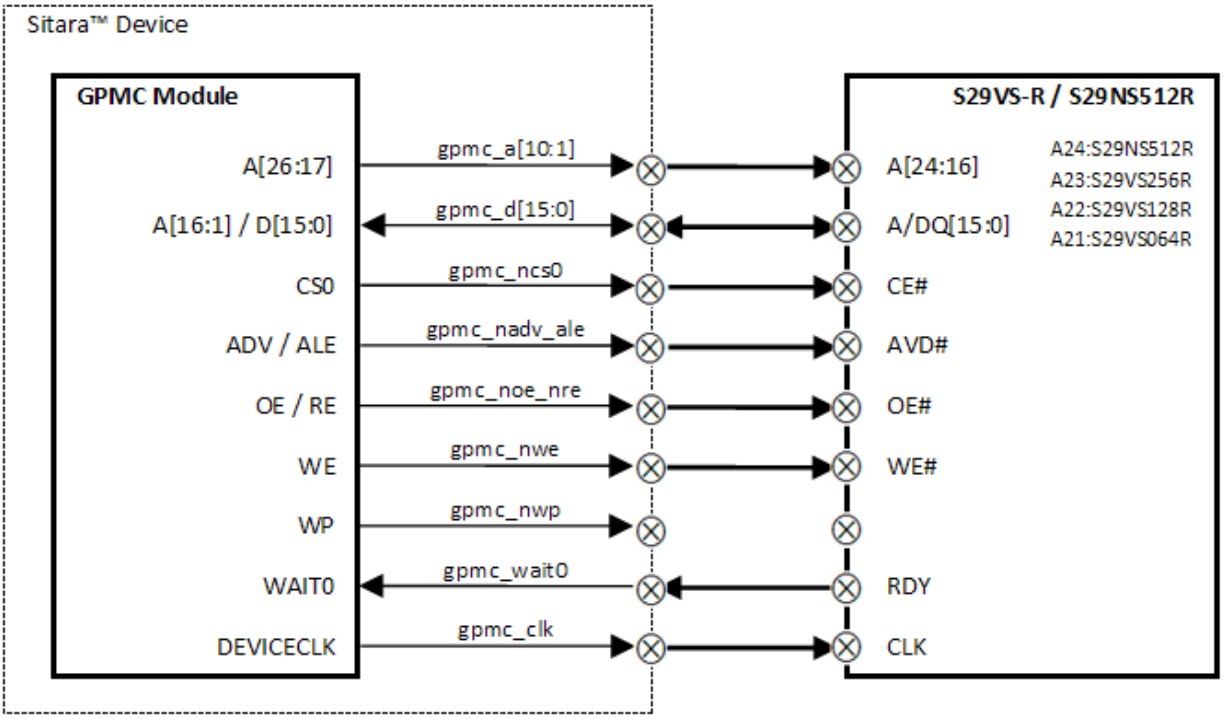

Figure 22. GPMC Interface to Spansion ADM Synchronous Devices

Spansion ADM NOR Flash Device features are as below.

Features	S29VS064R	S29VS128R / S29VS256R	S29NS512R
Voltage	1.8V		
Max Synch. Speed	104MHz	108MHz	104MHz
Initial Access Time	80ns	75ns	
Bank #	4	8	16
Boot Mode	Top	Top or Bottom	Uniform
Erase Block Size	64KB : Main 16KB : Boot	128KB : Main 32KB : Boot	128KB
Burst Length	8-, 16-Word Linear Burst with Wrap and Continuous		
Write Protection Pin (WP#)	Not Available		

AC Characteristics–Synchronous Burst Read

Parameter (Notes)	Symbol		83 MHz	104 MHz	108 MHz	Unit
Clock Frequency	CLK	Min	DC (0) for operations other than continuous and 32 byte synchronous burst. 120 in 32 Byte burst 1000 in continuous burst			KHz
Clock Cycle	t_{CLK}	Min	12	9.6	9.26	ns
CLK Rise Time	t_{CLKR}	Max	2.5	1.92	1.852	ns
CLK Fall Time	t_{CLKF}					
CLK High or Low Time	$t_{CLKH/L}$	Min	5	4	3.86	ns
Internal Access Time	t_{IA}	Max	75		72.34	ns
Burst Access Time Valid Clock to Output Delay	t_{BACC}	Max	9	7.6	6.75	ns
AVD# Setup Time to CLK	t_{AVDS}	Min	4		3.38	ns
AVD# Hold Time from CLK	t_{AVDH}	Min	3		2.89	ns
Address Setup Time to CLK	t_{ACS}	Min	4		2.89	ns
Address Hold Time from CLK	t_{ACH}	Min	5		4.82	ns
Data Hold Time from Next Clock Cycle	t_{BDH}	Min	3	2	2	ns
Output Enable to Data	t_{OE}	Max	15			ns
CE# Disable to Output High Z (2)	t_{CEZ}	Max	10			ns
OE# Disable to Output High Z (2)	t_{OEZ}	Max	10			ns
CE# Setup Time to CLK	t_{CES}	Min	4		3.38	ns
CLK to RDY valid	t_{RACC}	Max	9	7.6	6.75	ns
CE# low to RDY valid	t_{CR}	Max	10			ns
AVD# Pulse Width	t_{AVDP}	Min	6			ns

Figure 23. VS-R AC Characteristics for Synchronous Burst Read

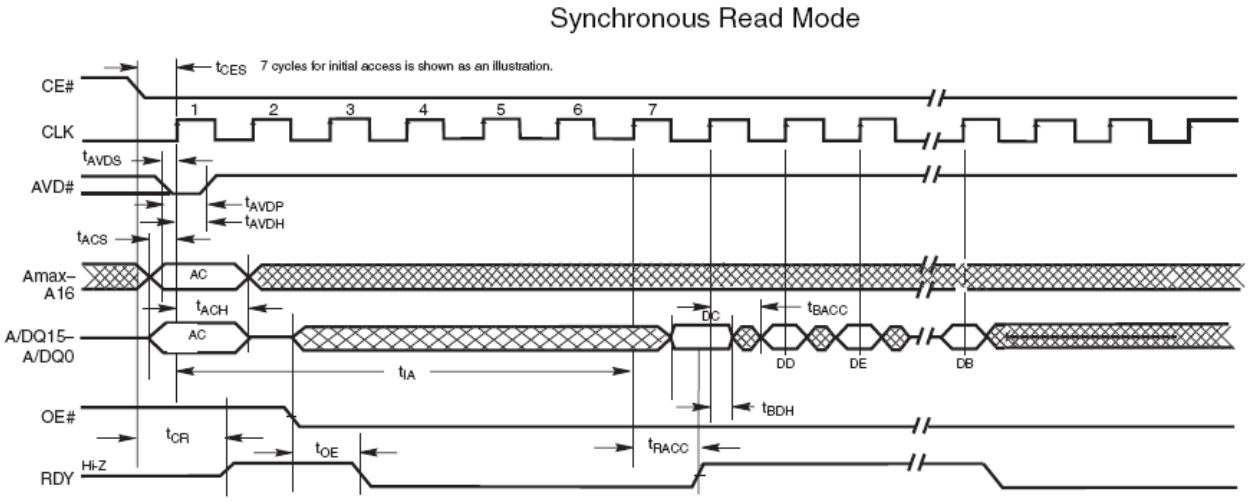

Figure 24. VS-R Synchronous Read Waveform

Wait State vs. Frequency

Wait State	Frequency (Maximum MHz)
3	27
4	40
5	54
6	66
7	80
8	95
9	104
10	120

Figure 25. Wait State and Frequency for VS-R

We can find below register settings to run, given 104MHz GPMC_FCLK (9.615ns clock duration).

Signal	Parameter	Value and Description
CLK	GPMCFCLKDIVIDER	0x00 : Clock divider radio 1:1 GPMC_CLK = GPMC_FCLK
	CLKACTIVATIONTIME	0x01 (1 clock delay) : GPMC_CLK output delay count
Read Op	RDCYCLETIME	0x0B : ReadAccessTime + 1clock = 11 clocks to generate 105.76ns
	RDACCESSTIME	0x0A : 92.215ns = ClkActiavationTime + tIACC + DataSetuptTime (9.615ns + 75ns + 7.6ns) >> 10 clocks to make 96.12ns
nCS	CSONTIME	0x0 : Immediate Assert with Read Cycle
	CSRDOFFTIME	0x0B : Same with RDCYCLETIME
nADV	ADVONTIME	0x0 : Immediate Assert with Read Cycle
	ADVEXTRADELAY	0x1 : nADV half clock delay of GPMC_FCLK
	ADVOFFTIME	nADV De-asserted Count : Provide AVD assertion duration with 1 cycle
nOE	OEONTIME	0x04 : Assert after 3 clocks
	OEOFFTIME	0x0B : Same with CSRDOFFTIME
PageBurstAccess	PAGEBURSTACCESSTIME	0x01 : tBACC = 7.6ns >> 1 clock access time
WAIT Monitor	WAITMONITORINGTIME	0x1 : one cycle before valid data
WAIT Polarity	WAITxPINPOLARITY	0x0 : Active Low
Wrap Burst	WRAPBURST	1 : Wrap Burst Enable
Page Length	ATTACHEDDEVICEPAGELENGTH	2 : 16 words burst size

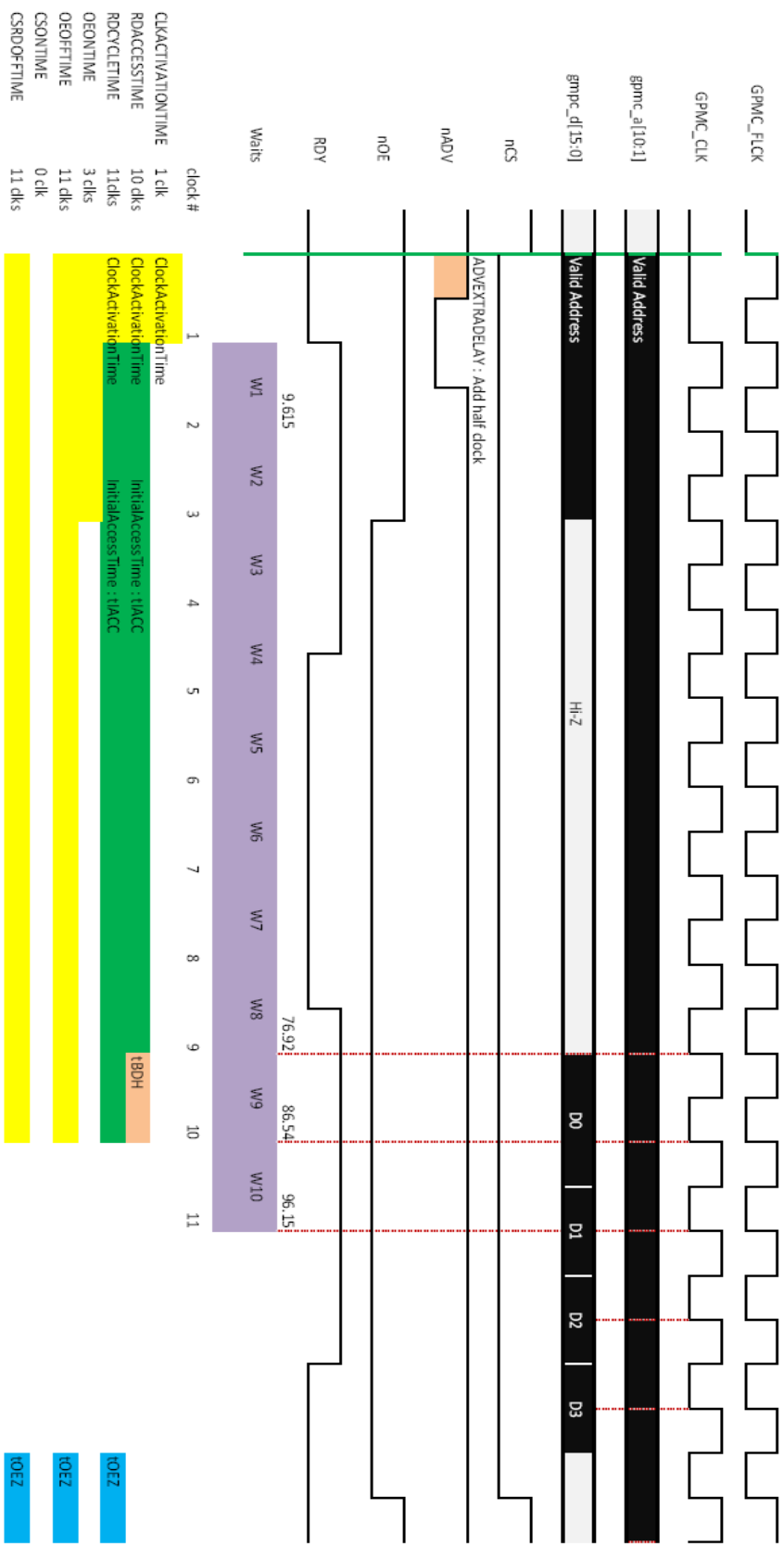

Figure 26. VS-R Synchronous Read Waveform Generation

3.5 GPMC Interface to 16-bit, ADP, Synchronous NOR Flash

Below shows interface between GPMC and Spansion ADP Synchronous NOR Flash devices

- S29WS-R (64Mbit)
- S29WS-P (128Mbit, 256Mbit, 512Mbit)

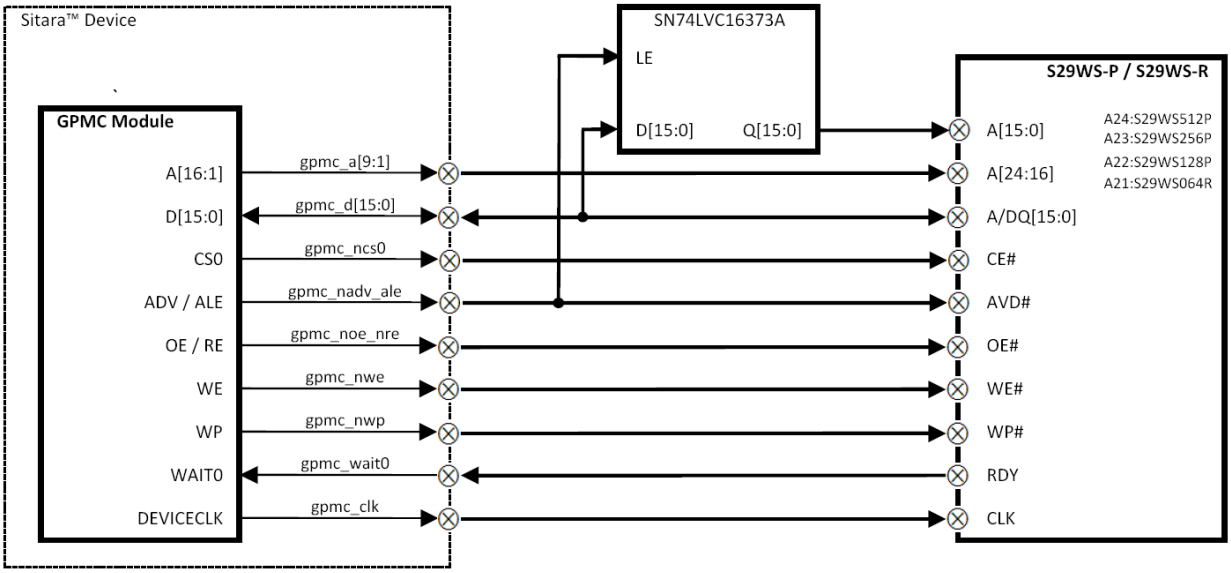

Figure 27. GPMC Interface to Spansion ADP Synchronous Devices

Spansion S29WS-P and S29WS-R ADP NOR Flash Device features are shown as below.

Features	S29WS064R	S29WS128P / 29WS256P / S29WS512P
Voltage	1.8V	
Max Synch. Speed	108MHz	104MHz
Initial Access Time	80ns	Depending on burst speed
Bank #	4	16
Boot Mode	Top or Bottom	Top and Bottom
Erase Block Size	64KB : Main 16KB : Boot	128KB : Main 32KB : Boot
Burst Length	8-, 16-Word Linear Burst with Wrap and Continuous	
Write Protection Pin (WP#)	Not Available	Available

Synchronous/Burst Read

Parameter		Description		54 MHz	66 MHz	80 MHz	104 MHz	Unit
JEDEC	Standard							
	t_{IACC}	Synchronous Access Time	Max	(WS-1) * t_{CK} + t_{BACC}				ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	13.5	11.2	9	7.6	ns
	t_{ACS}	Address Setup Time to CLK (Note 1)	Min	5	4	4	3.5	ns
	t_{ACH}	Address Hold Time from CLK (Note 1)	Min	6	6	5	5	ns
	t_{BDH}	Data Hold Time	Min	4	3	3	2	ns
	t_{RDY}	Chip Enable to RDY Active	Max	10				ns
	t_{OE}	Output Enable to RDY Low	Max	13.5	11.2	9	7.6	ns
	t_{CEZ}	Chip Enable to High Z	Max	10	10	10	7	ns
	t_{OEZ}	Output Enable to High Z	Max	10	10	10	7	ns
	t_{CES}	CE# Setup Time to CLK	Min	6				ns
	t_{RACC}	Ready Access Time from CLK	Max	13.5	11.2	9	7.6	ns
	t_{CAS}	CE# Setup Time to AVD#	Min	0				ns
	t_{AVC}	AVD# Low to CLK Setup Time	Min	6				ns
	t_{AVD}	AVD# Pulse	Min	t_{CLK}				ns

Notes:

1. *Addresses are latched on the rising edge of CLK*
2. *Synchronous Access Time is calculated using the formula (#of WS - 1)*(clock period) + (t_{BACC} or Clock to Out)*

Figure 28. WS-P AC Characteristics for Synchronous Burst Read

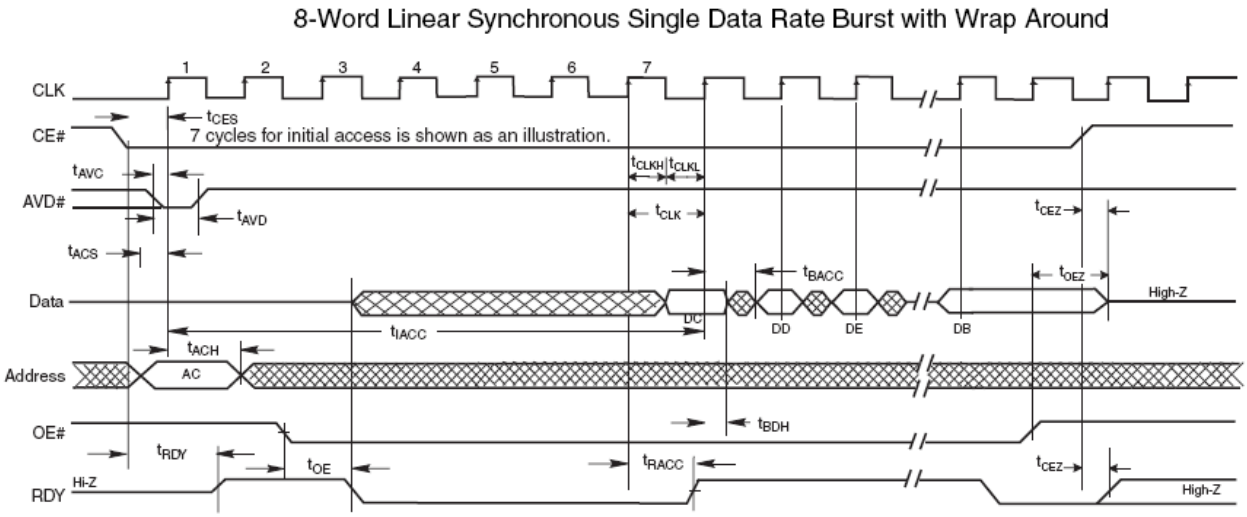

Figure 29. WS-P Synchronous Read Waveform

Non-Continuous Burst Mode with Wrap Around Burst Mode.

Max Frequency	Wait State Requirement
Frequency ≤ 27 MHz	3
27 MHz < Frequency ≤ 40 MHz	4
40 MHz < Frequency ≤ 54 MHz	5
54 MHz < Frequency ≤ 66 MHz	6
66 MHz < Frequency ≤ 80 MHz	7
80 MHz < Frequency ≤ 95 MHz	8
95 MHz < Frequency ≤ 104 MHz	11

Figure 30. Wait State and Frequency for WS-P

We can find below register settings to run, given 104MHz GPMC_FCLK (9.615ns clock duration).

Signal	Parameter	Value and Description
CLK	GPMCFCLKDIVIDER	0x00 : Clock divider radio 1:1 GPMC_CLK = GPMC_FCLK
	CLKACTIVATIONTIME	0x02 (2 clock delay) : GPMC_CLK output delay count
Read Op	RDCYCLETIME	0x0C : ReadAccessTime + 1clock = 12 clocks to generate 115ns
	RDACCESSTIME	0x0C : 122.98ns = Addr Latch + ClkActiavationTime + tIACC(11CLK and tBACC) = 9.615ns + 9.615ns + ((11-1)x9.615ns + 7.6ns) >> 12 clocks to make 122.98ns
nCS	CSONTIME	0x0 : Immediate Assert with Read Cycle
	CSRDOFFTIME	0x0D : Same with RDCYCLETIME
nADV	ADVONTIME	0x0 : Immediate Assert with Read Cycle
	ADVEXTRADELAY	0x1 : nADV half clock delay of GPMC_FCLK
	ADVOFFTIME	0x02 : nADV De-asserted Count with 2 cycles (1st : Address Latch, 2nd : Address Capture on Processor)
nOE	OEONTIME	0x04 : Assert after 4 clocks
	OEOFFTIME	0x0D : Same with CSRDOFFTIME
PageBurst Access	PAGEBURSTACCESSTIME	0x01 : tBACC = 7.6ns >> 1 clock access time
WAIT Monitor	WAITMONITORINGTIME	0x1 : one cycle before valid data
WAIT Polarity	WAITxPINPOLARITY	0x0 : Active Low
Wrap Burst	WRAPBURST	1 : Wrap Burst Enable
Page Length	ATTACHEDDEVICEPAGELENGTH	2 : 16 words burst size

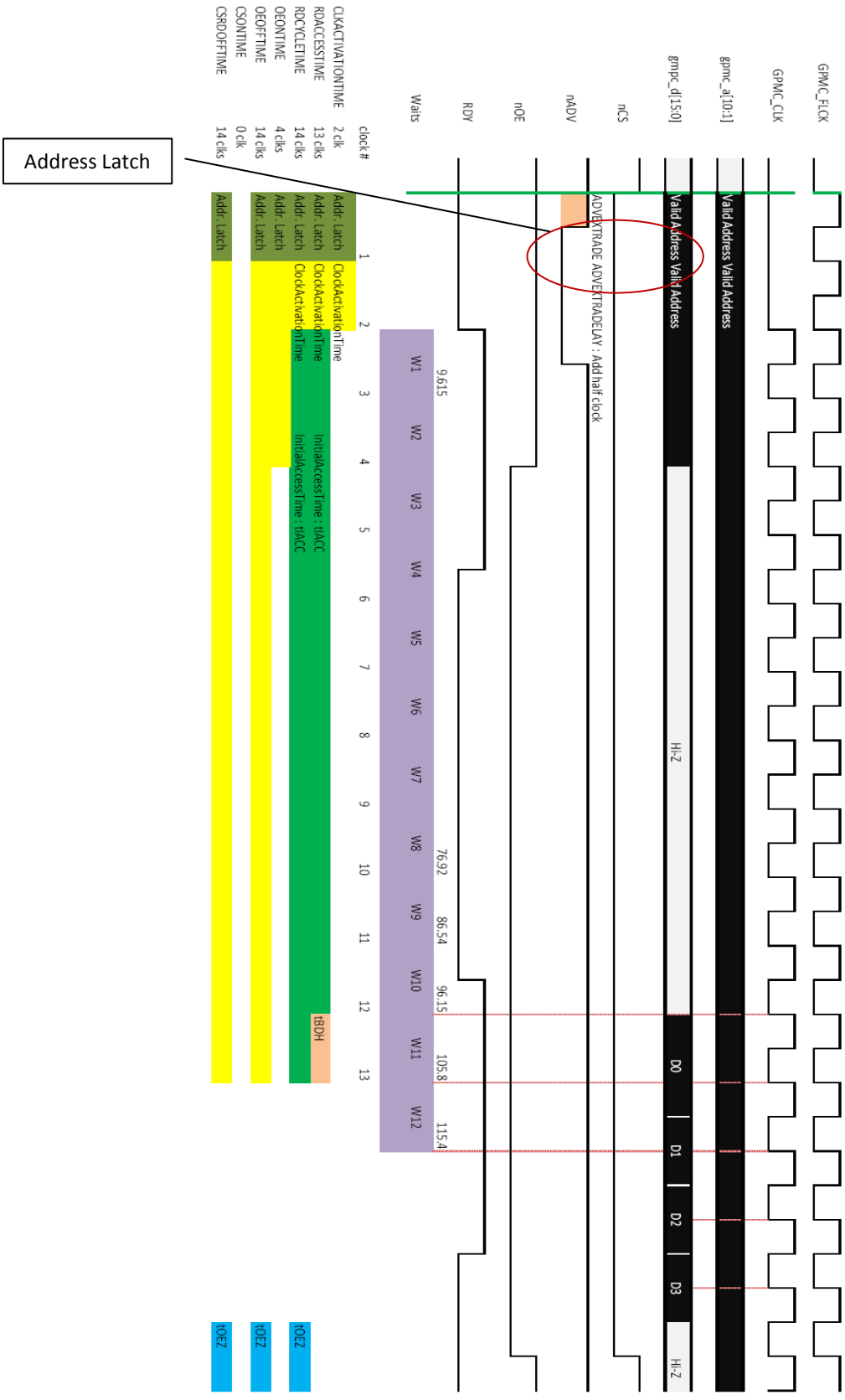

Figure 31. WS-P Synchronous Read Waveform Generation

Intentionally Blank

Using Spansion Flash with TI Sitara™

– AM3517 based