4.3.4 HyperLink Net Classes & Specific Rules

Routing requirements for the HyperLink (if implemented) bus shall follow standard microwave design and routing guidelines. Specific attention shall be paid to net classes within this group and should have the highest routing priority. The HyperLink bus is intended for DSP to DSP connectivity only.

- Each differential receive pair shall be individually skew matched to within 1 pS (absolute maximum). 1 pS equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). An example of a differential pair is MCMRXN0 & MCMRXP0.
- All differential receive pairs shall be routed on the same layer.
- ~~Each complementary transmit pair shall be individually skew matched to within 5 pS (absolute maximum). 1 pS equates to equates to approximately 5.464 mils to 7.092 mils (depending on propagation delays). Example of complementary pairs include MCMTXN0 & MCMTXP0.~~
- Each differential transmit pair shall be individually skew matched to within 1 pS (absolute maximum). 1 pS equates to approximately 5.5 mils to 7.1 mils (depending on propagation delays). An example of a differential pair is MCMTXN0 & MCMTXP0.
- All differential transmit pairs shall be routed on the same layer.
- ~~All complementary receive pairs MCMRXN/P3:0 shall be assigned to an individual net class and routing skew shall not be greater than 5 pS (absolute maximum) between all receive pairs.~~
- All differential receive pairs MCMRXN/P3:0 shall be assigned to an individual net class and routing skew shall not be greater than 100 pS (absolute maximum) between all receive pairs.
- ~~All complementary transmit pairs MCMTXN/P3:0 shall be assigned to an individual net class and routing skew shall not be greater than 5 pS (absolute maximum) between all transmit pairs.~~
- All differential transmit pairs MCMTXN/P3:0 shall be assigned to an individual net class and routing skew shall not be greater than 100 pS (absolute maximum) between all transmit pairs.
- ~~All nets and net classes unless otherwise specified shall be < 3.0” (76.2 mm) in total length, recommended is 2.00” (50.8 mm).~~
- All differential pairs shall be < 4.0” (101.6 mm) in total length, recommended length is 2.00” (50.8 mm).
- ~~The MCMRXFLCLK & MCMRXFLDAT nets shall be skew matched within 5 pS (absolute maximum) of one another and within 6 pS of both MCMRXNn and MCMRXPn nets.~~
- The MCMRXFLCLK & MCMRXFLDAT nets shall be skew matched within 250 pS (absolute maximum) of one another.
- ~~The MCMTXFLCLK & MCMTXFLDAT nets shall be skew matched within 5 pS (absolute maximum) of one another and within 6 pS of both MCMRXNn and MCMRXPn nets.~~
- The MCMTXFLCLK & MCMTXFLDAT nets shall be skew matched within 250 pS (absolute maximum) of one another.

- ~~The MCMRXPMCLK & MCMRXPMDAT nets shall be skew matched within 5 pS (absolute maximum) of one another and within 6 pS of both MCMRXFLCLK and MCMRXFLDAT nets.~~
- The MCMRXPMCLK & MCMRXPMDAT nets shall be skew matched within 250 pS (absolute maximum) of one another.
- ~~The MCMTXPMCLK & MCMTXPMDAT nets shall be skew matched within 5 pS (absolute maximum) of one another and within 6 pS of both MCMTXNn and MCMTXPn nets.~~
- The MCMTXPMCLK & MCMTXPMDAT nets shall be skew matched within 250 pS (absolute maximum) of one another.
- Transmit and receive signals must be referenced to continuous, parallel ground planes.
- ~~No vias are allowed.~~
- Differential signal routing must achieve 100-ohm differential impedance.
- Routing shall take into account propagation delays between microstrip and strip line topologies.
- ~~Timing assumptions are based on a 80 pS period, 40 pS half-period time.~~
- To prevent crosstalk in a simple board stack-up, we recommend that the differential receive pairs be routed as microstrip (outer layer) on one side of the board and the differential transmit pairs be routed as microstrip (outer layer) on the other side of the board.
- Up to 2 vias are allowed but there must be no stub and the differential nature of the circuit must be maintained. This forces routing on the outer layers unless blind via technologies or back-drilling are used.
- If a via is implemented, an adjacent ground via will be implemented to minimize the discontinuity.
- HyperLink lanes can be swapped to simplify routing. The differential pairing must be maintained.
- P and N connections for a single differential pair can be inverted to simplify routing.
- The HyperLink interface is intended for DC coupled operation between two DSPs on a single board.

Board layout simulation is a requirement for this class of circuit to validate the PCB routing.