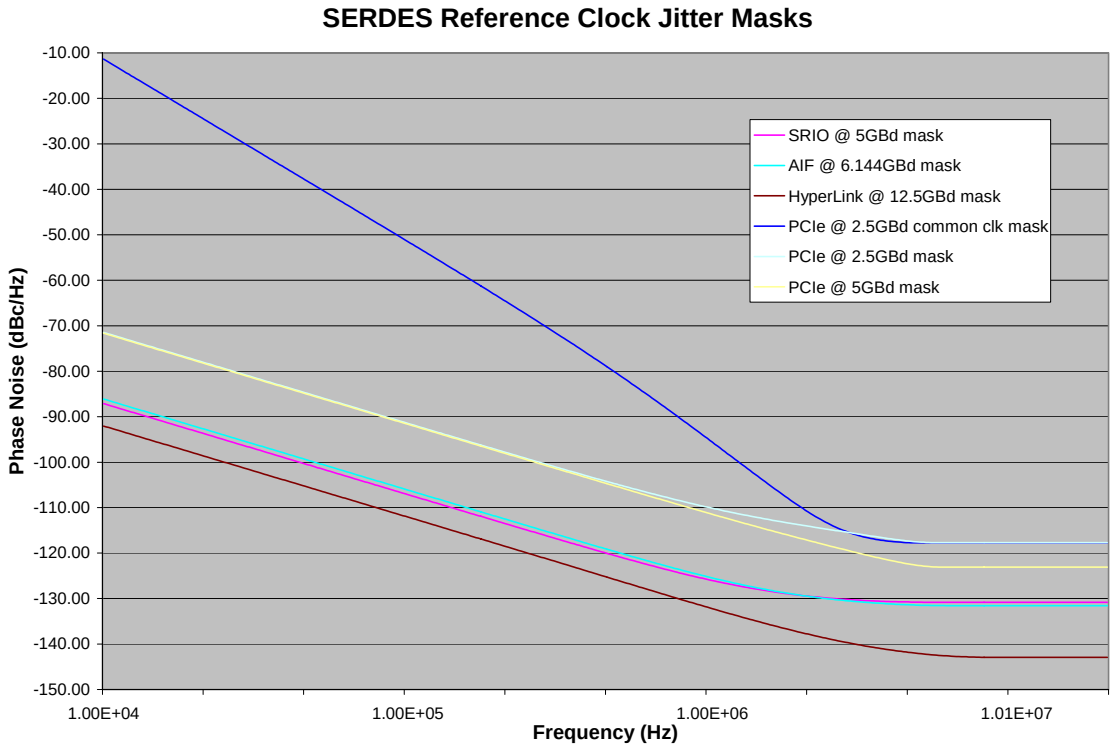
Reference Clock Jitter Requirements

KeyStone DSPs contain several high performance serial interfaces commonly known as SERDES interfaces. The SERDES architecture [in general] allows for reliable data transmission without a need for common synchronized clocks. However, they do require high quality clock sources that have very little phase noise. Phase noise is also commonly referred to as clock jitter.

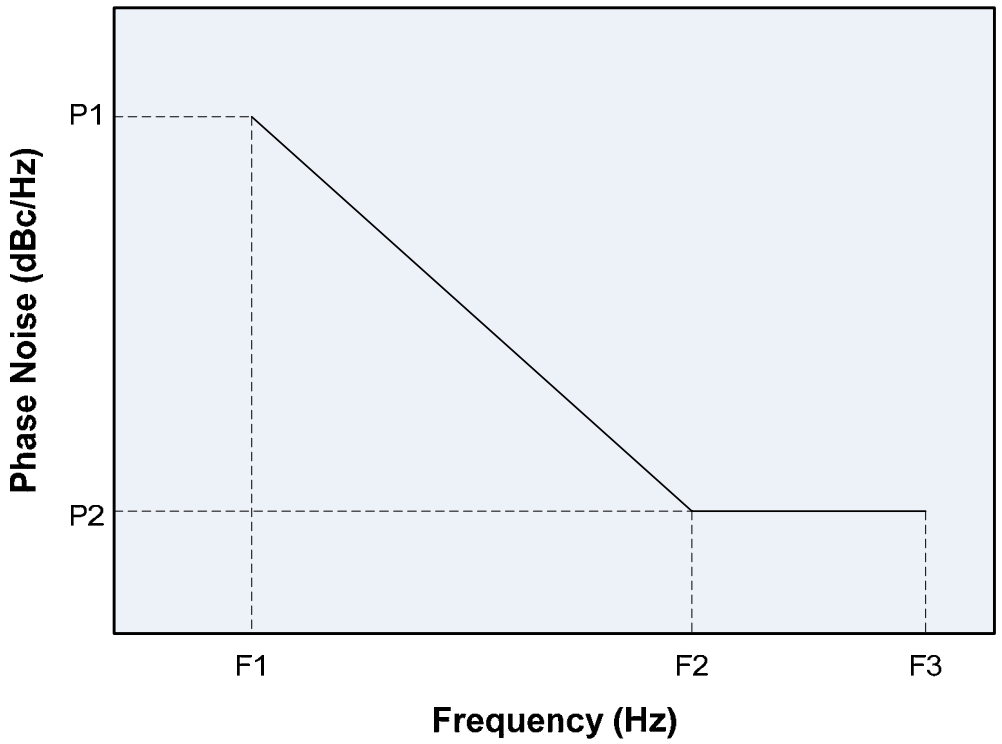
Please note that PCIe can be operated with a common clock and this allows use of spread spectrum clock sources that have higher levels of bounded phase noise. HyperLink is also defined as an interface requiring a common clock since it is expected to be a very short reach transmission between DSPs located on the same board.

Random Jitter

Phase noise amplitude is not the only concern. The frequency content of this phase noise is also significant. Therefore, masks are provided as a means of indicating an acceptable phase noise tolerance. Each SERDES interface has a slightly different mask. SERDES data rate, input clock rate and required bit error rate affect the phase noise tolerance. The following graph shows the basic phase jitter tolerance masks for the KeyStone SERDES interfaces. The mask shown is for the highest performance operating mode defined for each SERDES interface. Board designers must provide a reference clock that has clock jitter below the appropriate mask across the entire frequency range.



Since this graph will be difficult to use, we also provide this information as a straight-line approximation with the end points and the knee defined. This template is shown in the graph below and the endpoints in the table that follows. The mask level at specific frequencies can now be estimated based on the straight-line approximation. This is useful when comparing clock sources from various vendors who specify jitter masks in different ways.



Interface & Rate (GBd)	Reference Clock Frequency (MHz)	BER Rate	F1 (Hz)	P1 (dBc/Hz)	F2 (Hz)	P2 (dBc/Hz)	F3 (Hz)
SRIO @ 5	250	1e-15	10K	-87.1	1.56M	-130.8	20M
AIF @ 6.144	256	1e-12	10K	-86.1	1.91M	-131.6	20M
HyperLink @ 12.5	250	1e-17	10K	-92.1	3.43M	-142.9	20M
PCIe @ 2.5	250 (common)	1e-12	10K	-11.4	2.96M	-117.7	20M
PCIe @ 2.5	250	1e-12	10K	-71.5	2.18M	-117.7	20M
PCIe @ 5	250	1e-12	10K	-71.7	3.76M	-123.1	20M

A single value is also commonly provided as the limit for phase noise. This is an integration of the phase noise across a frequency range. The next table shows the integrated value for each of the phase noise masks across the 10KHz to 20MHz frequency range and across the 1MHz to 20MHz frequency range. These limits are also useful for evaluating high performance clocks sources from some vendors.

Interface & Rate (GBd)	Reference Clock Frequency (MHz)	BER Rate	Rj (ps) 10KHz to 20MHz	Rj (ps) 1MHz to 20MHz
SRIO @ 5	250	1e-15	4.12	1.17
AIF @ 6.144	256	1e-12	4.56	1.09
HyperLink @ 12.5	250	1e-17	2.26	0.33
PCIe @ 2.5	250 (common)	1e-12	14030	8.99
PCIe @ 2.5	250	1e-12	24.59	5.62
PCIe @ 5	250	1e-12	23.65	3.37

Please note that not all clock sources with jitter values below the single values shown in the preceding table will meet the templates shown above. These figures were generated assuming that the reference clock spectrum is shaped in the same manner as the template. Further verification may be needed.

All of the masks shown above assume the input clock rate is about 250MHz. The input clock rate affects the phase noise tolerance. This is because the reference clock phase noise is multiplied within the SERDES PLL. Higher levels of phase noise can be tolerated if the input reference clock rate is higher. The entire mask shifts proportional to the frequency difference. This mask offset is approximated by the equation 20*log(F2/F1). The integrated phase noise value also shifts by the same ratio. It is approximated by the equation F2/F1. Since all of the masks shown above are for 250MHz reference clocks, the mask and phase noise adjustments from 250 MHz are shown in the following table.

Reference Clock Frequency	Phase Noise Mask Offset	Rj Multiplier
100 MHz*	-8.0 dB	0.40
122.88 MHz	-6.2 dB	0.49
153.60 MHz	-4.2 dB	0.61
156.25 MHz	-4.1 dB	0.63
250 MHz	0.0 dB	1.00
312.5 MHz	1.9 dB	1.25

(* Only supported for PCIe)

The phase noise masks provided are at the maximum supported data rates for SRIO, AIF and HyperLink. Additional phase noise margin is gained when the data rate is reduced. This is because the margin for jitter increases as the data eye gets longer when the data rate decreases. Once again, the mask offset is approximated by the equation 20*log(F2/F1) and the integrated phase noise value is approximated by the equation F2/F1. The following table shows the mask and phase noise adjustments for the available SRIO operating rates. Similar numbers can be computed for AIF and HyperLink. Please note that this does not apply for PCIe. The phase noise masks are defined within the PCIe specification and the masks converge at low frequency regardless of data rate as shown in the figure above.

SERDES Data Rate	**Phase Noise Mask Offset**	**Rj Multiplier**
5 GBd	0.00 dB	1.00
3.125 GBd	4.08 dB	1.60
2.5 GBd	6.02 dB	2.00
1.25 GBd	12.04 dB	4.00

Deterministic Jitter

Reference clock sources may also contain deterministic jitter in the form of spurs that must also be accounted for . The effects of spurs varies depending upon whether they are correlated or uncorrelated. An exact determination of the effects of the spurs would be very complicated. (There are published papers concerning the complexities of combining the noise power of spurs.) A simplified formula is shown below.

$$Jitter_{spurs} = \frac{2}{2 \cdot pi \cdot F_{reference}} \sqrt{\sum_{1}^{N} 10^{\frac{Spurs_N\,(dBc)}{10}}} \leq 0.1ps$$

The limit of 0.1ps is a level chosen to provide a reasonable margin without complex analysis. This equation has sufficient margin to be used for all interface types and baud rates.