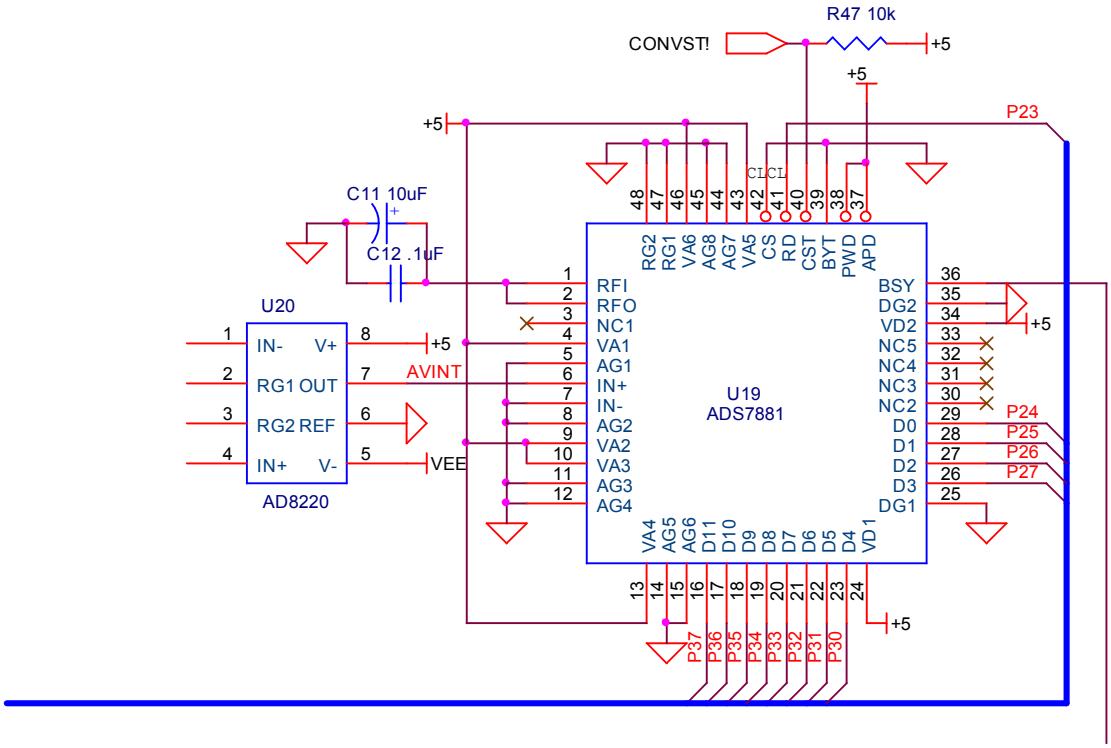
olaney@gmail.com



We have a problem reading data from this converter – we get all ones, which is the default state for the data bus because it has weak pull-ups. As you can see, CS! Is tied low, so that asserting RD! should put data on the bus, but apparently the chip disagrees. We know it is cycling because BY goes high during the conversion. Have I missed something here or should I look elsewhere?