

Understanding the ADC Input on the MSC12xx

Russell Anderson
Data Acquisition Products

ABSTRACT

The analog inputs of the MSC12xx are sampled continuously. This sampling process creates an effective input impedance that varies with sampling frequency and the gain selected. In addition to the input sampling, there is also a second sampling for the output data rate. Both of the sampling frequencies can create aliasing. If anti-aliasing filters are included, care must be observed that the inputs are driven correctly; otherwise, additional errors of offset, noise and drift will be created. This application note discusses concerns about the input impedance, usage of the buffer and limitations which must be observed when driving the inputs. Using the buffer improves the input impedance, but limits the input voltage range.

Contents

1	Introduction	3
2	Drive Limitations	3
3	Signal Range (Buffer Off)	3
4	Using the Buffer	4
5	Differential vs. Single-Ended	4
6	ADC Sampled Input.....	5
7	Sinc Filter Response.....	7
8	Anti-Aliasing	8
9	Output Sample Aliasing.....	9
10	Input Filter Concerns	10
11	Input Impedance.....	12
12	Offset Drift	13
13	Driving the Reference	13
14	Summary.....	13
	References.....	14

Figures

Figure 1.	Measuring 5V Signal with 2.5V Reference	4
Figure 2.	Measuring 5V Signal with 5V Reference	5
Figure 3.	MSC12xx Input.....	5
Figure 4.	Sinc Filter Responses.....	7
Figure 5.	Sinc Filter Response.....	8
Figure 6.	Filters for Aliased Signals	8
Figure 7.	Filtering and Low Decimation Ratio	9
Figure 8.	Anti-Alias 1/3Hz Filter	9
Figure 9.	Second-Order Sallen-Key 1/3HZ Filter	10
Figure 10.	Residual Currents with Buffer.....	11
Figure 11.	Source Impedance	12

1 Introduction

The delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC) included in the MSC12xx family of devices has a sampled input which must be correctly understood in order to achieve the desired measurement results. The actual input impedance is a function of sampling speed and Programmable Gain Amplifier (PGA) settings. Input circuitry that drives this input impedance must be carefully designed to assure that data accuracy is preserved. In addition, further caution must be taken to ensure that the input fully settles between each sample; otherwise, there will be additional offset introduced into the measurement.

2 Drive Limitations

Before we can determine how to drive the ADC inputs, we need to evaluate four requirements of the input signal.

1. Does the signal range allow buffering?
2. Is the input differential or single-ended?
3. What is the signal frequency?
4. What accuracy and resolution are needed?

3 Signal Range (Buffer Off)

The analog input signals for the MSC12xx products can range from 0.5V below AGND to 0.5V above AV_{DD} . The ADC measures the differential signal between the two selected analog input pins. It does not matter what the common-mode voltages are on the input pins, as long as they are within the input signal range. With $A_{IN+} = +1.5V$ and $A_{IN-} = 0V$, one will observe the same reading as that taken when $A_{IN+} = +5V$ and $A_{IN-} = +3.5V$. The voltage potential between REF_{IN+} and REF_{IN-} sets the full-scale voltage of $(REF_{IN+} - REF_{IN-}) / PGA$.

The digital output can be selected to be either unipolar or bipolar. In unipolar mode, the input voltage V_{IN+} needs to always be a positive voltage between AGND and V_{REF} ($REF_{IN+} - REF_{IN-}$) and greater than V_{IN-} . For a bipolar input, the A_{IN+} input can be either below or above the A_{IN-} input by (V_{REF}). This capability means that in unipolar mode, using a 2.5V reference, the unipolar signal would be from 0 to +2.5V; in bipolar mode, the range would be from -2.5V to +2.5V, or a 5V span. Since both results use all 24 bits to represent the range of possible values, the unipolar least significant bit (LSB) is one-half the size of the bipolar LSB. In other words, the ADC has twice the resolution when the voltage range is selected to be unipolar. Any negative input samples when using the unipolar mode will have a converted value of all zeros.

4 Using the Buffer

To maintain a high input impedance (for changes in sampling frequency and PGA) the input buffer can be enabled. The buffer will minimize errors from impedance mismatches. There are four drawbacks to using the buffer:

- It increases the analog power
- It has a limited input voltage range
- It is impossible to perform a gain calibration when REF IN+ is greater than $AV_{DD} - 1.5V$
- It increases the noise

Whereas non-buffered inputs can have signals that range beyond AGND to AV_{DD} , buffered analog inputs can only range from 50mV above ground to 1.5V below the AV_{DD} supply voltage. This range limitation is not a problem for many measurements, such as bridge measurements, but if the input node voltage exceeds these limits, the measurement will be incorrect.

5 Differential vs. Single-Ended

Many times, it is desirable to measure a 0 to 5V single-ended signal. The maximum internal reference voltage is 2.5V. By connecting the 2.5V reference voltage to the negative analog input (as shown in Figure 1) and the applying the input voltage from AGND to AIN+, the full range in the bipolar mode can go from 0V to 5V. The positive input is never more than 2.5V from the negative input. However, the output code will be in a two's complement representation that will show **-2.5V** for the 0V input and **+2.5V** for +5V input. This can be converted to 0 to 5V by adding 2.5V to all readings; alternatively, the most significant bit (MSB) can be inverted, and the values read as an unsigned 24-bit number.

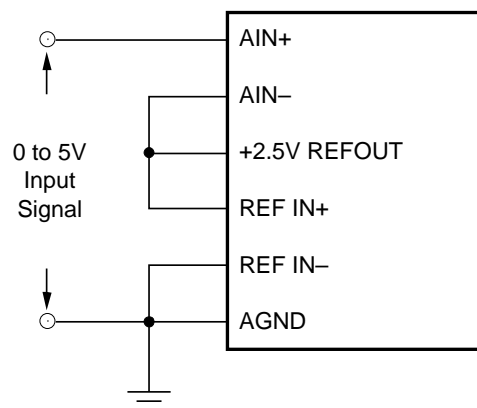


Figure 1. Measuring 5V Signal with 2.5V Reference

Figure 2 shows how it possible to use an external 5V reference, and then set up the ADC for the unipolar mode and measure zero to 5V signals. The INL is not as good when using a 5V reference.

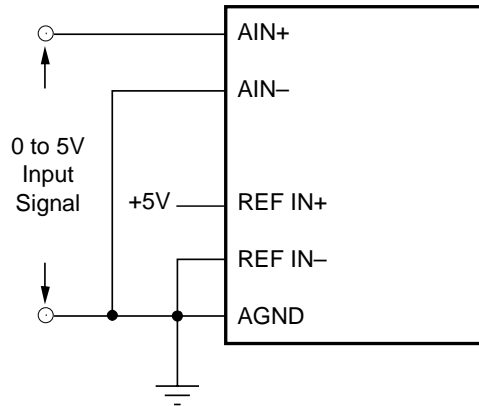


Figure 2. Measuring 5V Signal with 5V Reference

6 ADC Sampled Input

A delta-sigma converter continuously samples its input signal. This approach to data conversion is unlike a SAR converter, which only samples the input when signaled to initiate a conversion. The delta-sigma converter always samples the input, and then filters those signals into a periodic output. The ratio of the sampling speed and the output data rate is set by the decimation ratio. Figure 3 shows a representation of the input for the MSC12xx when it is not buffered.

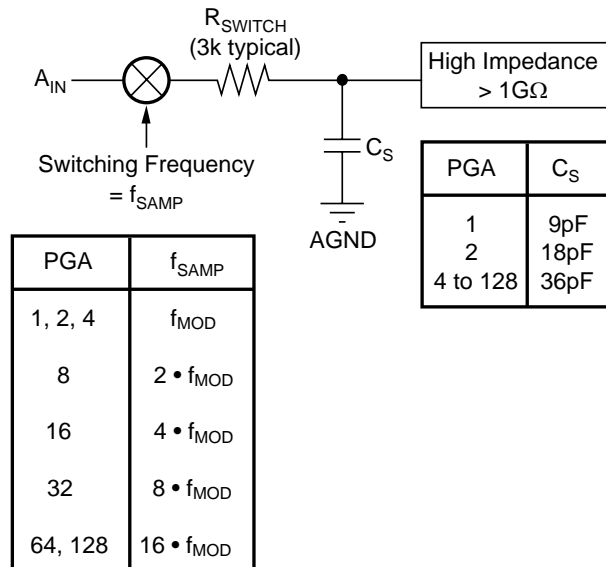


Figure 3. MSC12xx Input

As can be seen in Figure 3, the impedance of the analog inputs is a combination of the modulation clock and the PGA selection. The PGA is adjusted by changing the sampling frequency and the sampling capacitors. Therefore, the PGA setting will also affect the input impedance.

Inputs that sample and store charge on an internal capacitor appear to be resistive. The magnitude of the resistance is determined by the size of the sampling capacitor and the sampling frequency. (See Equation 1 and Equation 2.)

$$R = \frac{V}{I} = \frac{V}{\frac{Q}{t}} = \frac{V}{Qf} = \frac{V}{CVf} = \frac{1}{Cf} \quad (1)$$

$$A_{IN} \text{ impedance} = \frac{1}{C_S \cdot f_{SAMP}} \quad (2)$$

The modulation clock frequency (f_{MOD}) is defined in the following equation, using the value of the ACLK register and the MSC clock frequency, f_{OSC} :

$$f_{MOD} = \frac{f_{OSC} / (ACLK + 1)}{64} \quad (3)$$

For PGA settings of 1, 2 and 4, the sample frequency is equal to the modulation clock frequency. For higher PGA settings, the sampling frequency doubles for each increase in PGA gain, until a maximum of 16 times modulation frequency is reached.

For a sampling frequency of 15.625 kHz (and PGA = 1), the input impedance is 7.1MΩ. In general, the impedance can be described as follows. For a gain of 128, there is a change in a feedback capacitance that doubles the gain without any change of the input impedance. So, for PGA = 128, one would use a value of 64 in the following equations:

$$A_{IN} \text{ impedance} = \left(\frac{1\text{MHz}}{\text{clock} / (ACLK + 1)} \right) \cdot \left(\frac{7.1\text{M}\Omega}{\text{PGA}} \right) \quad (4)$$

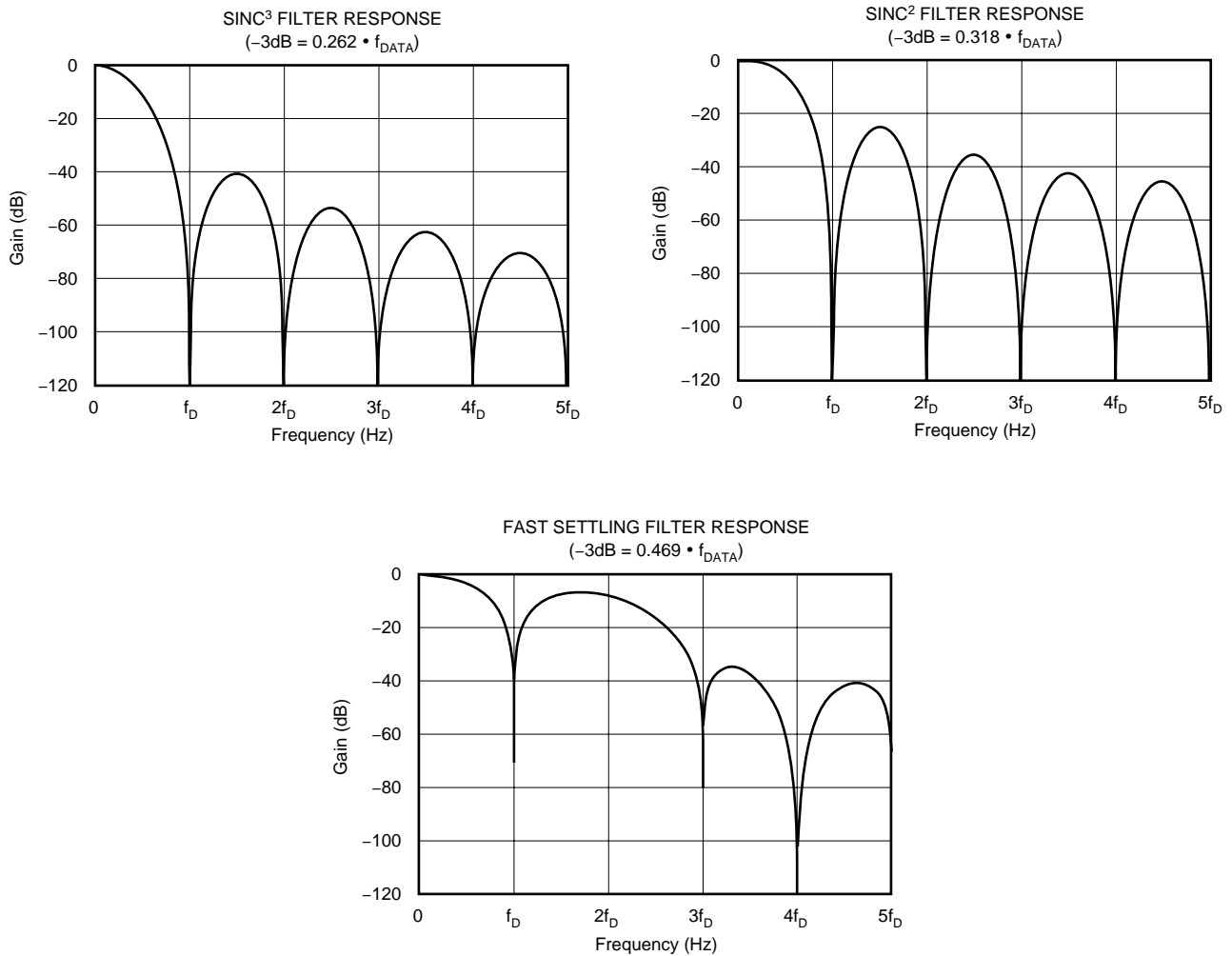
For the MSC1210, $clock = f_{OSC}$; for the MSC1211 and MSC1212, $clock = f_{CLK}$.

As can be seen, the actual sampling frequency is determined by the clock frequency (clock), the ACLK register and PGA setting. High sampling frequencies and high PGA values will yield a low input impedance. For example, at a PGA of 64 or 128, the impedance is 64 times lower than for a PGA of 1 at the same f_{MOD} rate. This means that the impedance would be reduced from 7.1MΩ to 110kΩ ($f_{MOD} = 15.625$ kHz).

7 Sinc Filter Response

After the input is sampled, it is filtered and decimated to achieve a high-resolution result. The Sinc filter has a deep notch at the sample frequency and multiples of the sample frequency. (See Figure 4.) That notch can be used effectively to remove unwanted signals. For example, the 60Hz signal could be eliminated by using an output data rate of 60Hz. If it was desired to eliminate both 50Hz and 60Hz, then a data output rate of 10Hz could be used. The Sinc filter has a roll-off in the frequency response that reduces the amplitude of signals that are close to the data rate.

The primary use for Sinc filter converters is to measure very low frequency (approximately DC) signals. Depending on the desired performance, three filters are available on the MSC12xx devices: Sinc³, Sinc² and Fast Settling, as shown in Figure 4.



NOTE: f_D = Data Output Rate = 1/t_{DATA}

Figure 4. Sinc Filter Responses

8 Anti-Aliasing

As with any sampled data system, care should be taken that spurious signals and noise do not alias into the desired measurement signal band. Figure 5 shows the aliasing that will occur around the sampling frequency given a data rate of 60Hz and a sampling frequency of 14,400kHz. Therefore, a decimation ratio of 240 is achieved. As seen in Figure 5, the Sinc filter response is duplicated around the sample frequency and multiples of the sampling frequency.

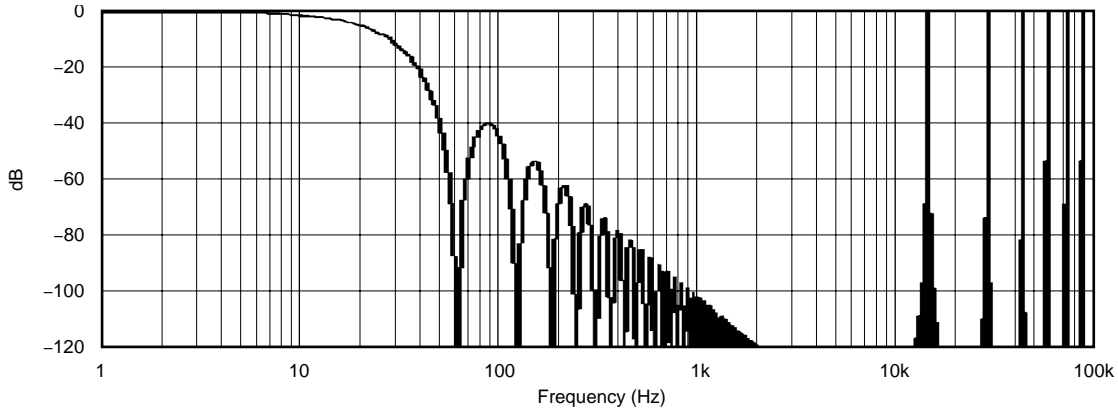


Figure 5. Sinc Filter Response

An analog filter can be used to eliminate the signals that can come from aliasing around the sample frequency. Using a 10Hz pass-band filter, the effectiveness of a 1- or 2-pole filter is plotted in Figure 6.

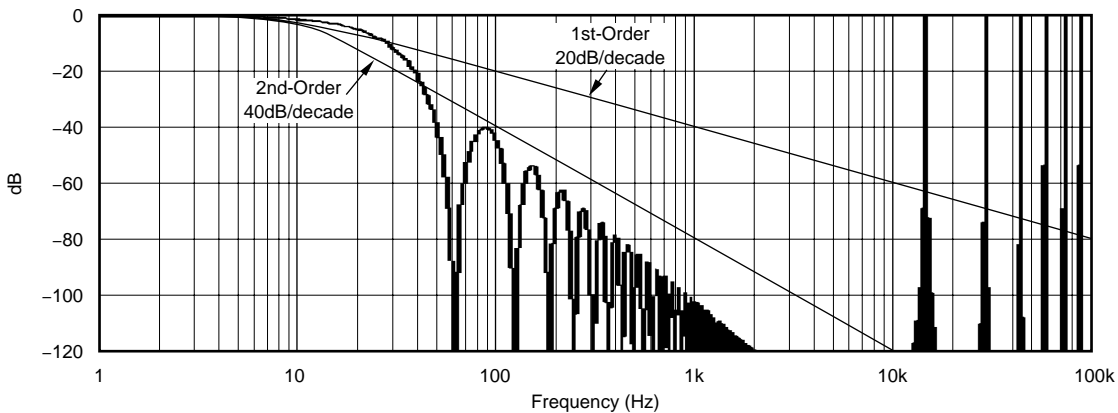


Figure 6. Filters for Aliased Signals

Although this shows that a second-order filter will work effectively to eliminate the aliased signals that occur at the sample rate, changing the decimation ratio could also change this effect significantly. Figure 7 shows the same data rate of 60Hz with a decimation ratio of 24.

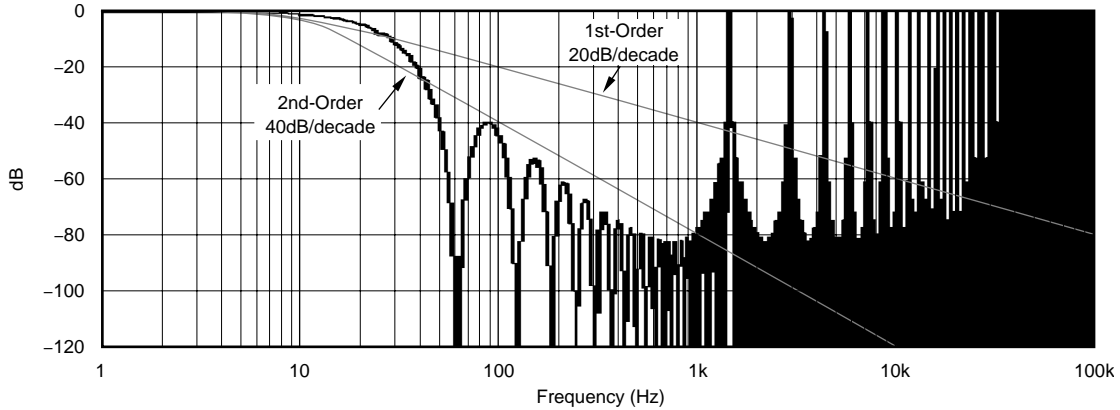


Figure 7. Filtering and Low Decimation Ratio

However, aliasing that can occur because of the sampling frequency may not be the primary concern. The output sample frequency can also cause aliasing.

9 Output Sample Aliasing

With a Sinc filter delta-sigma converter, there are actually two sample frequencies that can cause aliasing; one is the sampling frequency and the other is the data output frequency. Any signals that are greater than one-half the data output frequency can be aliased into the lower frequencies. With a data output rate of 60Hz, a signal of 35Hz would be attenuated by 16.7dB before it aliased at 25Hz.

We can add a filter to deal with these aliased signals as shown in Figures 8 and 9.

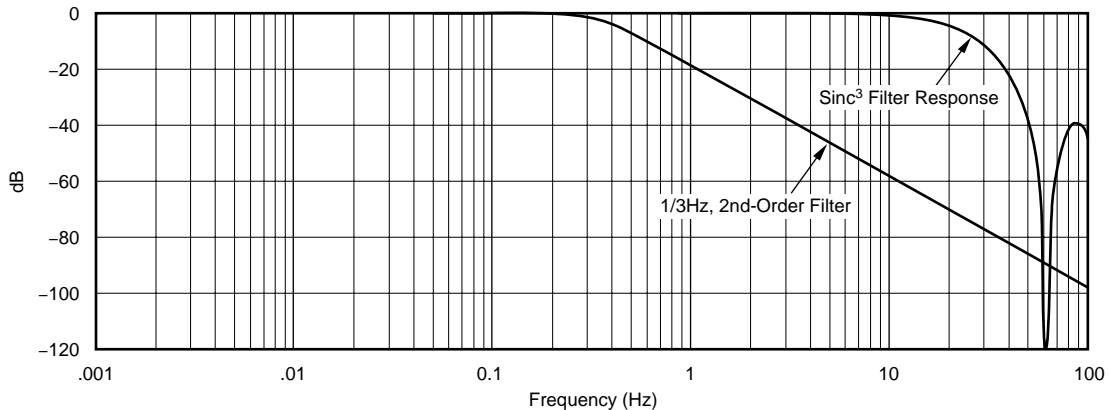


Figure 8. Anti-Alias 1/3Hz Filter

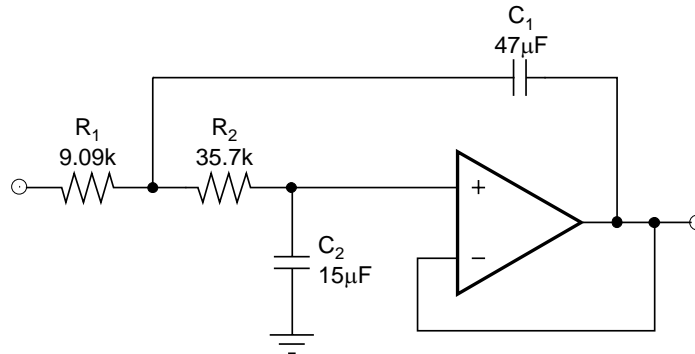


Figure 9. Second-Order Sallen-Key 1/3HZ Filter

This 1/3Hz filter does not eliminate all the aliasing signals. Quite often, though, one does not need to mathematically eliminate all possibilities for aliased signals with an anti-alias filter. It will depend on the user's system and signal source. For example, if one measures temperature, one can be assured that the temperature will not change faster than the environment will allow. With the second-order filter used in Figure 8, the attenuation for a 35Hz signal will be almost 80dB. This result, in combination with the Sinc3 filter response, gives a total attenuation of over 95dB. This 95dB attenuation will reduce a full-scale signal by 95dB. But it is seldom that the aliased signal will be a full-scale signal. If the aliased signals are already 20dB below full-scale, then the total attenuation would be 115dB.

10 Input Filter Concerns

It would seem that to eliminate aliased signals, we simply need to add a filter to the analog inputs of the delta-sigma converter. However, there are limitations to this approach. An R-C circuit on the input can have the unexpected result of giving an offset error to the measurement when working without the internal buffer. The main problem with this effect is that the sampling process at the input pulls a small quantity of charge from the input filter capacitor, which must be restored before the next sample is taken. The time constant of the driving input has to be such that the charge can be fully restored to the desired accuracy. Table 1 shows that in a high-resolution system—that is, one with a resolution of 20 bits or greater—it will take over 14 time constants before achieving the desired accuracy. Of course, a full 24 bits would even require more time (over 17 time constants). If the charge is not fully restored, one has the effect of a constant charging current through the resistance portion of the R-C filter, which produces a voltage drop and creates an observed offset error.

N	2 ^N	Time Constants to 1/2LSB
8	256	6.24
10	1024	7.62
12	4096	9.01
14	16384	10.40
16	65536	11.78
18	262144	13.17
20	1048576	14.56
22	4194304	15.94
24	16777216	17.33
26	67108864	18.71

Table 1. Settling to 1/2LSB

Figure 10 shows the type of offset voltages that are introduced when there is not enough time allowed for the capacitor on the input to be fully charged. A sample of charge is taken from the 470pF capacitor to charge the internal sampling capacitor. There is insufficient time for that charge to be fully restored before the next sample is taken. This condition creates the effect of a constant charging current, which leads to a voltage drop across the input resistors and, therefore, an offset error in the measurement.

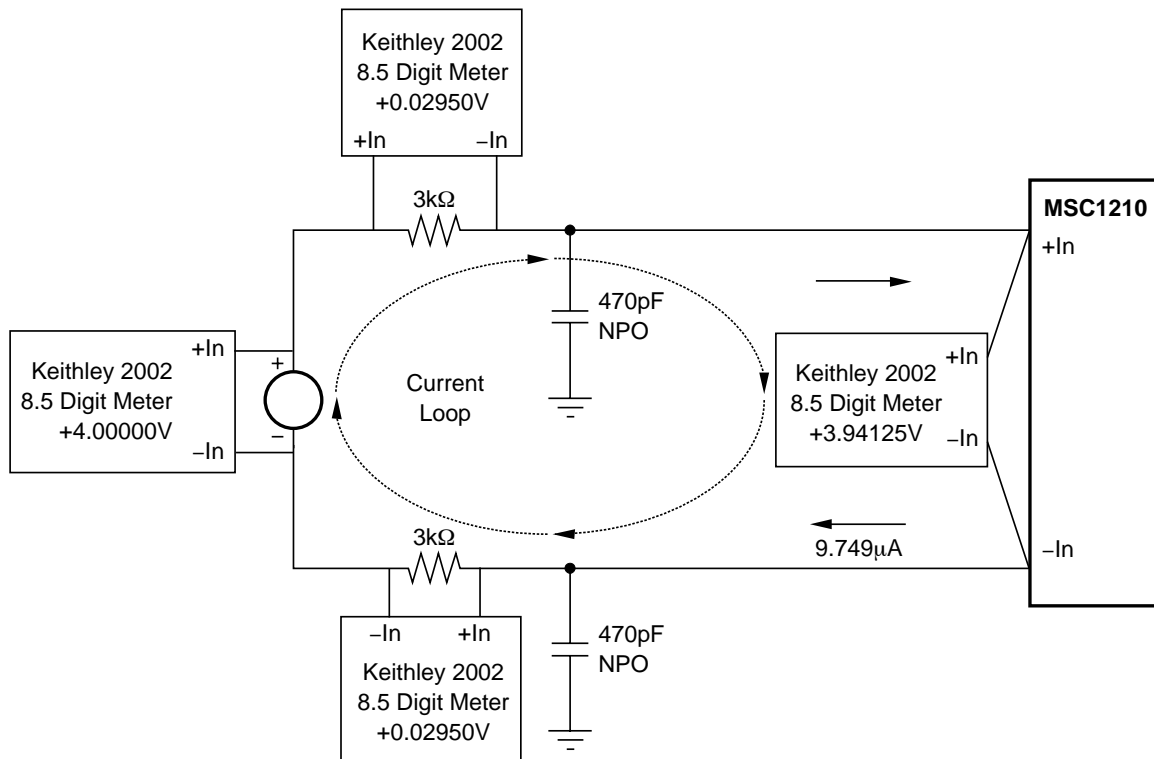


Figure 10. Residual Currents with Buffer

The types of offsets that are observed here are eliminated by enabling the internal buffer. With the buffer enabled, the input impedance is much higher and the charging currents are greatly reduced. Enabling the input buffer simplifies the driving of the input for better accuracy, although it will increase the noise by approximately 25% for a low PGA. With the buffer enabled, the inputs are still sampled as part of the chopper-stabilized circuit. This chopper, however, uses very small parasitic capacitances, which increase the impedance significantly.

11 Input Impedance

In the unbuffered mode, as shown in Figure 11, whatever impedance that may be driving the input will increase the time constant for driving the sampling capacitor as well. That may not be critical unless there is also an external capacitor, C_{EXT} , on the input. Care must be taken that such a capacitor does not cause a loss in accuracy. It might be impractical to have a capacitor from the A_{IN} pin to ground to be used for an anti-aliasing filter. C_{EXT} could be large enough so that charging C_S would change the input voltage by less than 1LSB. For 20 bits, that would require C_{EXT} to be greater than $9\mu\text{F}$. (See Equation 5.)

$$C_{EXT} = 2^{20} \cdot 9\text{pF} = 9.4\mu \quad (5)$$

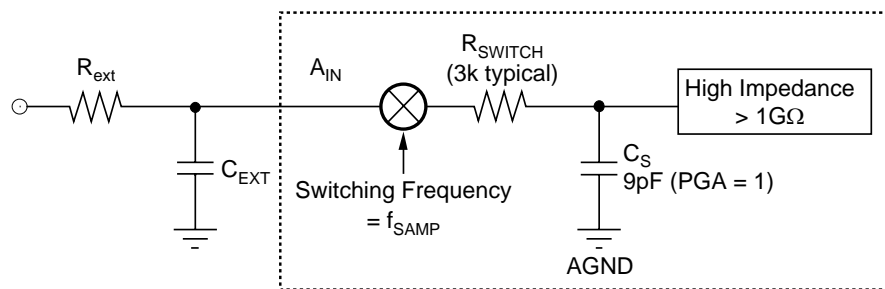


Figure 11. Source Impedance

But even with a large capacitance, the time constant would still need to be fast enough to fully charge the capacitor to the required accuracy (that is, 14 time constants for 20 bits of resolution). Otherwise, the small charges that are removed could eventually have an impact that will be larger than 1LSB.

Alternately, C_{EXT} could be small enough so the time constant of $R_{EXT}C_{EXT}$ would allow the charge on C_{EXT} to be restored before the next sample. But with a small C_{EXT} , the cutoff frequency for $R_{EXT}C_{EXT}$ would not be low enough to be used as an anti-aliasing filter.

Looking at the number of time constants needed in order for the driving R-C circuit to settle will set the limit on the amount of filtering or sample frequency. For example, from Table 1, we can see that if we desire 20-bit resolution, it will take 14.5 time constants to settle to within $\frac{1}{2}$ LSB. It is obvious that a 1/3Hz filter will not be able to settle to 14.5 time constants in the sample time of 15 kHz. One solution may be to add an op amp follower after the anti-aliasing filter, to supply the sampling currents needed. But if the anti-aliasing filter is buffered, then we have added the noise, offset and drift of that amplifier into our signal path.

A better approach would be to enable the on-chip input buffer to greatly reduce the amount of charging current required.

If an external R_{EXT} and C_{EXT} are used, the capacitor should be a high quality component, with low non-linearities and dielectric absorption.

The two R-C circuits on a differential input must be perfectly matched or the response to a common mode signal will appear as a differential signal. To help alleviate this problem, a differential capacitor should be added that is at least 100 times larger than the capacitors to ground. [1]

12 Offset Drift

The analog input of the MSC12xx has a chopper-stabilized circuit design to greatly reduce low frequency drift or $1/f$ noise. If an amplifier is used to drive the inputs, then the overall drift of the system might be adversely affected.

Any time additional active circuits are included, one must be sure that in the process of solving one problem that a second problem (that is harder to compensate for) is not introduced. Whereas the offset and gain errors of the internal amplifier can be calibrated out, this approach is not as easily done for an external amplifier. For offset calibration, a zero signal will have to be switched into the input, and an additional conversion made. The value of that additional conversion would then be saved, and used to remove the offset from future measurements.

13 Driving the Reference

The reference input is similar to the unbuffered analog input. To ensure that the analog input is fully settled, we must have either a very large capacitor on the input or a fast amplifier so that the input will be stable and settled for each sample. The reference input is sampled on each sample clock, and must fully settle before the next sample is taken. Since the reference signal is a DC signal, a large capacitor can be used on that input. If an op amp is used to drive the input, care must be observed again that the op amp does not introduce new offset and drift errors.

14 Summary

The simplest solution that maintains low drift and high input impedance is to enable the on-chip buffer. This will raise the noise perceptibly, but the noise might be easier to address than precision errors from the driving circuits. If the signal range includes AGND, or is greater than 1.5V below AV_{DD} , then the non-buffered input must be used.

If the signal range requires avoiding the use of the buffer, then care must be observed to assure that the required accuracy is maintained and that any filters are fully settled. If amplifiers or buffers are required, this will have the effect of introducing additional offset and drift errors. The MSC12xx calibration options can correct internal offset and gain errors. System calibration must be used to correct offset and gain errors that will include the external amplifiers. This requires the capability to apply to the inputs either the zero or full-scale signal before the amplification. [2, 3]

References

1. Stitt, R.M. Input Filtering the INA117 \pm 200V Difference Amplifier. Application Note. (SBOA016)
2. Gurevich, M. ADC Offset in MSC12xx Devices. Application Note. (SBAA097A)
3. Gurevich, M. ADC Gain Calibration – Extending the ADC Input Range in the MSC12xx Devices. Application Note. (SBAA107)

To obtain a copy of the referenced documents, visit the Texas Instruments web site at www.ti.com.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265