ADC ADS7230 Test Results

VREF is tied to 4096 mV for 12-bit ADC, so the read result is supposed to follow the input

Channel 0		Channel 1	
Input (mV)	Read (mV)	Input (mV)	Read (mV)
0	1152	0	16
250	848	500	3840
500	560	1000	3600
750	288	1500	3568
1000	0	2000	3504
1250	3808	2500	3456
1500	3520	3000	3392
1750	3232	3500	3328
2000	2944	4000	3232
2250	2624	4500	4080

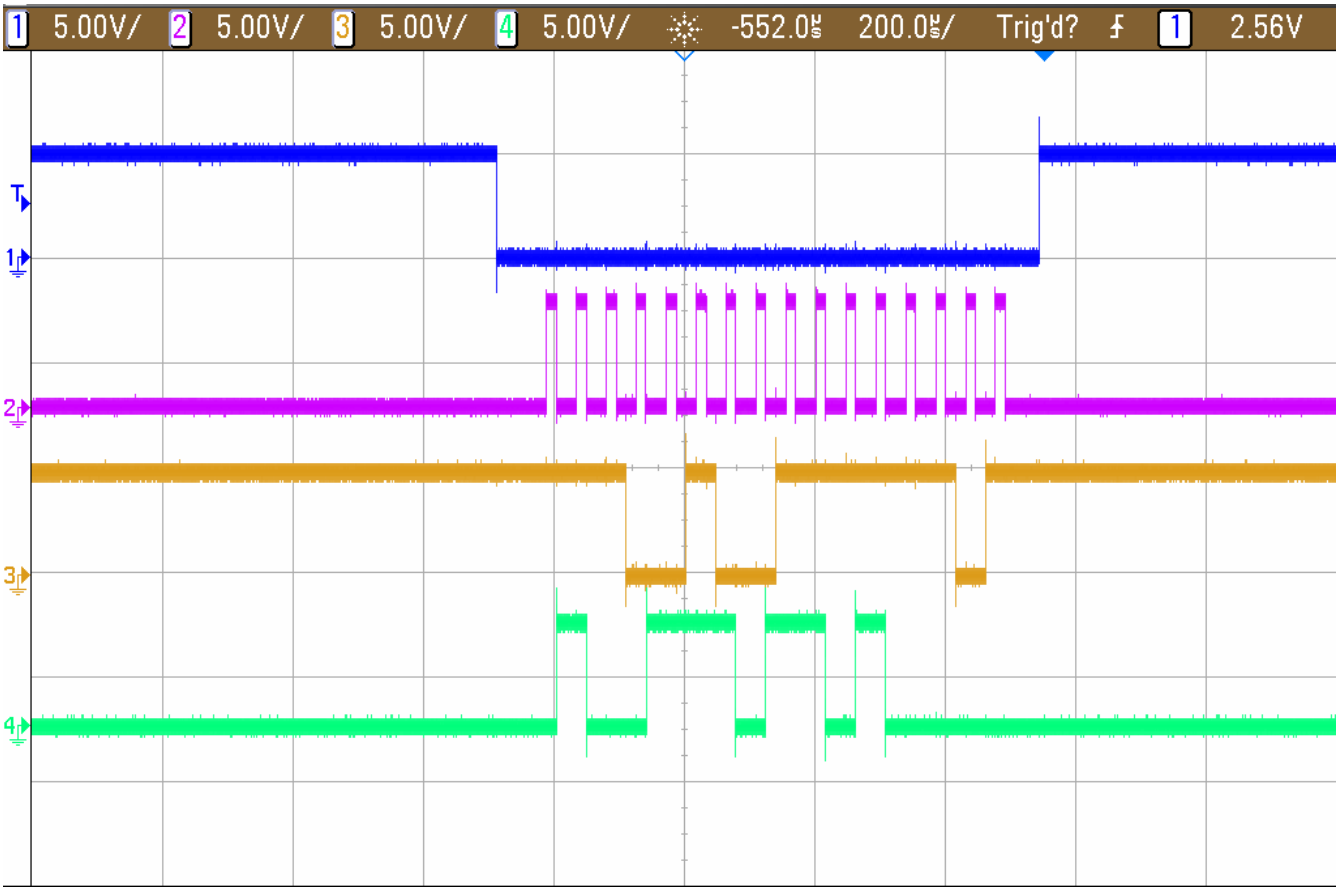
Init

1. Write 16-bit 0xE000 to reset the chip
2. Write 16-bit 0xE4FD for config data 0x4FD with : , verified by readback with exactly the same data written to ensure the right clock phase and polarity for SPI bus of the chip
    a. Manual Channel Select
    b. Internal Clock
    c. Auto Trigger
    d. No TAG bit
3. Read Result with 2 operations
    a. Write 4-bit channel number
    b. Write 4-bit read cmd 0xD and Read 12-bit result (repeat 4)
4. Read Result with 1 operation : write 4-bit channel number and read 12-bit result (repeat 4)

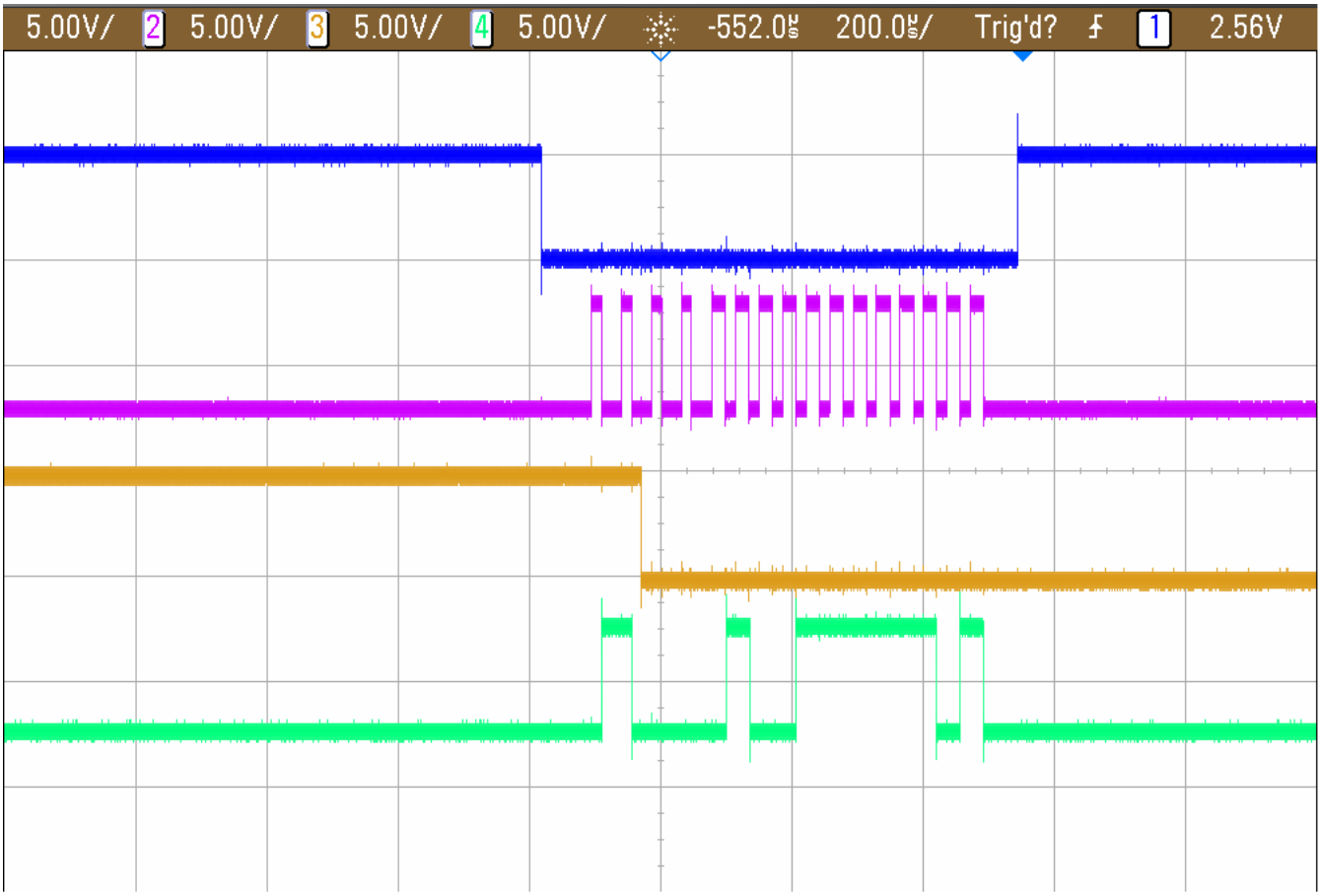
Both ways give almost identical results.

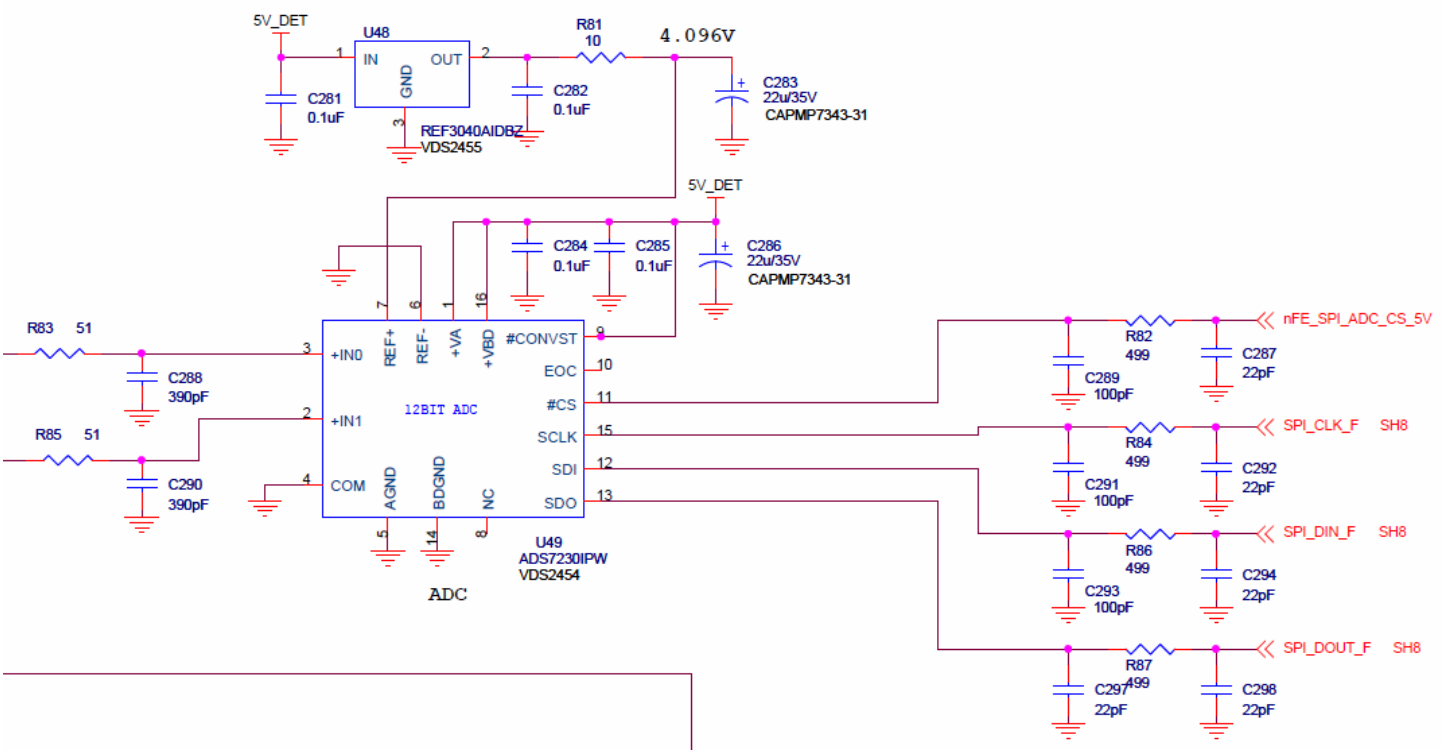
In read operation, the chip sends out at falling edge, so the host MCU must read at rising edge.

Set CFG : 0xE4FD



Get CFG : 0xC




5V_DET
U48
IN
GND
OUT
REF3040AIDBZ
VDS2455
C281
0.1uF
C282
0.1uF
R81
10
4.096V
C283
22u/35V
CAPMP7343-31
5V_DET
C284
0.1uF
C285
0.1uF
C286
22u/35V
CAPMP7343-31
R83 51
R85 51
C288
390pF
C290
390pF
+IN0
+IN1
COM
REF+
REF-
+VA
+VBD
AGND
BDGND
NC
#CONVST
EOC
#CS
SCLK
SDI
SDO
12BIT ADC
U49
ADS7230IPW
VDS2454
ADC
R82
499
C289
100pF
C287
22pF
nFE_SPI_ADC_CS_5V
R84
499
C291
100pF
C292
22pF
SPI_CLK_F SH8
R86
499
C293
100pF
C294
22pF
SPI_DIN_F SH8
R87
499
C297
22pF
C298
22pF
SPI_DOUT_F SH8