



Basics

1 - 1

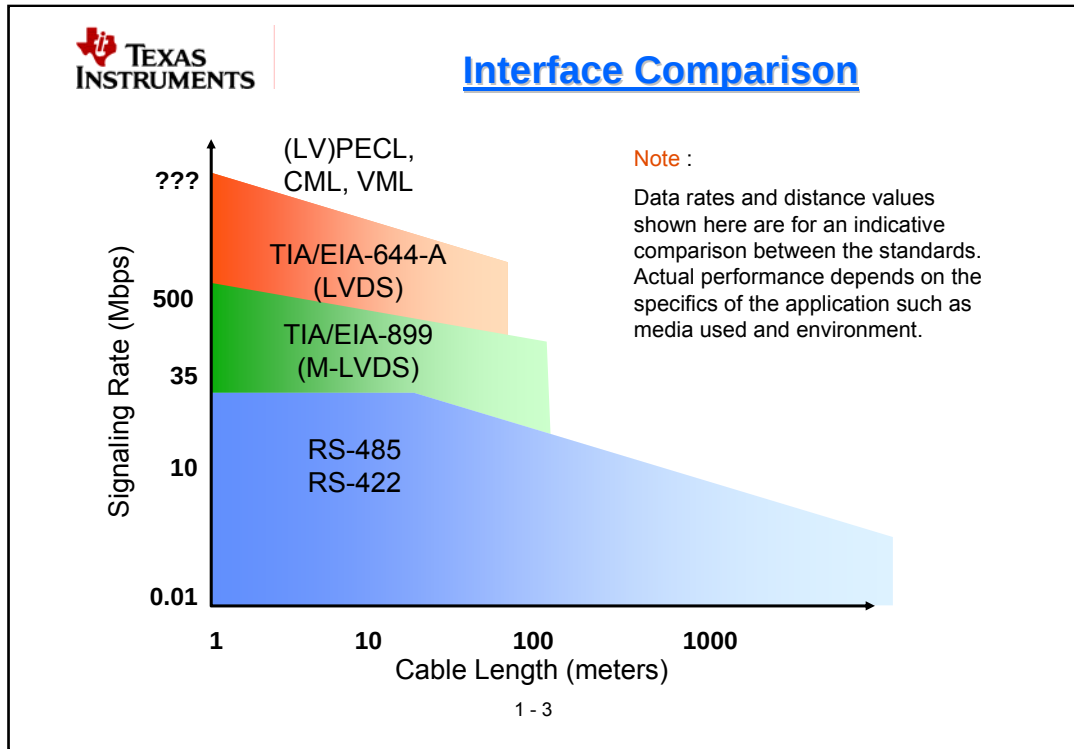


Basics Section Overview

- Single Ended vs. Differential
- Multidrop vs. Multipoint
- Transmission Line Theory
- Wave Analysis
- Line Reflections & Termination Practices
- Crosstalk
- Failsafe
- Tests associated with Signal Transmission
 - Electro Static Discharge (ESD)
 - Eye-Pattern
 - Inter Symbol Interference (ISI)
 - Bit Error Rate Testing (BERT)

1 - 2

This section repeats some of the basics we once learned at school, but may have neglected in the past, as they didn't apply to low-speed connections. Furthermore, some nomenclatures that may be used in different meanings are clarified, respectively the use within Texas Instruments and throughout this handbook. After repeating the transmission line theory briefly, we'll take a look at reflections and how to avoid them by proper terminations. Crosstalk is discussed as well as failsafe. Finally, test that are used to determine the robustness and signal integrity of devices and connections are introduced.



With many fields of applications, all having different requirements, many standards have been developed and many more are currently in the works. This seminar covers all of the above.

M-LVDS: Multipoint – Low Voltage Differential Signaling

LVDS: Low Voltage Differential Signaling

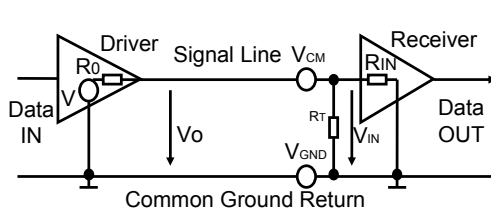
(LV)PECL: (Low Voltage) Pseudo Emitter Coupled Logic

CML: Current Mode Logic

VML: Voltage Mode Logic



Single-ended (Unbalanced) vs. Differential (Balanced)

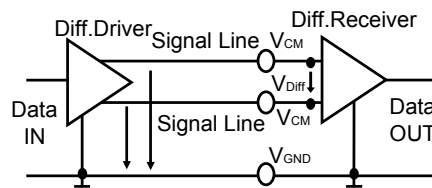


Advantages

- Low system cost
- Simple to implement

Disadvantages

- Noise and crosstalk
- Ground shifts
- Low data rates
- Low line length



Advantages

- Low sensitivity to crosstalk
- Ground noise rejection
- Common Mode noise rejection
- High Signaling Rates (>10Mbps)
- Long Line Length up to 1200m

Disadvantages

- Twisted Pair Cable required
- Higher Cost

1 - 4

The difference between single ended (or unbalanced) in comparison to differential (or balanced) transmissions is essential:

Single ended transmission is performed on one signal line, its output is interpreted with respect to ground. For simple, low speed interfaces, a common ground return path is sufficient, for more advanced interfaces a single return path for each signaling line (twisted pair cable) is recommended.

For balanced or differential transmission, a pair of cable is necessary for each channel. On one line, a “true” signal is transmitted, while on the second one, the inverted signal is transmitted. The receiver detects basically the sign of the inputs. It switches its output depending on which input line is more positive than the other one. As seen above, there is still a ground return line. It is still necessary, to have a interconnection of the driver and the receiver to provide a return current path.

Advantages of single ended transmission

The advantages of single ended transmission are simplicity and low cost of implementation. Obviously a single ended system requires one line per signal and is therefore ideal for parallel communication where many lines are required e.g. PC parallel printer port or serial communication with many handshaking lines e.g. RS-232. Cabling costs can be kept to an absolute minimum with short distance communication requiring no more than a low cost ribbon cable. For longer distances or/and noisy environments, shielding is essential and cabling costs begin to increase.

Disadvantages of single ended transmission

The main disadvantage of the single ended solution is its poor noise immunity. Because the ground wire forms part of the system, transient voltages or shifts in voltage potential may be induced (from nearby high frequency logic or high current power circuits), leading to signal degradation. This ultimately leads to false receiver triggering. For example, a shift in the ground potential at the receiver end of the system can lead to an apparent change in the input switching threshold of the receiver device, thus increasing its susceptibility to noise.

Cross talk is also a major concern especially at high frequencies. Crosstalk is generated from both, capacitive and inductive coupling. Capacitive coupling tends to be more severe at higher signal frequencies as capacitive reactance decreases. The impedance and termination of the coupled line determines whether the electric or the magnetic coupling is dominant. If the impedance of the line is high, the capacitive pickup is large. Alternatively, if the line impedance is low, the series impedance as seen by the induced voltage is low, allowing large currents to flow.

These problems will generally limit the distance and speed of reliable operation for a single ended link.

Advantages of differential transmission

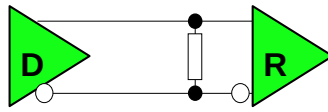
Balanced interface circuits consist of a generator with differential outputs and a receiver with differential inputs. Under the assumption that any noise is coupled into both wires of the transmission line in the same way, the resulting voltage difference between these two wires will be always zero. Due to the common mode rejection capability of a differential amplifier this noise will be rejected. This is true in any case for crosstalk from neighboring signal lines. It is also true for noise from other sources as long as the common mode voltage does not exceed the common mode range of the receiver. Also the common mode rejection of the receiver eliminates to a certain degree noise caused by a ground voltage difference between the generator and the receiver. The twisted pair cable used in these interfaces in combination with a correct line termination - to avoid line reflections - allows very high data rates of more than 30MBit/s and a cable length of up to 1200m.

Disadvantages of differential transmission

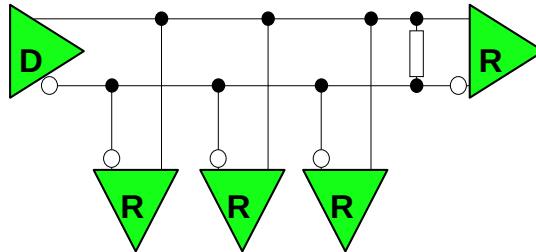
All these advantages come with some drawbacks. Owing to the more complex circuit technique required to achieve high performance these circuits are more expensive. Furthermore the high data rate possible requires well defined line impedance and a correct line termination to avoid line reflections. Also, twisted pair cable instead of cheap multi core cables have to be used.



Bus Topologies Point-to-point & Multidrop



Point-to-Point



Multidrop

1 - 6

As often bus topologies get confused, a brief introduction:

Point to point interfaces consist of just one driver and one receiver. A typical example is the serial port according to RS-232.

Multidrop has one driver, to which multiple receivers are connected. This type of interface is utilized by RS-422 industry bus systems.

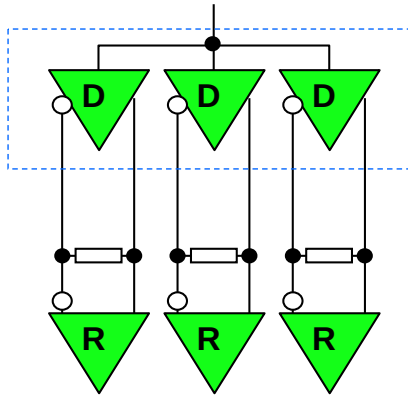
The mode of operation is referred to as “simplex”, respectably “simplex distribution bus”.

1 - 7

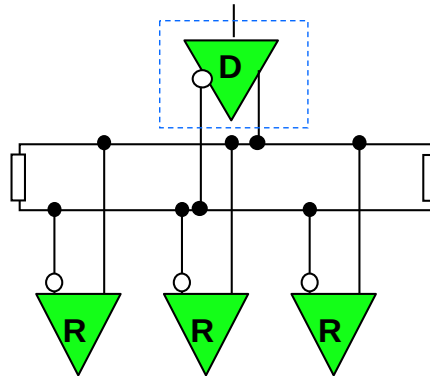
The mode of operation is called multiplex.

Bus Architectures

Point-to-Point (Star)



Multipoint



1 - 8

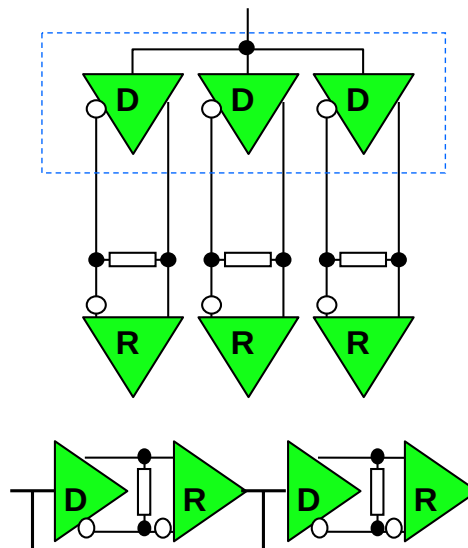
There are two major topologies for clock signal distribution: traditionally, and used for the majority of on-board-distribution, is a point-to-point connection, i.e. every device that needs a reference-clock has its individual feed, usually generated from a master-clock and splitted through a CDC-part (Clock Distribution Circuit) which converts one input to many outputs (=buffer). Sometimes, usually over backplanes, one can find a daisy-chain architecture, i.e. the connections from board to board are point-to-point, but each link depends on the reliability of the preceding ones.

Another approach, frequently used in data transmission over backplanes, is a multipoint-architecture. It enables multiple, alternate sources for the clock, which is transmitted over a bus, where each receiver represents a tap.



Point-to-point – Pros & Cons

- 👍 Good signal integrity (impedance-matching along entire path, proper termination)
- 👍 No Stub-lines (reflections)
- 👍 Independency of links (failure of one does not compromise other links)
- 👍 Synchronicity (e.g. meandering/delay-lines/delay-circuits)
- 👎 Star-topology: many connection lines, many connectors at star-point
- 👎 Daisy-Chain: long/different latencies, signal-degradation / need for regeneration (PLL), still twice as many connectors, multiple point-of-failures



1 - 9

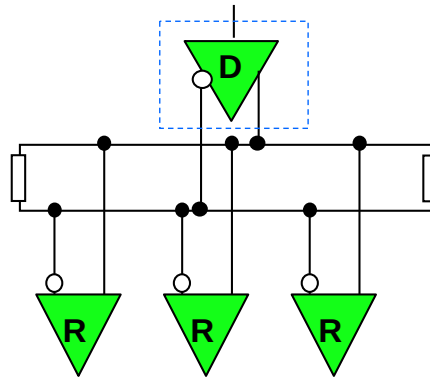
The main advantage of point-to-point connections is the good controllability over the complete link: the impedance is constant, therefore matching connectors can be used and the necessary value of the termination resistor is predictable. The board layout is easy, as no stub-lines occur. Furthermore, if one link fails, the other can still continue operation – unless the master-clock or the splitter fails.

The disadvantages are the high number of necessary connections and the need for a splitter device in case of a star-topology. Assuming daisy-chaining, the number of necessary connections is reduced compared to above described star-topology, but is still twice as high vs. a multipoint-architecture. Furthermore, with a chain, a single point of failure will cause the whole down-stream-section to fail. Another drawback is, that without jitter-cleaning (requiring a PLL), the contribution of each link (transmitters, connectors, traces/cables, receivers) will add to the total jitter, which limits the maximum number of links. Most importantly, if one blade is pulled, the chain is interrupted. Some backplane-connectors avoid this by shorting the connectors in the plug if no card is present, but even in this case, a significant distortion is to be expected.



Multipoint - Pros & Cons

- 👍 Few connectors and lines
- 👍 Option for multiple sources / source-nodes
- 👍 Easy monitoring
- 👍 More space: easier layout
- 👎 Impedance-matching difficult (compromise of node-count)
- 👎 Reflections due to stub-lines
- 👎 Signal-Integrity due the above
- 👎 Higher capacitive loading (slew-rates, propagation times)
- 👎 Crosstalk
- 👎 Multiple point-of-failures



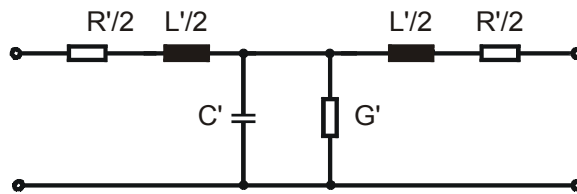
1 - 10

For multipoint, obviously the number of connectors can be significantly reduced. Also, it allows for multiple, alternate sources, which can provide redundancy. The monitoring of the clock (existence and quality) is very simple, as only one link needs to be observed.

Vice-versa, the layout gets more difficult, as care needs to be taken with respect to stub-line lengths, capacitances and impedances of the stubs, etc. The stub-lines will cause reflections and their capacitances will cause the bus impedance to change with the number of loads. Therefore, the optimum termination can only be a carefully chosen compromise between light- and full-load of the bus. A further impact of the capacitive load is prolonged transition times, ultimately limiting the achievable frequency. Another drawback is point of failure, as any node on the bus may impact the complete chain in case of a failure of its bus I/O, e.g. a short-circuit.



Circuit diagram of a Transmission Line



L'	Characteristic inductance per unit length	nH/cm
C'	Characteristic capacitance per unit length	pF/cm
R'	Characteristic resistance per unit length	Ω /cm
G'	Characteristic conductance per unit length	S/cm

Line Impedance:
$$Z_0 = \sqrt{\frac{j\omega L' + R'}{j\omega C' + G'}}$$

1 - 11

The equivalent circuit of a transmission line consists of an inductance L' - representing the inductance of the transmission line, a resistor R' - representing the ohmic resistance of the line, a capacitance C' - representing the capacitance of the line and the conductance G' - representing the losses in the capacitance of the line. All these values are length dependent and are therefore specified in unit/length, e.g.: nH/cm, pF/cm, Ω /cm, and S/cm. By setting up a set of differential equations, one can calculate the impedance of a transmission line:

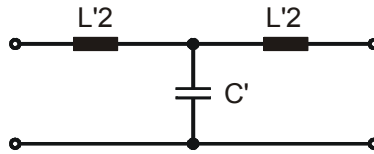
$$Z_o = \sqrt{\frac{j\omega L' + R'}{j\omega C' + G'}}$$

In practice this equation is difficult to handle. Firstly, the line impedance results in a complex number which makes the required calculations time consuming. Secondly, the line impedance is frequency dependent. This fact becomes uncomfortable in digital circuit, where one has to consider many frequencies simultaneously.



Loss-free Transmission Lines

At high frequencies the transmission line losses (R' , G') can be neglected compared with the impedance of the inductance and the conductance of the capacitance.



With $R' \ll j\omega L'$ and $G' \ll j\omega C'$:

Line impedance $Z_o = \sqrt{\frac{L'}{C'}} \quad (\text{real number!})$

Propagation time $t_p = \sqrt{L' \times C'}$

1 - 12

In digital circuits low frequencies are not generally of concern. At higher frequencies (above some 10kHz) the impedance of the inductance $j\omega L'$ becomes large compared to the resistance R' of the wire. The admittance $j\omega C'$ is also much greater than the corresponding conductance G' . Under this assumption R' and G' can be neglected. The impedance of the transmission line can now be calculated by the simple formula:

$$Z_o = \sqrt{\frac{L'}{C'}}$$

The impedance is now a real number which can be handled like an ohmic resistor. A further advantage is Z_o is now independent of the frequency.

An important parameter in data transmission circuits is the propagation time t_p of the signal on a transmission line. This time is also determined by the parameters of the line:

$$t_p = \sqrt{L' \cdot C'}$$

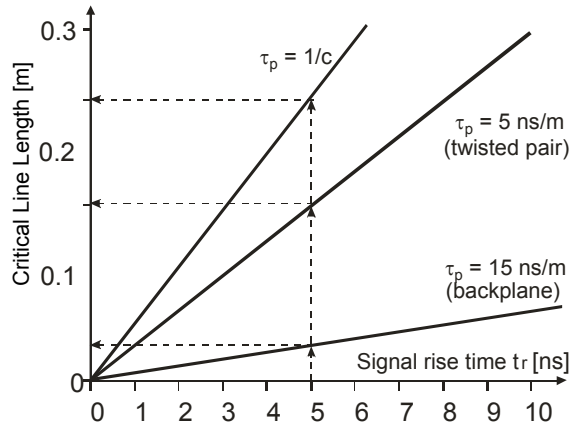
On typical cables used in transmission circuits (coaxial cable, twisted pair cable) the propagation time becomes $t_p = 5\text{ns/m}$. This reflects a propagation speed $v = 200,000\text{km/s}$ (about 60% of the speed of light).



Transmission Line Theory

Rule of Thumb:

Transmission line theory has to be applied when the rise time of the signal is shorter than twice the propagation time.



Critical line length

$$l_{\max} = \frac{t_r}{6 \times \tau_p}$$

1 - 13

As a rule of thumb, transmission lines have to be treated as lines in accordance with transmission line theory when twice the signal propagation time becomes longer than the rise time of the signal. However, the more common approach is to use six times the propagation delay as basis for better signal integrity, i.e. when the (first three) line reflections no longer fall anymore into the rise time interval. For a given rise time $t_r = 5 \text{ ns}$ and a typical propagation time of the signal $t_p = 5 \text{ ns/m}$, the critical line length in $l_{\max} = 16 \text{ cm}$. In applications where the propagation time of the signal is much longer - e.g. bus lines - the critical line length is even shorter.



Analysis of Line Reflections

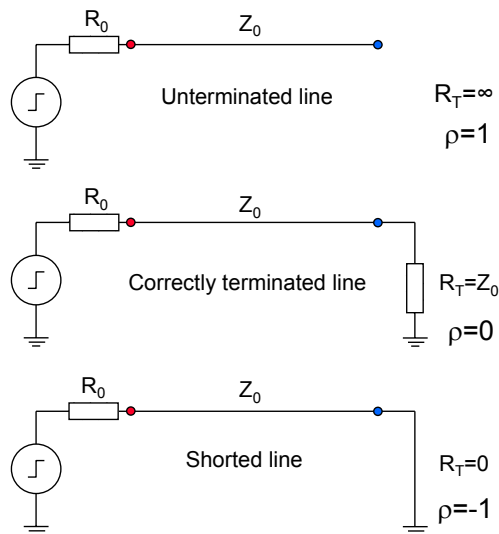


1 - 14

In data transmission systems the designer has to take care of line reflections caused by improperly terminated lines. These line reflections may lead to an additional signal distortion which cause incorrect detection of the value of the signal at the line end (receiver input). This may result in an false operation of the system.



Reflection-Factor



1 - 15

There are three options to terminate: with too high impedance (or not at all), properly, i.e. with a resistor matching the line impedance or with too low impedance (worst case: short circuit).

If the termination is chosen too high, a positive reflection factor will cause reflected waves adding to the incoming one. Analogy: cliff or wall.

$$\rho = \frac{R_T - Z_0}{R_T + Z_0} = \frac{\infty - 50\Omega}{\infty + 50\Omega} = 1$$

With proper termination, no reflection will occur. Analogy: tetrapods.

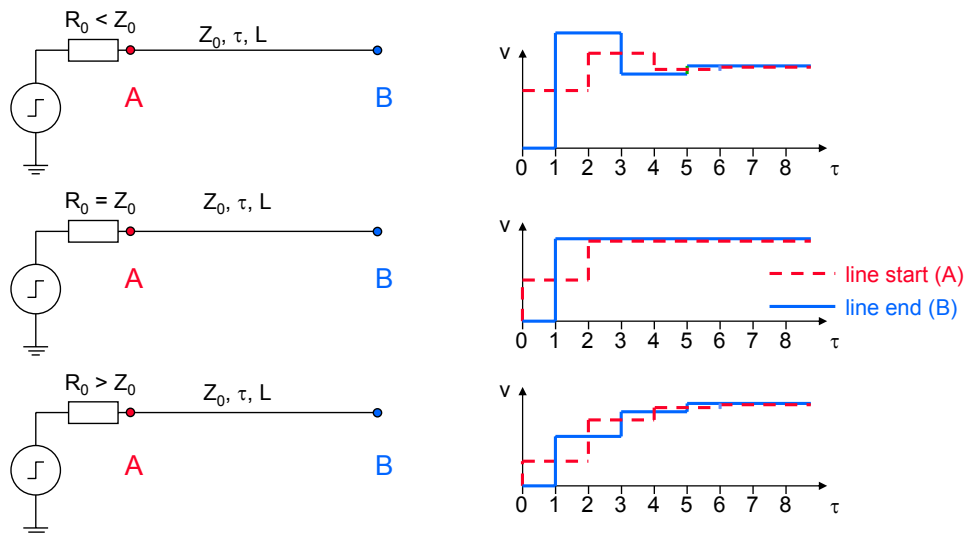
$$\rho = \frac{R_T - Z_0}{R_T + Z_0} = \frac{50\Omega - 50\Omega}{50\Omega + 50\Omega} = 0$$

With too low impedance (less than the line impedance), negative reflections will be generated, subtracting from the incoming wave. This is also undesired, as the amplitude will be degraded and distortions are inevitable. Analogy: wide, flat beach.

$$\rho = \frac{R_T - Z_0}{R_T + Z_0} = \frac{0 - 50\Omega}{0 + 50\Omega} = -1$$



Typical wave-forms on unterminated lines



1 - 16

Typical wave-forms on unterminated lines:

1) $R_0 < Z_0$:

The resistor divider R_0 and Z determine the amplitude of incident wave. In this case the amplitude is higher than 50% of the full voltage swing. This signal is 100% reflected at the unterminated end of the line, this means that it is doubled thus a overshoot can be seen at the line end. A negative reflection factor at the line start generated a undershoot when the reflected wave arrives.

2) $R_0 = Z_0$:

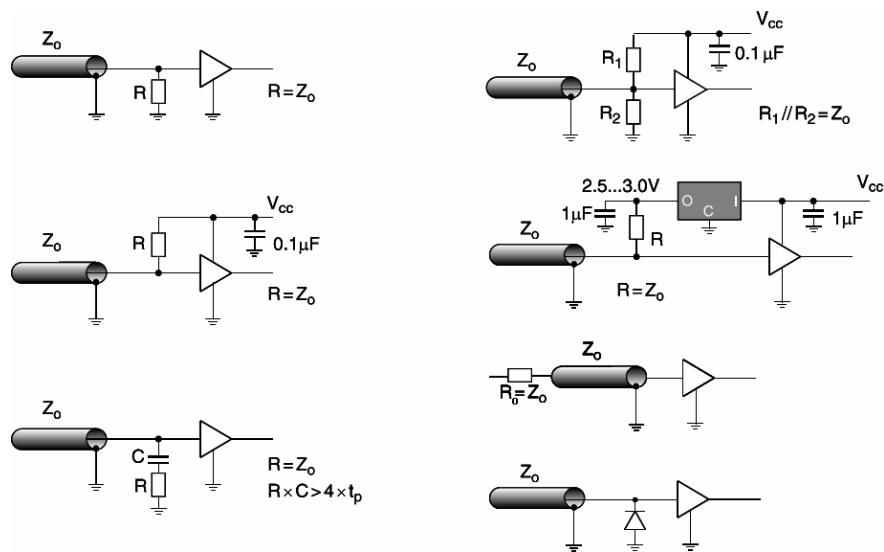
Two equal resistors generate a incident wave with exactly half of the full voltage swing. Again the incident wave is 100% reflected at the line end, hence the voltage doubles. The amplitude of the incident and the reflected wave together result in exactly the full generator voltage swing.

3) $R_0 > Z_0$:

The high output impedance of the generator limits the amplitude of the incident wave to less than 50% of the generator amplitude. Thus the sum of the incident wave and the reflected wave are less than 100%. It takes several signal delay times to reach the final high level.



Line Termination Circuits

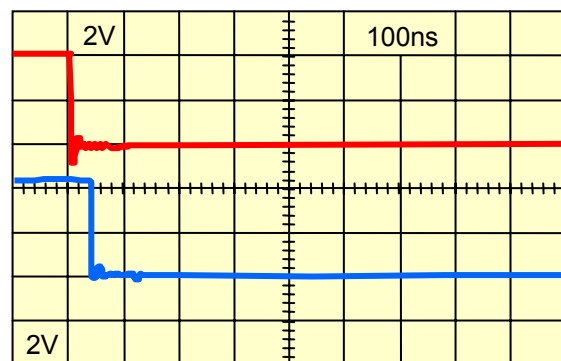


1 - 17

Single ended or unbalanced transmission lines are usually terminated by a resistor between the line end and signal ground. If the drive capability of the generator in high state is not sufficient - e.g. circuits with open collector or open drain outputs - the termination resistor can also be placed between the line and the positive supply rail. This rail for low frequencies is shorted to ground via the power supply and for high frequencies via the decoupling capacitor (typical 10nF).

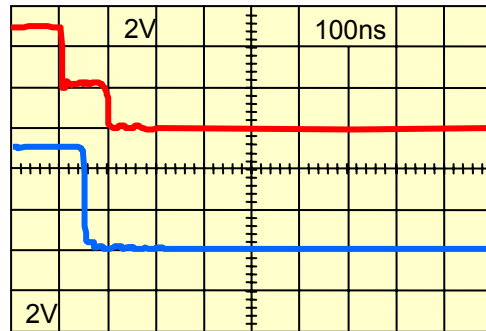
Particularly in CMOS applications, the designer does not like the continuous current in the termination resistor. This current increases the power dissipation. The current can be blocked by placing a capacitor C in series with the termination resistor R_t . When the time constant RC is about 4 times the propagation time of the interface circuit, the line is almost sufficiently terminated.

In TTL systems, a resistor divider is often found at the line end (split resistor or Thevenin termination). This circuit is adapted ideally to the drive capability of TTL circuit and performs well in terms of eliminating line reflections. However the disadvantage of this arrangement is the large DC current through the resistor divider.



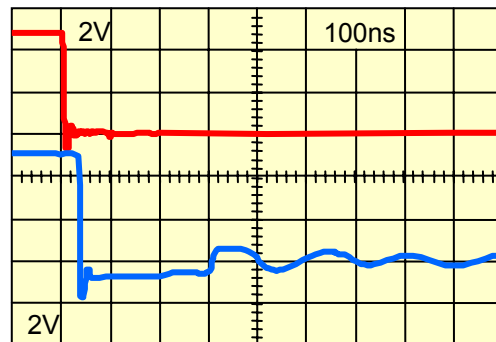
An elegant method to avoid under- and overshoots at the line end is to match the output impedance of the driver circuit to the line impedance by placing a resistor in series with the output. A different output impedance of the driver in the low and the high state mostly does not allow correct matching. As long as the output impedance of the circuit in question is chosen to be 60 % to 100 % of the line impedance, a reasonable signal quality can be expected at the line end (receiver input).

This technique is applicable in uni- and bi-directional point-to-point interfaces. In multi-point applications, where several stations are located along the transmission line, this technique is not recommended due to the long settling time of the signal (up to twice the propagation time).



An effective method to avoid excessive under- and overshoot at the line end is to limit this by means of clamping diodes. As the picture shows, a negative transition at the beginning of the transmission line causes a negative

undershoot at the line end where the amplitude is limited to the forward voltage of the clamping diode at the line end ($\approx 0.7V$). The energy stored in the transmission line is not absorbed totally. Therefore, one can observe several waves traveling forward and backward on the line. However, their amplitude is only a few 100mV.



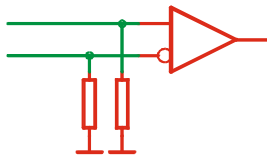
Owing to the positive influence of these diodes, clamping diodes are integrated into all logic circuits. TTL circuits contain at their inputs clamping diodes to the ground terminal to limit negative undershoots. In a CMOS environment, where owing to the higher voltage swing the positive overshoots are also of concern, additional clamping diodes between the input and the positive supply rail are often incorporated.

Therefore, in advanced systems a circuit is often used, which is called “active termination”. Here, the termination resistor is placed between the line end and the output of an additional power supply, which provides an output voltage of 2.5 ... 3V. Since on average 50 % of its active time the line is in the high state, the supply current is reduced by this amount. This termination technique is also used in bus applications, where much of the operating time all bus drivers are in inactive mode (3-state). In this situation the supply current becomes zero. Last but not least, the pull-up resistor avoids the line floating when all bus drivers are in the 3-state.



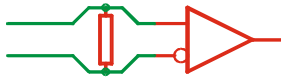
Differential Line Termination

Parallel

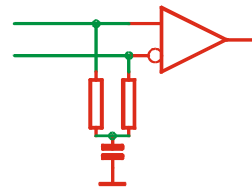


- for open collector/drain ((LV)PECL, CML)
- differences in common mode currents
- **not suitable** with DC-offset signals

Differential



- requires push-pull drivers (LVDS, VML)
- no common mode termination (=> unsymmetries of the media cause reflections)

Differential tapped
Differential symmetrical

- requires push-pull drivers (LVDS, VML)
- (AC-) common mode termination
- lowest noise solution

1 - 19

Differential lines have to be terminated a bit differently.

Parallel termination treats each line individually. Common mode voltage changes won't get terminated with this method. This scheme is not applicable with transmission methods, that use a DC-offset, such as LVDS (~1.2V).

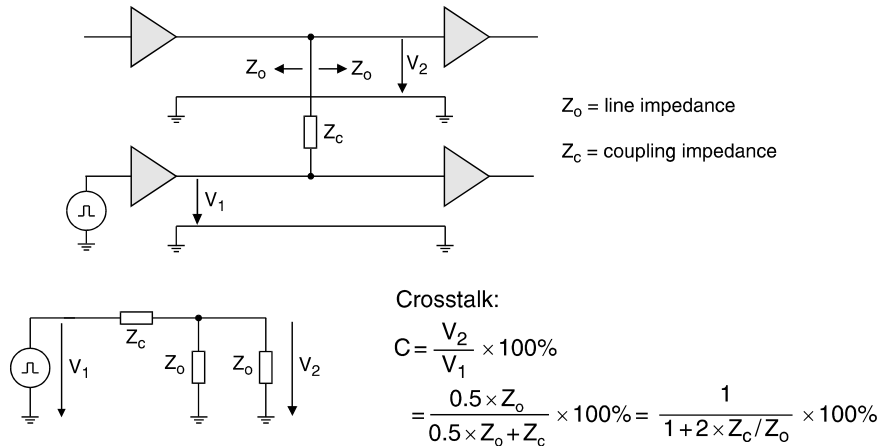
Differential termination is the most frequently used one for LVDS signals. It's not applicable for drivers that do not provide a push-pull-output like i.e CML or LVPECL. Common mode voltage changes won't get terminated with this method

Center-tapped-differential describes a split-termination, where a center-tap of the termination-resistor (or more likely two i.e. 50Ω-resistors in series for an effective 100Ω termination) is used to balance the signal around a common mode level. It's for example mandatory in cases where short unbalances in the differential signal have to be canceled.



Crosstalk

On long transmission lines ($2 \times t_p > t_r$) the crosstalk can be calculated as follows:



1 - 20

The characteristics of a transmission line can be described by its inductance and capacitance per unit length. When two transmission lines are placed in parallel, one can now define inductance and capacitance per unit length between these two circuits, to give the coupling impedance Z_c . Using this assumption, one can easily describe the crosstalk between interfaces: a signal is transmitted via one line and is coupled via the coupling impedance into the neighboring line. Assuming the coupling would happen at one certain point, the load for the cross-coupled signal is half of the line impedance Z_0 (two lines running in opposite direction). The resulting crosstalk can now be calculated by using the following formula:

$$C = \frac{1}{1 + 2 \frac{Z_c}{Z_0}}$$



Crosstalk on Printed Circuit Boards (example)

	Line Impedance Z_0 [Ω]	Coupling Impedance Z_c [Ω]	Crosstalk [%]
	200	100	50
	80	125	25
	100	400	11

Note: line width = line distance

For Details please reference:

"High-Speed Digital Design, A Handbook of Black Magic" by Howard Johnson & Martin Graham (ISBN: 0-13-395724-1)

"Printed Circuit Board Design Techniques for EMC Compliance" by Mark I. Montrose (ISBN: 0-7803-1131-0)

1 - 21

By applying the formula above, the crosstalk between signal lines on printed circuit boards can be analyzed. In the first example two printed wires are running in parallel, with the width of the wires equal to the distance between the wires e.g. 0.5mm. This arrangement results in a coupling impedance $Z_c=100\Omega$. (In the literature dealing with strip lines and microstrips, formulas are shown which allow the calculation of the line impedance based on the physical dimension of the lines). The ground return line is assumed to be far away e.g. 2cm. This leads to a line impedance of 200Ω and a crosstalk of 50%. Since no logic circuit provides a noise margin of 50%, such an arrangement is not applicable.

In the second example a ground plane is placed on the opposite side of the printed circuit board. By this, depending on the thickness of the dielectric, the line impedance is lowered to e.g. $Z_0=80\Omega$, the coupling impedance is increased to $Z_c=125\Omega$. The exact formulae for this calculation can be found in the LVDS section of this handbook. The resulting crosstalk is now only 25%. In digital circuits such value may be acceptable. This example also explains the benefit of a multi layer-board with a ground plane in terms of lowering the noise level in digital circuits.

In the third example a shielding wire is placed between the signal lines. (Note: the shielding wire must be connected to ground on both ends.) Again it is assumed, that the line width is equal to line separation. In such an arrangement the line impedance becomes $Z_0=100\Omega$ and the coupling impedance $Z_C=400\Omega$. The resulting crosstalk is lowered to $C=10\%$, which is in most cases acceptable.

This also explains why twisted pair cables are used for longer lines. One wire of the pair is the signal line, and the other the signal return (ground). Similar behavior is found, if flat cables are used with alternate ground and signal lines. Such an arrangement gives a well defined line impedance ($Z_0=80$ to 120Ω) and a low crosstalk. Last but not least, typical crosstalk in a well designed interface will be at least 10%. This is also valid for the interference between any electrical cable and the interfaces.

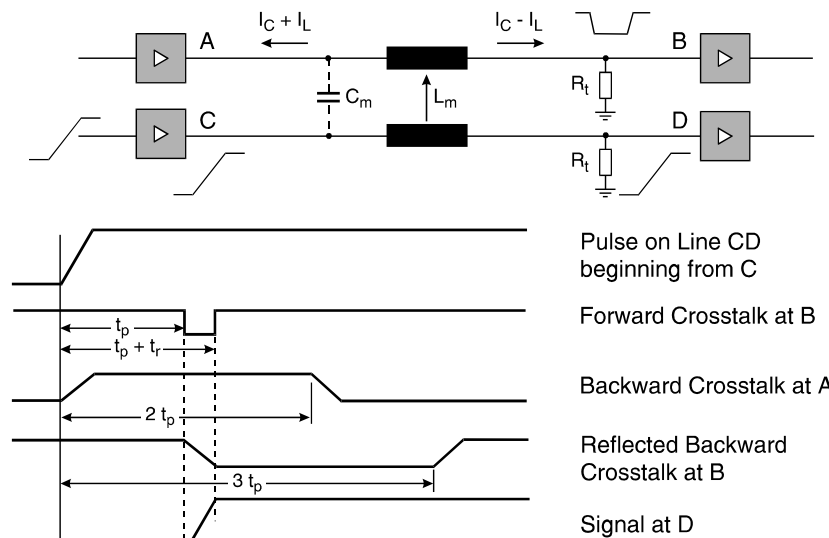
Following literature may be helpful:

“High-Speed Digital Design, A Handbook of Black Magic” by Howard Johnson & Martin Graham (ISBN: 0-13-395724-1)

“Printed Circuit Board Design Techniques for EMC Compliance” by Mark I. Montrose (ISBN: 0-7803-1131-0)



Crosstalk on Transmission Lines



1 - 23

When analyzing the crosstalk in more detail, one finds that

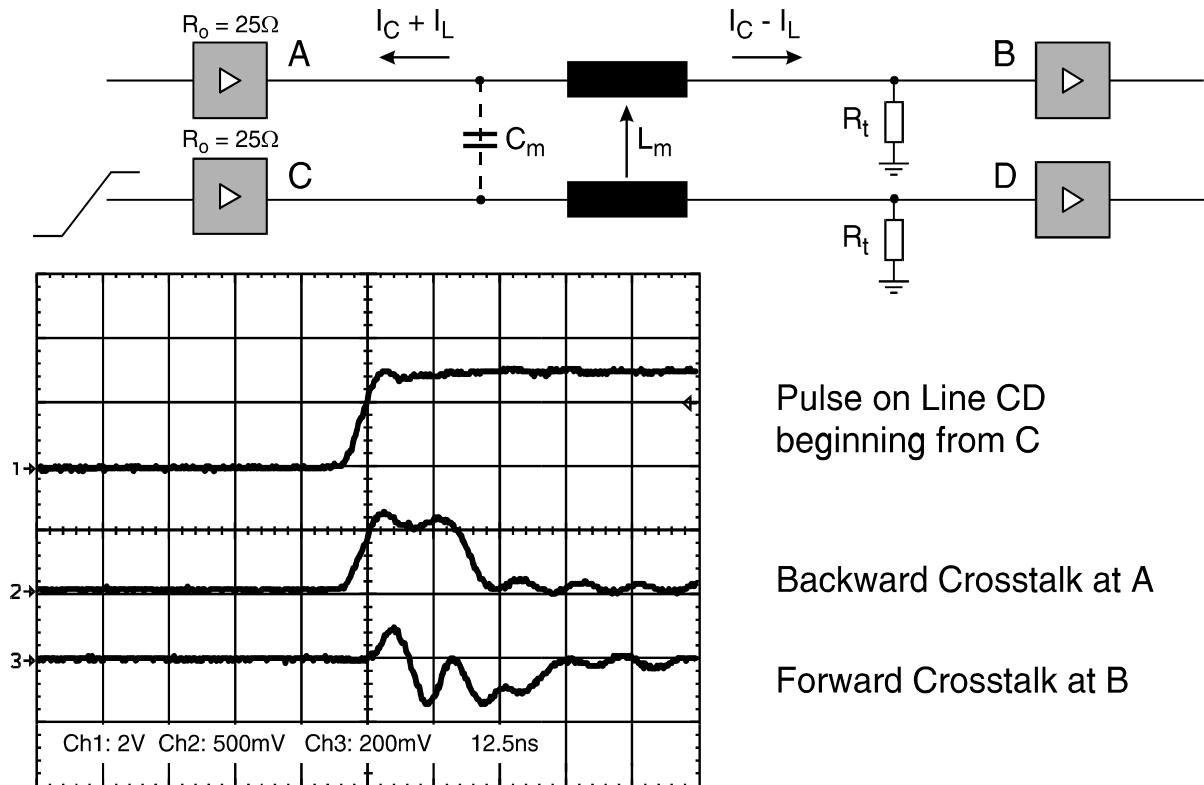
- a) there is capacitive coupling and
- b) inductive coupling

which induces two currents into the affected line: a current I_C caused by the capacitive crosstalk and a current I_L caused by the inductive crosstalk. When looking from the generator standpoint, the currents travelling down the affected line subtract ($I_C - I_L$). As the inductive coupling on parallel lines is usually stronger than the capacitive, this results into a negative pulse at the end of this line. Its width is equal to the rise time of the original signal, as the coupling only occurs during the signal transition (Forward Crosstalk at B in the picture above).

In the reverse direction, the currents add ($I_C + I_L$), which leads at the line end near to the generator to a pulse which width is equal to twice the propagation time of signal, as the coupling occurs one the whole line during the whole propagation through the line (one propagation time) and gets reflected at point B, which will be seen another propagation time later at A. What is coupled at the very begin of the line, will be seen immediately at A (Backward crosstalk at A in the picture above). This noise pulse is reflected at the point A and arrives one propagation time later at the far end (Reflected Backward Crosstalk at B in the picture above).

Crosstalk on Transmission Lines, 3-wire Cable

In the following, the behavior of various circuits arrangements will be analyzed. In the first example a transmission line with length 2m is used which consists of three wires running in parallel (not twisted). The cross-coupled signal at the point B has again a relatively small amplitude which is superimposed on the noise caused by the reflected backward crosstalk at B. Since the generator output impedance at A is smaller than the line impedance, the reflection factor at A becomes negative. This results in a negative amplitude of the forward crosstalk at B.

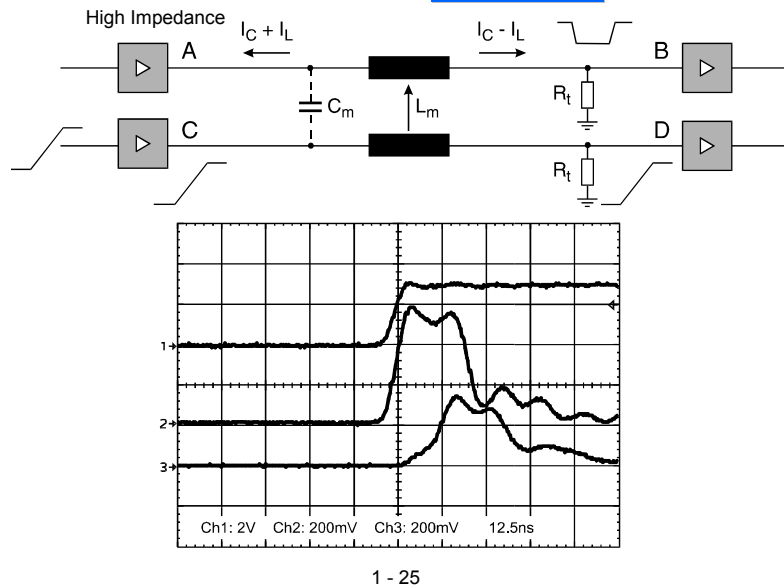


Note that the three wire circuit used in this application has a similar characteristic to the printed wire circuit with a shielding wire between these two lines (discussed above). The crosstalk is relatively small. In a multi core cable, where only one or a few ground return wires are available, the crosstalk becomes much larger. Under these conditions, reliable operation of the interface can no longer be guaranteed.

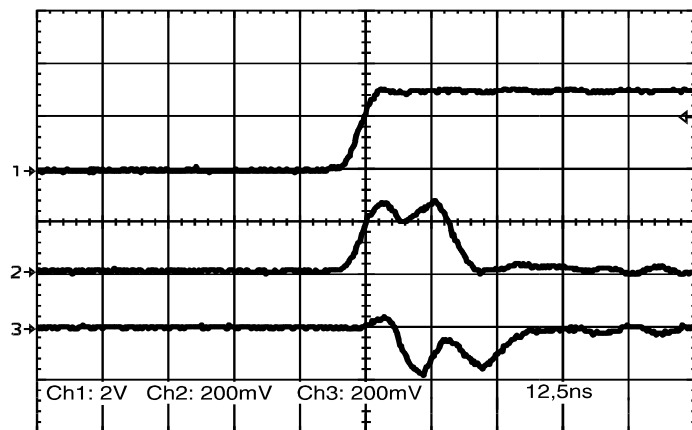


Crosstalk on Transmission Lines

2 twisted pairs, $Z_0=100\Omega$, Driver A in High Impedance



The same circuit arrangement, but using twisted pairs, shows a similar behavior. The crosstalk at the far end (the receiver at the induced line) again is relatively small. When using twisted pair cables the shielding effect of the many signal return wires keeps the crosstalk at moderately low level even if many pairs are running in parallel in cable.



Crosstalk on Transmission Lines, High Near End Impedance

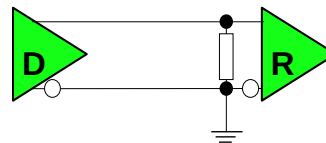
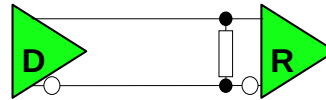
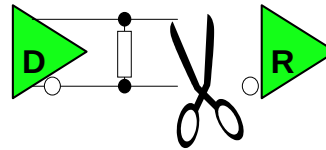
If the output impedance of the generator at the affected line becomes very large (e.g. generator output in 3-state), the reflection factor becomes $\rho=1$ (positive!). Thus the cross coupled signal has a large positive amplitude at the point A. This leads also to a positive amplitude of the noise voltage at the point B.

Consider also the following situation: assuming a receiver is located at B where the line is not terminated, the function of the receiver may be affected by the large noise voltage there.



Failsafe Open, Short & Idle

- Open-Failsafe:
Disconnected from the Bus,
no Termination
- Idle-Failsafe:
Connected to Bus,
Termination in Place
All Drivers Inactive (high Impedance)
- Short-Failsafe:
Connected to Bus,
Termination in Place
Short-circuit between the lines or
(possibly) one line shorted to Vcc or GND



1 - 26

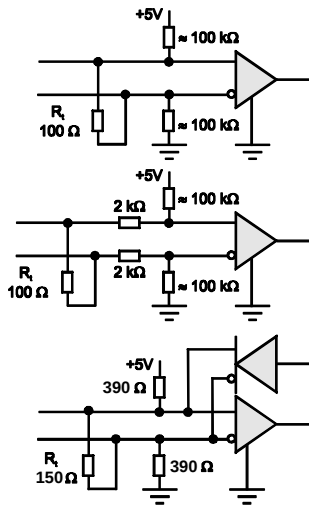
Failsafe indicates a known output stage of a receiver while no valid input signal is applied. One distinguishes between three categories:

- 1) “Open Failsafe”, indicating the receiver has a defined output if it is disconnected from the bus. Note: there is also no termination resistor!
- 2) “Idle Failsafe” signals that the receiver will output a defined level in case the bus is floating, e.g. if all connected drivers are set to high-impedance-outputs.
- 3) “Short Failsafe” means the receiver has a defined output if there is a short between the differential lines. It may also indicate failsafe in case one of the lines is shorted to Vcc or GND, but this is device / vendor dependent.



Fail Safe ??

Valid Logic Levels with Generator in the OFF-State



Integrated high impedance resistors generate a defined logic level. Not applicable with low impedance termination

Series resistors ($\approx 2\text{k}\Omega$) ensure a defined logic level even if the line is terminated by a low impedance. Not applicable with transceivers.

External low impedance resistors generate a defined logic level when the driver is in OFF-state. Not in conformance with RS-485: high load, reduced common mode range.

1 - 27

The following measures are used to avoid undefined states in a multi-point interface:

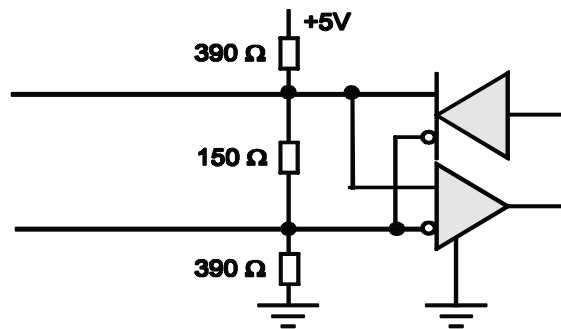
- 1) Option one shows a high impedance pull-up and pull-down resistor at the receiver inputs. The intention of this circuit is to provide a defined logic state in case of a broken wire or a missing transmission line. If, however, the line is terminated at the end by a low impedance resistor e.g. $R_T=100\Omega$ (mandatory in a multi-point interface!), the pull-resistors form a serial configuration with the termination resistor and the voltage difference across the latter becomes almost zero again (resistive voltage divider!). Interface circuits which incorporate these high impedance resistors are often called 'fail safe' in the data sheet.
- 2) Another option suggests additional resistors of $\sim 2\text{k}\Omega$ in series to the inputs. These resistors will avoid a short circuit of the pull-up / pull-down resistors even if the line is terminated by a low impedance resistor. In any case, these additional resistors reduce the sensitivity of the receiver. Finally, this method is not applicable to transceiver circuits.

- Continued on following pages -

3) A third circuit uses low impedance pull-up and pull-down resistors ($R=500\Omega$). Even if the line is terminated, the termination resistor will not short this biasing network. Therefore a differential voltage of about 500mV stays on the line when all generators are in the 3-state mode. A disadvantage of this circuit is the load generated by the pull-up and pull-down resistors. This load reduces the maximum number of receivers connected to the interface and also influences the common mode range (high current in the resistors when a high ground potential difference exists between the generator and the termination circuits.) Also, the high power consumption has to be considered ($[5V]^2/1100\Omega=23mW$).

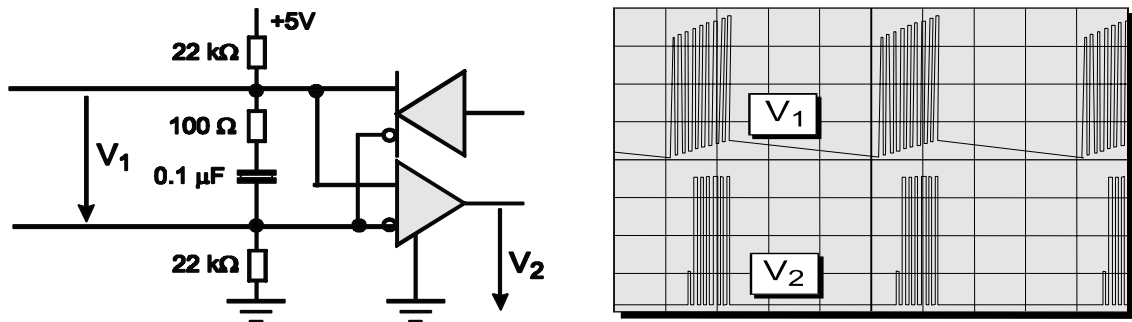
Valid Logic Levels with Inactive Generator

The Profibus (DIN 19245) has been designed for industrial control applications. To ensure valid logic levels when all generators are in the 3-state, pull-up and pull-down resistors are placed at the line end (390Ω each at both ends of the interface). Since these resistors are in parallel to the termination resistor, the termination resistor can be higher impedance ($R_T=150\Omega$ or 220Ω). That compensates the load of the biasing circuit.

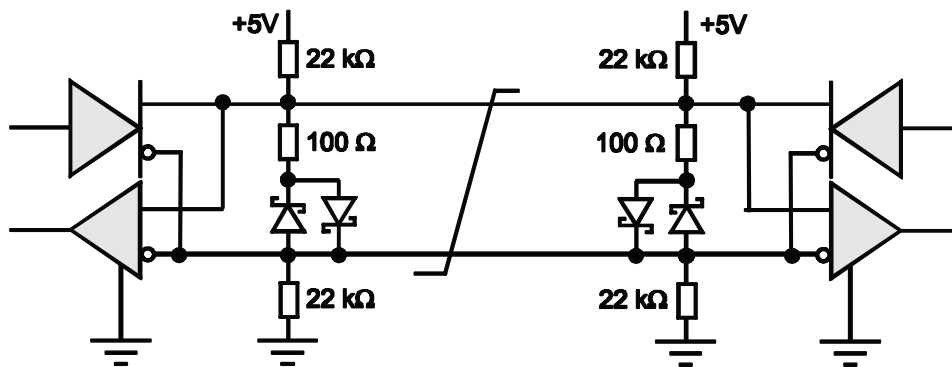


An elegant method to eliminate the DC current in the termination resistor and to reduce the power consumption of the interface is to place a capacitor of 0.1μF in series with the termination resistor. When doing this, the pull-up / pull-down resistors, which ensure valid logic levels with inactive generators, can be made high impedance (typ. 22 kΩ). The biasing function can be performed well with this arrangement. However problems may occur with the high ohmic resistance of long transmission lines. When all generators are in 3-state, the capacitors in series with the termination resistors are charged up via the pull-up / pull-down resistors to a voltage equal to $V_{CC}=5V$. When a generator now becomes active again, this capacitor has to be discharged again (average voltage at the capacitor is 0V when the bus is active). During this discharge the voltage divider caused by the ohmic

resistor of the wires and the termination resistor in conjunction with the capacitor perform a low-pass, which prevents valid logic levels at the line end for some time. As the oscillograph shows, this phenomenon leads to loss of the first part of the transmitted data stream.



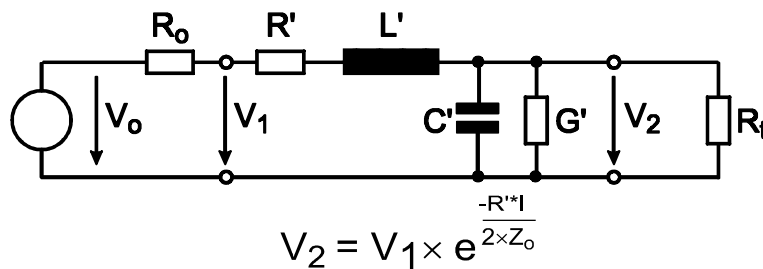
Adequate biasing of an inactive interface can also be made by two inverse-parallel connected Schottky diodes (forward voltage $V_f \gg 400$ mV) in series with the termination resistor. Since only a very low current is required to force a voltage drop of 400 mV at the Schottky diodes, the pull-up and pull-down resistors can be made high impedance again (22 kΩ each).



Traditionally, receivers often provide “Open Failsafe” only. To achieve “Idle Failsafe” one of the solutions as described above would be used. Modern transceivers often come with “Open, Short and Idle Failsafe”. The external measures are not necessary with those.

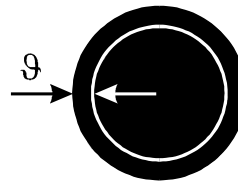


Losses on Transmission Lines



Owing to the skin effect at frequencies above some hundred kHz only the outer layer of the wire conducts. Thus losses increase by a factor $\sqrt{f}$.

f (MHz)	ϑ (μm)
1	68
100	6.8
10,000	0.68



1 - 30

Owing to the ohmic resistance of the wires R' , and to a lower degree the conduction G' of the transmission lines, the amplitude of the signal is degraded with increasing line length. The voltage at the line V_2 can be calculated by using the following formula:

$$V_2 = V_1 \cdot e^{\frac{-R' \cdot l}{2 \cdot Z_0} + \frac{-G' \cdot l \cdot Z_0}{2}}$$

with $G' \rightarrow 0$ one can simplify the equation:

$$V_2 = V_1 \cdot e^{\frac{-R' \cdot l}{2 \cdot Z_0}}$$

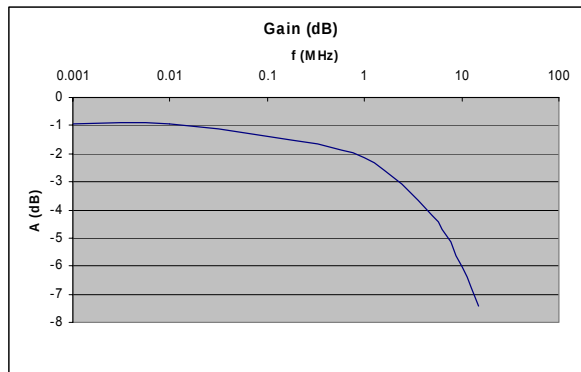
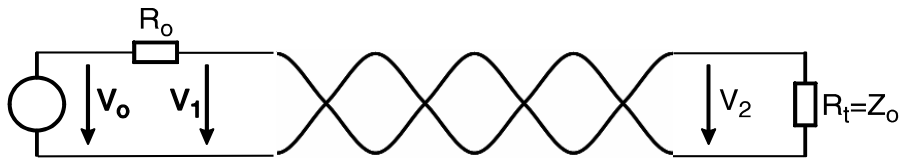
As an example, a transmission line with impedance $Z_0=100\Omega$, length $l=1000\text{m}$ and resistance per unit length $R=0.1\Omega/\text{m}$, reduces the voltage at the line end by about 40%.

The formula shown above does not consider the so called *skin effect*. This causes the current to flow only on the surface of the conductor at higher frequencies. This becomes of importance at frequencies $>100\text{kHz}$.

Therefore above this frequency the resistance of the wire increases with $\sqrt{f}$.



Frequency Response of a Transmission Line



Twisted Pair Cable
Length = 100m

1 - 31

Due to the skin effect, a transmission line has a characteristic similar to a low-pass filter. To analyse the actual behaviour of a transmission line, we measured a twisted pair cable of length $l=100\text{m}$. As can be seen in the picture above, up to a frequency of approximately 1MHz the losses of the cable remain small. Above 1MHz however, the attenuation increases considerably.



Electro Static Discharge (ESD) examples

- Shoes on carpet:
35kV @ 20% RH 1.5kV @ 65% RH
- Shoes on PVC:
12kV @ 20% RH 250V @ 65% RH
- Poly-Bag picked up from Desk:
20kV @ 20% RH 1.2kV @ 65% RH

RH: Relative Humidity

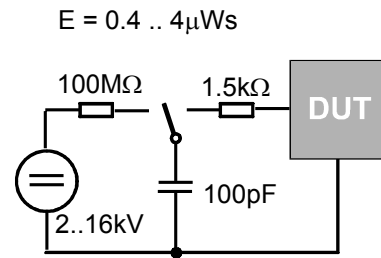
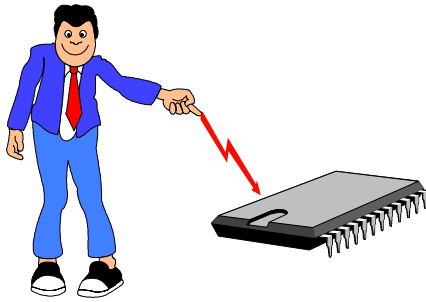
1 - 32

Above some ordinary events are listed, along with their potential to charge. Especially with low humidity, several 10kV can be achieved with such simple things like walking or picking up a plastic bag. This demonstrates the importance of high tolerances to ESD strikes, despite the fact that ESD-precautions shall be taken whenever handling electronic equipment.



Electrostatic Discharge 1

Human Body Model



The Human Body Model (HBM) simulated the discharge of a human body into an electronic device

Note: when it tickles the finger, the voltage is $>\sim 4000\text{V}$.

1 - 33

Human Body Model

Various test methods have been developed to analyze the immunity of electronic components to damage by an electrostatic discharge. One popular test circuit is the so called Human Body Model, which simulates the situation where the electric charge stored in a human body is discharged into the device under test. To simulate that a capacitor $C=100\text{pF}$ (capacitance of the human body) is charged up to a test voltage (e.g. 2000V) and is discharged thereafter via a resistor $R = 1.5\text{k}\Omega$ into the circuit.

The transition time of the current in the circuit under test at the beginning of the discharge is extremely short: $t_r < 1\text{ns}$. During this short time interval only a small area of the total protection network inside the integrated circuit starts to conduct. This small area in some cases is not capable of dissipating the total power. The silicon melts and the device is destroyed. This phenomenon explains also that if the discharge does not occur in the immediate neighborhood of the circuit but at a certain distance the device will survive: the inductance of the interconnect between the point of discharge and the integrated circuit slows down the rise time. Now the total area of the integrated protection network can conduct and short the current to ground.

The protection network must be able to carry the relative high currents during the discharge. In the test circuit shown above the peak current is $\sim 1.5\text{A}$.

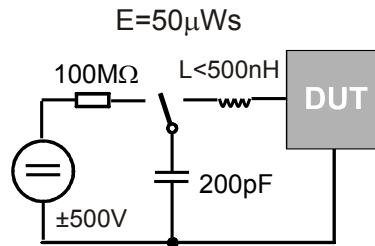
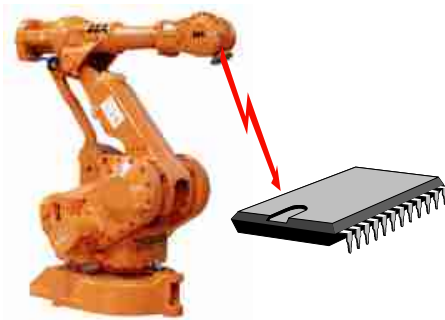
The protection network must be capable of handling the energy during a discharge. Mostly, however, the energy is not of concern. Most of the power stored in the capacitor is dissipated in the series resistor. Assuming the breakdown voltage of the device under test to be $V_{br}=20V$ (in most applications only the forward voltage of the clamping diode $V_f=1$ to $2V$ has to be considered), the resulting Energy E_a to be absorbed (@ $2kV$ test-voltage) by the device under test can be calculated as follows:

$$E_a = V_{br} \cdot V \cdot C = 20V \cdot 2000V \cdot 100 pF = 4 \mu Ws$$

The JEDEC-Standard EIA/JESD-22-A114-A specifies a similar circuitry which generates even harder conditions: The capacitor has $150pF$ and the series-resistor only 330Ω .



Electrostatic Discharge 2 Machine Model



The Machine Model simulates the discharge of a machine, e.g. an automatic handler, into an electronic device

Today's integrated devices withstand a discharge voltage of 200 ...500V

1 - 35

Machine Model

Another test circuit had been developed in Japan called the Machine Model. In this test set up a capacitor of $C = 200\text{pF}$ is charged up to a voltage $V = \pm 500\text{V}$, after which the capacitor is discharged into the device under test without any current limiting series resistor. Because of this, the energy E_a to be absorbed in the device under test becomes much larger:

$$E_a = 0.5 \cdot V^2 \cdot C = 500^2 V^2 \cdot 200 \text{ pF} = 50 \mu\text{Ws}$$

On the other hand, the test specification allows a relatively high inductance in the discharge circuit (up to 500nH). This inductance slows down the rise time of the discharge current. Finally, this test mostly addresses the capability of the device under test to absorb a certain amount of energy. Therefore, a fast reaction time of the protection circuit is not that much of concern.

Last but not least, state-of-the-art integrated circuits withstand without damage a Human Body Model test of 15kV, while most circuits in a Machine-Model test withstand only voltages up to 500V.

The JEDEC-Standard EIA/JESD-22-A115-A specifies a similar circuitry.



Robustness: ESD and Transients

ESD-Strikes have

- Very high Voltages (several kV)
- Limited Current (due to series resistor of 1.5k Ω (JEDEC) or 330 Ω (IEC))
- Limited Duration (due to small capacitance of 100pF (JEDEC) 150pF (IEC))

resulting into

- Limited Energy-Content

requiring primarily

- Spacing to avoid arcing

Voltage Transients have

- Limited Voltages (several 100V)
- High Current (due to limited resistance)
- Relatively long Duration (50us till half amplitude)

resulting into

- High Energy-Content

requiring primarily

- high Power Dissipation
- Large Silicon-Area causing high Capacitances (->Limited Signaling Rate)

Note: External Protection Diodes have the same Causal-Chain and may react slower than the Transceivers Protection-Circuitry, resulting into failing to protect!

1 - 36

As we have seen throughout the past slides, different ESD-threads exist that origin from multiple sources. Even though the associated voltages are extremely high, due to low storage-capacity, the energy content is limited. With appropriate spacing, ESD is relatively easy to address. A much more dangerous incident origin from power-surges or transients: despite being of lower voltages, the power involved as well as the duration is much higher. The resulting energy content is way higher. To dissipate the heat generated during such a strike, a large silicon-area is required. In CMOS-technology, this comes along with high capacitances and consequently limited signalling rates.

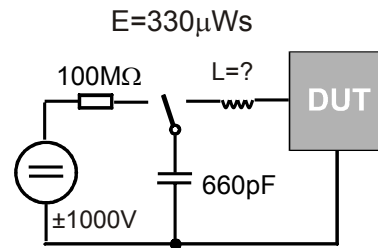
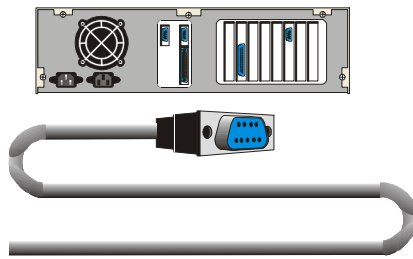
Below table shows some examples of different origins and their impact.

	Voltage	Current	Rise-Time	Duration
Lighting	25kV	20kA	10us	1ms
Switching	600V	500A	50us	500ms
EMP	1kV	10A	20ns	10us
ESD	15kV	30A	<5ns	100ns

A frequent approach to deal with such threads is external protection, e.g. using *suppressor diodes*. An almost as frequent neglect is the fact that devices that survive such high energy-surges present a high capacitance themselves. Worst case, those might fail to protect the downstream hardware, because the transceivers' own protection reacts quicker than the external one as is blown. In any case, the addition capacitance has to be considered as a limiting factor for the signalling rate.



Real World ESD Test Connection of a charged Cable



A cable with a length of 10 m ($C = 660 \text{ pF}$) is connected to an electronic equipment. The energy stored in the capacitance of the cable is discharged into the electronic components of the interface circuitry.

1 - 38

All the tests shown above do not show by far the rough treatment which may happen to interface circuits. At typical situation is the following: a modem needs to be connected to a personal computer. The modem is placed at one end of the room, the computer at the other end, with 10 m between these two equipments. The man who installs the cable walks through the room over carpet, which, as is well-known, generates high electrostatic charge. By keeping one end of the cable in his hand, the cable may be charged up to a voltage $V=1000\text{V}$. When the cable is now connected to the equipment, the capacitance of the cable $C=660\text{pF}$ (maximum allowable capacitance for twisted pair $6.6\text{nF}/100\text{m}$) is discharged into the interface circuits. The energy to be absorbed under this condition is far higher than that found in the previous test standards:

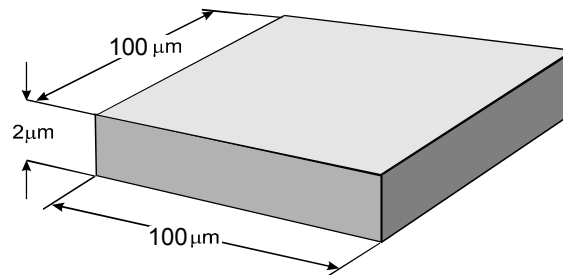
$$E_a = 0.5 \cdot V^2 \cdot C = 0.5 \cdot 1000^2 \text{V}^2 \cdot 660 \text{ pF} = 330 \mu\text{Ws}$$

There are many more standards that describe circuitries to test the robustness of semiconductors. The most important ones are:

- IEC 61000-4-2 (ESD Immunity)
- IEC 61000-4-3 (Radiated Immunity)
- IEC 61000-4-4 (Fast Transient Immunity)
- IEC 61000-4-5 (Surge Immunity)

Temperature in a protection circuit

The protection network inside an integrated circuit has to absorb the energy during the electrostatic discharge described above. The discharge time is relatively short. In the case of the charged cable the discharge time is twice the propagation time of a wave on the cable equaling to $2 \times 10 \text{ m} \times 5 \text{ ns/m} = 50 \text{ ns}$. During this time energy is injected into the protection circuit. It is further assumed that the protection circuit occupies an area of $100 \times 100 \mu\text{m}^2$, and that the depth of the junction is 2 mm , which results in a volume $V_s = 20 \times 10^{-6} \text{ mm}^3$.



Considering that the thermal propagation time of the heat wave in the silicon crystal is about 1 mm/ms , one can say that during the first microseconds the total heat will stay in the protection circuit. By knowing the thermal capacitance of silicon $C_s = 1.631 \text{ Ws/Kcm}^3$, the temperature increase $\Delta \theta$ in the protection network can be calculated:

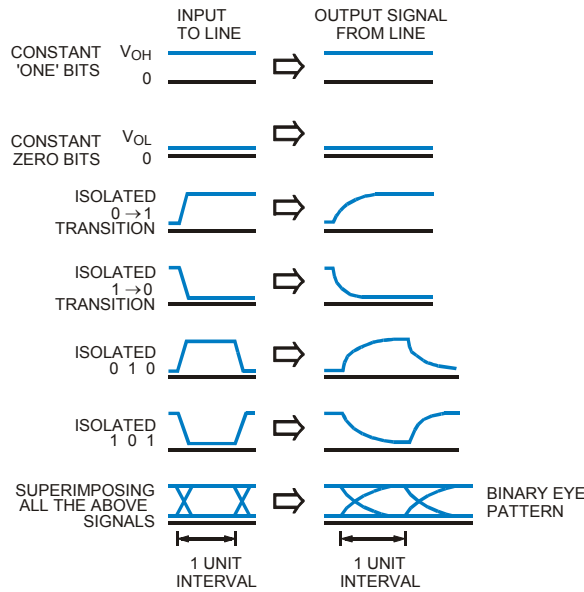
$$\Delta \theta = \frac{E_a}{V_s \cdot C_s} = \frac{330 \mu\text{Ws}}{20 \cdot 10^{-6} \text{ mm}^3 \cdot 1.631 \text{ Ws / Kcm}^3} = 10116 \text{ K}$$

The melting temperature of silicon is about 1600°C . The aluminum metallization - already melted at much lower temperatures - will diffuse into the silicon. The normally high impedance ESD protection circuit becomes a short circuit.

Sometimes, external protection methods are used, e.g. suppressor diodes like Transzorb™. Note, that care must be taken regarding the layout, as the inductance in the trace may cause the Transzorb™ to act too slow and the transceiver may be harmed before the diode starts conducting.



Contributions to the Eye Pattern



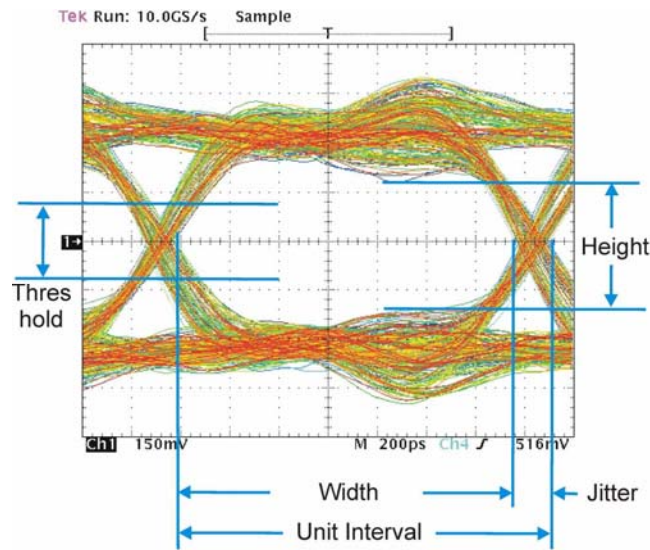
1 - 40

The above diagrams show left sided the signal at the begin of a transmission line, on the right side is the signal seen at the end of a line. The first line equals a long transmission of a high level, below it, a continuous transmission of a low level is seen. Furthermore a low to high and a high to low transition is displayed. Following an alternating pattern is given, showing that at the end of the line, no steady state will be reached, because the opposite signal level is applied, before the signal achieves it steady state.

At the very bottom, one can see the superposition of the above signals, which is referred to as eye-pattern.



Eye-pattern - Parameters



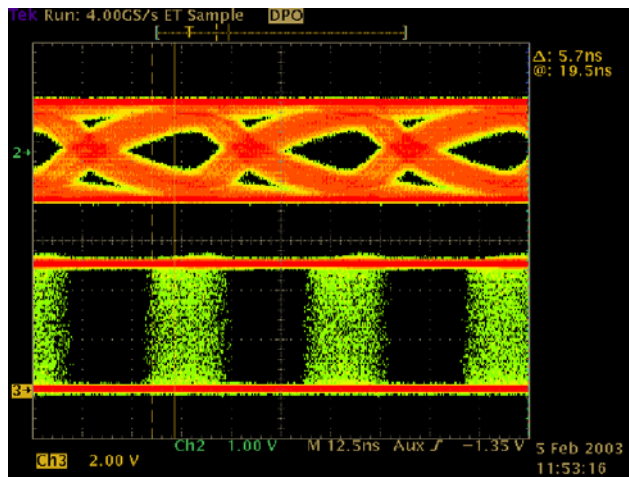
1 - 41

The graph above shows a typical eye-pattern, here taken on a heavily loaded backplane, transferring a LVDM-signal. The most important parameters are labeled:

- Unit interval indicates the length of a bit
- Jitter is the duration, during which transitions occur. Sampling during the jitter will most likely cause bit errors. The jitter is sometimes given as an absolute number (in ps, etc) or as a percentage of the unit interval. The jitter may be measured at the eye-crossing as indicated above or at the threshold.
- The height, measured during the “hold state” in which the sampling should occur, indicates the minimum signal amplitude that will be achieved worst case (based on measurement conditions).
- The threshold indicates the amplitude at which the receiver will switch worst case. The difference between the height and the threshold indicates the noise margin.



Eye Pattern



Measurement conditions:

Data rate: 25Mbps

Cable: Twisted pair

Cable length: 160m

1 - 42

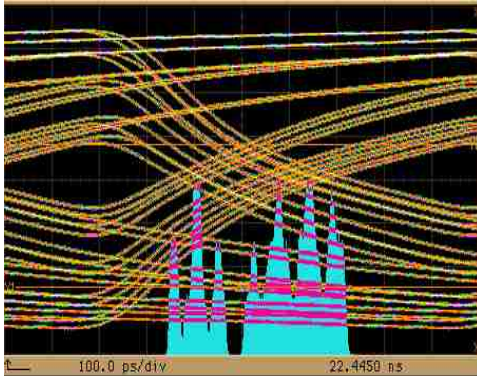
The transfer characteristic of a twisted pair cable has been tested, using PRBS (Pseudo Random Bit Sequence) pattern. The cable has length $l=160\text{m}$ and wire diameter $d=0.6\text{mm}$. The data rate of this NRZ-signal (Non Return to Zero, i.e. a signal that may have a DC content) is 25Mbps (Megabit per second, bit duration 40ns). The signal at the beginning (upper trace in the above picture) is a square wave. At the line end the low-pass filter performed by the cable slows down the rise time as well as the amplitude (lower trace). The ohmic resistance of the wire has only a minor influence when comparing the peak voltages at the beginning and the end of the line.

The majority of the signal quality degradation is caused by the frequency dependent losses (skin effect). The voltage swing and the time interval left for recovering the transmitted information is the eye shaped window in the signal flow. The height of the window gives the effective signal amplitude which has to be detected by the receiver circuit. The width of the eye determines the final time interval in which the information has to be sampled. This transition time variation is called jitter. Therefore in many receiver systems one can find a sophisticated clock recovery circuit to regenerate the original timing (clock) of the information for correct sampling of the data.

More examples of jitter in actual applications will be shown in the respective sections.



ISI – Inter-Symbol Interference



- Inter-Symbol Interference describes the influence of preceding bit(s) to the current one, respectively the influence of the current bit on the following transmission
- ISI may be considered as a memory-effect of the transmission system
- The Jitter in the graph on the left is very small, but due to ISI, the eye-opening still appears very small
- The main contributors are
 - charged capacitances (cables, I/O's, etc) which determine the starting point for the next transition
 - Reflections (of previous bits)

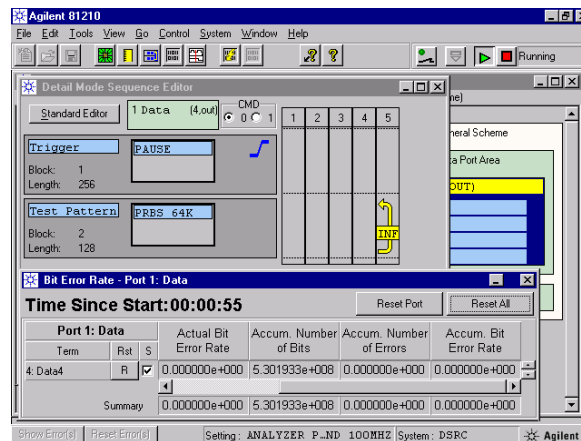
1 - 43

ISI (Inter Symbol Interference) defines the influence of previous bits on the current transmission. Charged capacitances, e.g. of the cable, the transceivers I/O's, etc., effect the actual "starting point" of the transition. E.g. after a long series of high level bits, the bas capacitance will be charged to a higher level, than after a single high-bit. Therefore, the high-low-transition begins at a higher level and will reach the threshold later. Reflections (from previous bits) that superimpose with the current signal add even more variance. The graph above shows clearly the low jitter, but the eye is still almost closed due to the ISI.



BERT

- BERT stands for Bit Error Rate Test(ing)
- Measure to test the signal accuracy (quality and integrity)
- PRBS (Pseudo Random Bit Sequence), Worst Case Pattern or Coded Data is sent
- Analyzer compares received data to stored original
- Benchmark is mostly a BER of 10^{-12}



1 - 44

BERT is the abbreviation for Bit Error Rate Test (sometimes Testing or Tester). A BERT is used to determine the signal quality and integrity at a point in the data-flow. It might be e.g. the input to the receiver at the end of a cable or bus or the recovered signal at the output of the receiver which the downstream equipment has to work with. The pattern sent is often PRBS, or, if known, the actual application data, here mostly worst case. If the application uses a coding scheme, this is often used for the tests as well. The same pattern that is sent via the data path of concern is also provided to the analyzer, mostly as a file, sometimes by capturing that data after a “error-free” transmission. The analyzer compares the received data to the original and counts the errors. Advanced testers can also provide the actual point of error within the data-stream, which helps finding solutions. Often a BER of 10^{-12} or less is the goal to be achieved.



Basics Section Review

- Single Ended vs. Differential
- Multidrop vs. Multipoint
- Transmission Line Theory
- Wave Analysis
- Line Reflections & Termination Practices
- Crosstalk
- Failsafe
- Tests associated with Signal Transmission
 - Electro Static Discharge (ESD)
 - Eye-Pattern
 - Inter Symbol Interference (ISI)
 - Bit Error Rate Testing (BERT)

1 - 45