4.4. DSP [Pass] / [Fail]

4.4.1. Clock [Pass]

Goal:
Qualify the DSP board clock

Initials	JVA		Board release:	R01
Date	24-10-2012		SN	12-28-001-828
			POC release	N/A

Measurement setup:
Master: Setup 1 – no master
EEQDM: Setup 1 – default

Method:

- Follow the measurement preparations as described with the setup.
- Measure at clock target
  - DC levels
  - Duty cycle

Results:

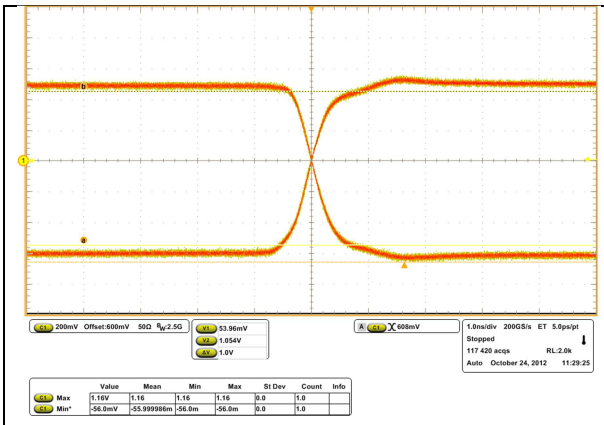


Figure 4-175: DSP_CLK_U300_max_min

Goal: Determine SI of DSP_CLK input at the DSP.

S1 (PA2596): DSP_CLK@U300 (Via near L19)
Scope DPO7254; SN1799

Parameter	Value	Measured
V_{il}	<0.24V	0.054V
V_{ih}	>0.96V	1.054V
V_{min}	>-0.3V	-0.056V
V_{max}	<1.5V	1.16V
Duty cycle	40..60%	+50.44 % -49.56 %

Conclusion: DSP Clock is OK

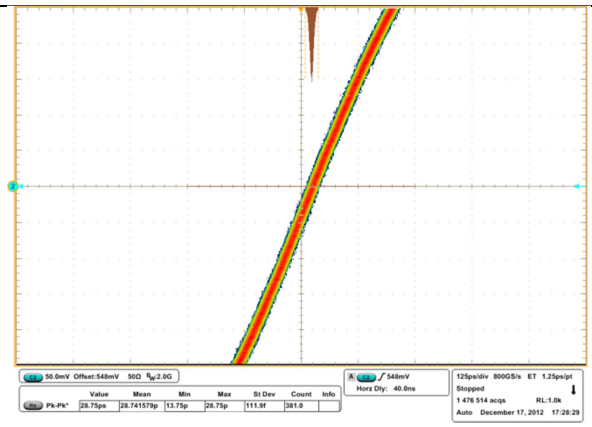


Figure 4-176: DSP_CLK_U300_jitter

Goal: Determine jitter of DSP_CLK input at the DSP(informative)

S1 (PA0786): DSP_CLK@U300 (Via near L19)
Scope DPO7254; SN0747

Parameter	Value	Measured
Period jitter	N/A	28.75ps

Conclusion: Jitter is small as expected

Conclusion: clock of the DSP is OK

4.4.2. JTAG [Pass]

Goal:
Qualify the DSP JTAG (only functional)

Initials	MVK		Board release:	R01
Date	2012		SN	12-28-001-828
			POC release	N/A

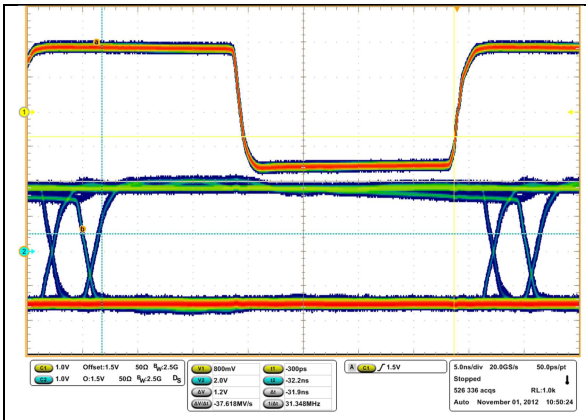


Figure 4-187: HPI_READ_DATA_SETUP_timing

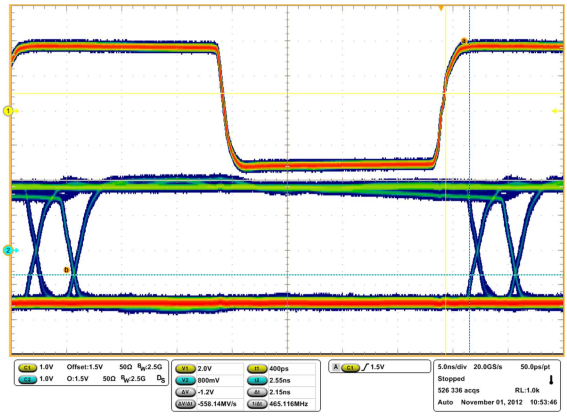


Figure 4-188: HPI_READ DATA_HOLD_timing

Goal: Verify HPI timing at FPGA

S1 (Ye, PA2596): FPGA_CLK@100 (P21)
S2 (Ye, PA2596): HPI_D1@U100 (A18)
Scope DPO7254; SN1799

Param	Req.	Measured	Remark
t_{su}	>10ns	31.9ns	Data setup
$t_{h(}$	>0ns	2.15ns	Data hold

Conclusion: Timing is OK

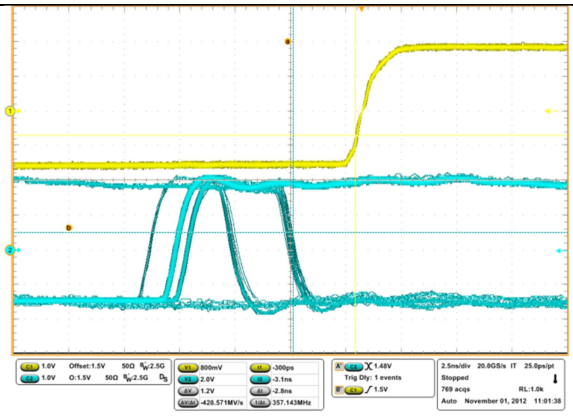


Figure 4-189: HPI_READ_RDY_SETUP_timing

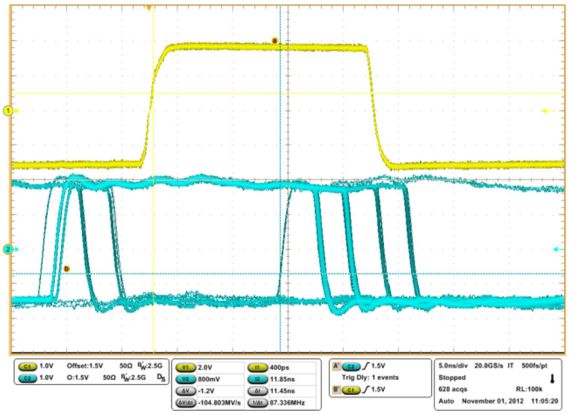


Figure 4-190: HPI_READ RDY_HOLD_timing

Goal: Verify HPI timing at FPGA

S1 (Ye, PA2596): FPGA_CLK@100 (P21)
S2 (Ye, PA2596): HPI_HRDY_n@U300 (H17)
Scope DPO7254; SN1799

Param	Req.	Measured	Remark
t_{su}	>10ns	2.6ns	Rdy setup
$t_{h(}$	>0ns	11.45ns	Rdy hold

Conclusion: Setup time violates with constraining in UCF. But the ready signal is threated asynchronous in the FPGA so there are no real timing requirements ➔ Pass

Conclusion: HPI Timing and SI is OK

4.4.4. DRAM [Pass] / [FAIL]

Goal: Verify SI and of the DRAM interface

Initials	JVA		SN	12-30-011-400
Date	04-12-2012		POC DSP	

Measurement setup:
Master: Setup 1 – no master
EEQDM: Setup 1 – default

Measurement:

- Power EEDQM
- Create DRAM Activity (DSP Code)
- Use Tektronix DDR Analysis tool to analyze the DRAM interface

4.4.4.1.Voltage levels [PASS]

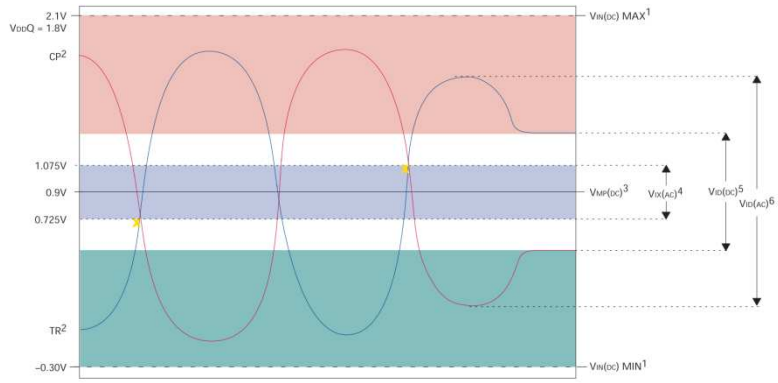
Goal: Measure the voltage levels, slew rate and jitter of the DDR interface.

4.4.4.1.1.Clock [FAIL]

Initials	JVA		SN	12-30-011-400
Date	04-12-2012		POC DSP	Debug version with read/write loop

Measurement remarks:

- Measure CK on DRAM
- CK must be measured single ended and differential according to the picture below



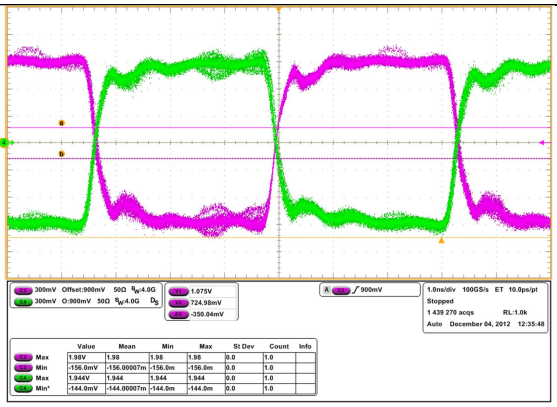


Figure 4.191: DDR_CK_DC

Goal: Verify the crossing levels of the DDR2 clock

S3 (Pu, PA827): DDR_CK_P@ U501(J8)
S4 (Gn, PA828): DDR_CK_N@ U501(K8)
Scope SN2848

Parameter		Required	Measured
$V_{IN,DC}$	Max	< 2.1V	1.98V
	Min	> -300mV	-156mV
$V_{ID,DC}$	Max	< 2.1V	NA
	Min	> 250mV	
$V_{IX,AC}$	Max	<1075mV	PASS
	Min	>725mV	

Note: the VID(DC) is the minimum value when the differential signal is static incase if there is an overshoot or undershoot in the signal.
No overshoot and undershoot, measure VID(AC)

Conclusion:Voltage levels are OK
The single ended voltage levels are OK

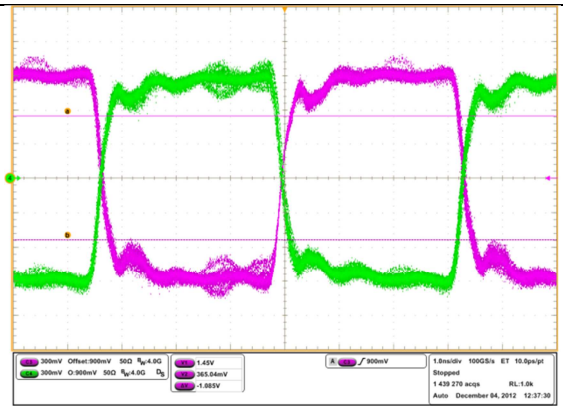


Figure 4.192: DDR_CK_AC

Goal: Verify the AC voltage levels of the DDR2 clock
POC FPGA: B160

S2 (Pu, PA827): DDR_CK_p @ U501 (J8)
S3 (Gn, PA827): DDR_CK_n @ U501 (K8)
Scope SN2848

Parameter		Required	Measured
$V_{ID,AC}$	Max	< 2.1	1.085V
	Min	> 500mV	

Conclusion:
The voltage levels are OK

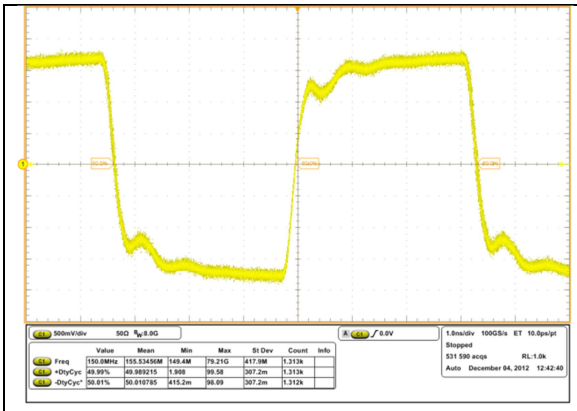


Figure 4.193: DDR_CK _DUTY_CYCLE

Goal: Verify the frequency and duty cycle of the clock

S1 (Ye, PD2375): DDR_CK @ U501(J8/K8) (differential)
Scope SN2848

Param	Required	Measured
-Duty-cycle	>48%	49.99%
+Duty-cycle	<52%	50.01%
Frequency	150MHz	150MHZ

Conclusion:
Duty cycle and frequency are OK (multiplier set to 12)

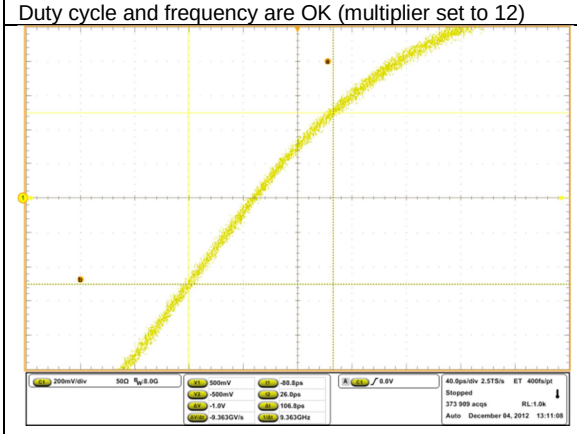


Figure 4.194: DDR_CK_RISE

Goal: Verify the slew rate of the clock
POC FPGA: B160

S1 (Ye, PD2375): DDR_CK @ U501(J8/K8) (differential)
Scope SN2848

Param	Required	Measured
Rise	Used for derating	4.68V/ns

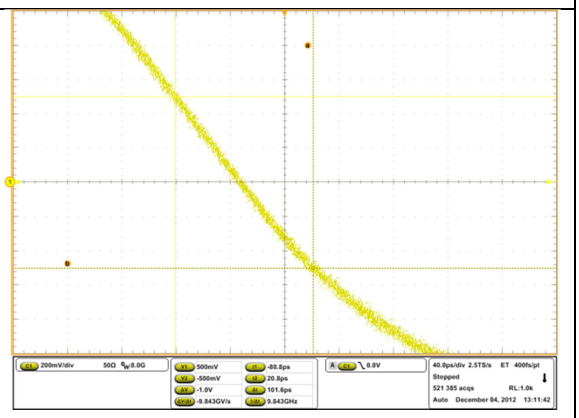


Figure 4.195: DDR_CK_FALL

Goal: Verify the slew rate of the clock
POC FPGA: B160

S1 (Yel, PD2375): DDR_CK @ U501(J8/K8) (differential)
Scope SN2848

Param	Required	Measured
Fall	Used for derating	4.92V/ns

Note that the measurements are done with a differential probe so the slew rate must be divided by 2.

4.4.4.1.1.1.Clock Jitter [FAIL]

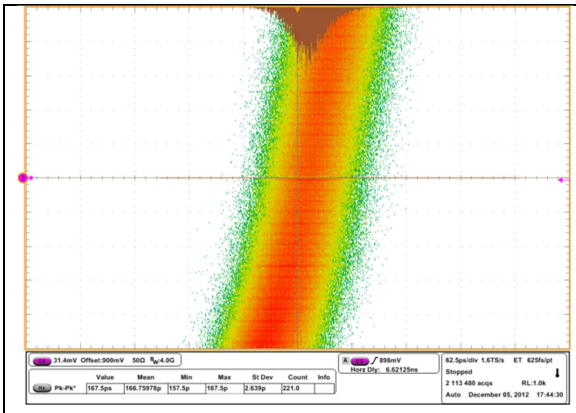


Figure 4.196: DDR_CK0_PERJITTER_MAN

Goal: Measure the period jitter using the Manual method (informative)

S3 (Pu, PA2366): DDR_CK_p @ U501(J8)
Scope SN2848

Param	Required	Measured
$T_{PJ(max)}$	-100ps < $T_{PJ(max)}$ < 100ps	167 (pk-pk)

Conclusion: The peak peak period jitter is within requirements but on the high side

Description	Mean	Std Dev	Max	Min	p-p	Max-cc	Min-cc
tJIT(per), CK	NA	NA	93.711ps	-87.383ps	NA	NA	NA
tJIT(duty), CK	NA	NA	61.827ps	-58.027ps	NA	NA	NA
tJIT(cc), CK	2.0161fs	29.286ps	138.88ps	-124.12ps	263.00ps	222.40ps	-231.36ps
tERR(2per), CK	NA	NA	120.22ps	-145.35ps	NA	NA	NA
tERR(3per), CK	NA	NA	163.73ps	-175.78ps	NA	NA	NA
tERR(4per), CK	NA	NA	210.30ps	-192.25ps	NA	NA	NA
tERR(5per), CK	NA	NA	246.67ps	-242.30ps	NA	NA	NA
tERR(6-10per), CK	NA	NA	448.78ps	-427.11ps	NA	NA	NA
tCH(avg), CK	501.11mtCK(avg)	106.05utCK(avg)	501.41mtCK(avg)	500.73mtCK(avg)	682.69utCK(avg)	37.818utCK(avg)	-31.491utCK(avg)
tCL(avg), CK	498.89mtCK(avg)	106.05utCK(avg)	499.27mtCK(avg)	498.59mtCK(avg)	682.69utCK(avg)	31.491utCK(avg)	-37.818utCK(avg)

Figure 4.197: DDR_CK0_PERJITTER

Goal: Measure the period jitter using the DPOJET (DDR Software)

S1 (Ye, PD2375): DDR_CK_p @ U501(J8/K8) (Diff)
Scope SN2848

Param	Required (DDR-800)	Required DDR-400	Measured
tJIT(per), CK	Min: -100ps Max +100ps	Min: -125ps Max +125ps	-87.383ps +93.711ps
tJIT(duty), CK	Min: -100ps Max +100ps	Min: -125ps Max +114 ps	-58.027ps 61.827ps
tJIT(cc), CK	Max 200 ps	Max 250 ps	222.40ps
tERR(2per), CK	Min: -150ps Max +150ps	Min: -175ps Max +175ps	-145.35ps 120.22ps

tERR(3per), CK	Min: -175ps Max +175ps	Min: -225ps Max +225ps	-175.78ps 163.73ps
tERR(4per), CK	Min: -175ps Max +175ps	Min: -250ps Max +250ps	-192.25ps 210.30ps
tERR(5per), CK	Min: -175ps Max +175ps	Min: -250ps Max +250ps	-242.30ps 246.67ps
tERR(6-10per), CK	Min: -300ps Max +300ps	Min: -350ps Max +350ps	-427.11ps 448.78ps
tCH(avg), CK	0.48..0.52 tCK (avg)	0.48..0.52 tCK (avg)	500.73…501.41 mtCK(avg)
tCL(avg), CK	0.48..0.52 tCK (avg)	0.48..0.52 tCK (avg)	498.59…499.27 mtCK(avg)

Conclusion: Jitter is too high (even when the DRAM is only doing refresh cycles).
Input clock jitter and supply noise are OK

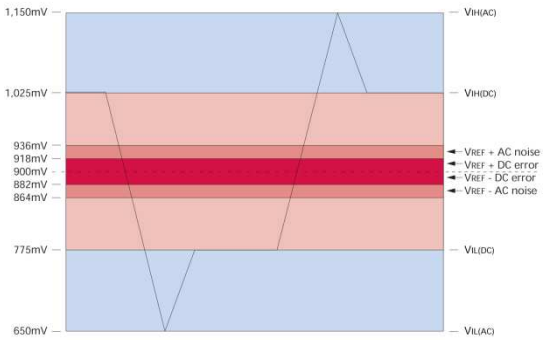
Conclusion:

4.4.4.1.2.DQS [PASS]

Initials	JVA		SN	12-30-011-400
Date	04-12-2012		POC DSP	

Measurement remarks:

- Measure DQS as close as possible to the BGA balls
- Use P7313 for measuring DQS



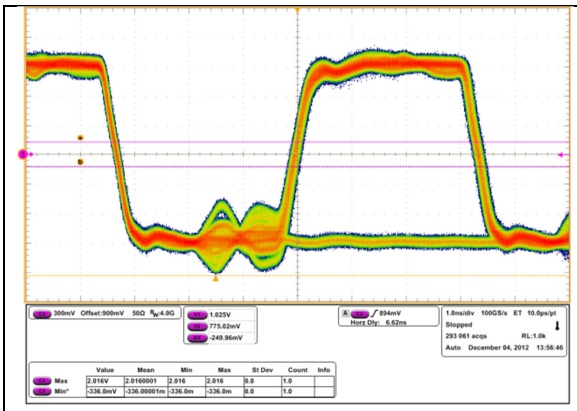


Figure 4.198: DDR_LDQS_WRITE

Goal: Verify the crossing levels of the DQS

S3 (Pu, PA2366): DDR_LDQS@ U501(B7)
Scope SN2848

Param	Required	Measured
$V_{IH,AC}$	< 2.1V	*2.016V*
$V_{IL,AC}$	>-0.3 V	*-336 mV*
$V_{IH,DC}$	> V_{REF} + 0.125	*Pass*
$V_{IL,DC}$	< V_{REF} – 0.125	*Pass*

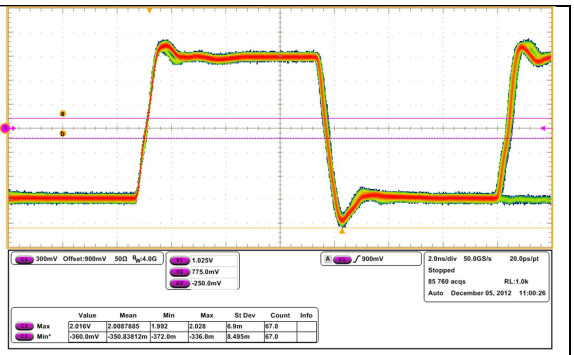


*Figure 4.*199: DDR_L DQS_READ

Goal: Verify the levels of the DQS (reduced drive strength)

S3 (Pu, PA2366): DDR_LDQS@ U300(T14)
Scope SN2848

Param	Required	Measured	Remarks
$V_{IH,AC}$	< 2.1V	2.028V	
$V_{IL,AC}$	>-0.3 V	-275 mV	Zoomed in
$V_{IH,DC}$	> V_{REF} + 0.125	Pass	
$V_{IL,DC}$	< V_{REF} – 0.125	Pass	

Conclusion: Levels are OK

Conclusion: Some crosstalk cause by the data signals but outside the threshold levels (cursors). The undershoot (caused by the crosstalk) is too high but within absolute max values (-0.5V) ➔ OK

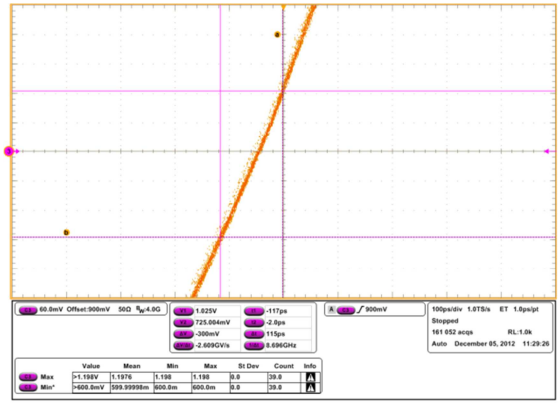


Figure 4.200: DDR_LDQS_RISE

Goal: Verify the slew rate of the DQS

S3 (Purple, PA2366): DDR_LDQS @U501(B7)
Scope SN2848

Param	Required	Measured
Rise	Used for derating	2.609V/ns

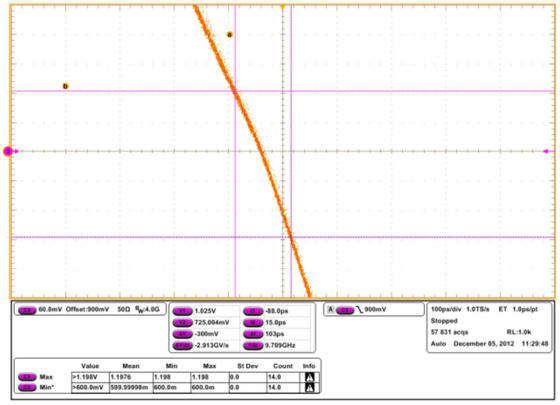


Figure 4.201: DDR_LDQS_FALL

Goal: Verify the slew rate of the DQS

S3 (Purple, PA2366): DDR_LDQS @U501(B7)
Scope SN2848

Param	Required	Measured
Fall	Used for derating	2.931V/ns

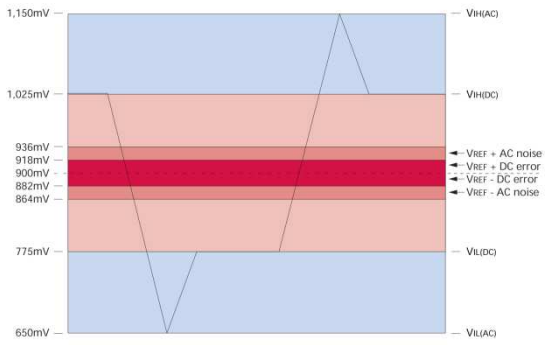
Conclusion: DQS is OK

4.4.4.1.3.DQ [PASS]

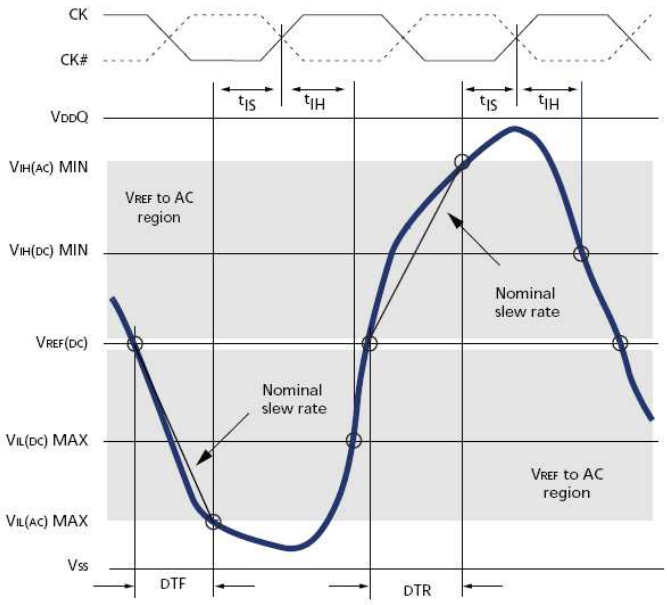
Initials	JVA		SN	12-30-011-400
Date	05-12-2012		POC DSP	

Measurement remarks:

- Measure DQ as close as possible to the BGA balls
- DQ must be measured single ended according to the picture below



- t_{DH} nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)\ MAX}$ and the first crossing of $V_{REF(DC)}$. T_{DH} nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)\ MIN}$ and the first crossing of $V_{REF\ (DC)}$. For more information see the picture below



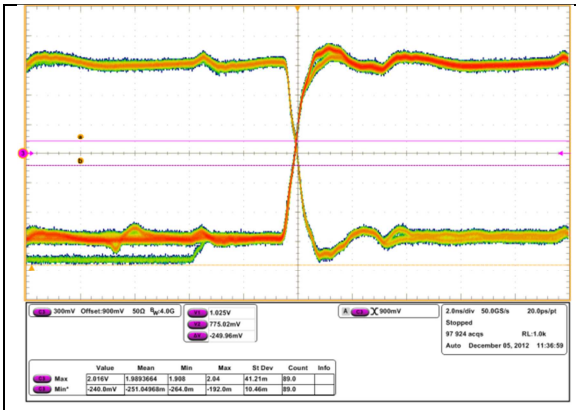


Figure 4.202: DDR__DQ_WRITE

Goal: Verify the voltage levels of the DQ. DQ is measured while writing

S3 (Pu, PA2366): DDR_DQ0 @U501(B9)
Scope SN2848

Param	Required	Measured
$V_{IH,AC}$	< 2.1V	2.04V
$V_{IL,AC}$	>-0.3 V	-0.264V
$V_{IH,DC}$	> V_{REF} + 0.125	Pass
$V_{IL,DC}$	< V_{REF} – 0.125	Pass

Conclusion: Write DQ SI is OK

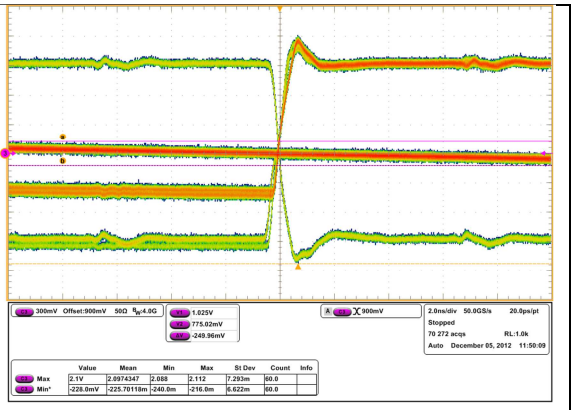


Figure 4.203: DDR_DQ_READ

Goal: Verify the voltage levels of the DQ. DQ is measured while reading

S3 (Pu, PA2366): DDR_DQ @U300(U15)
Scope SN2848

Param	Required	Measured	Remarks
$V_{IH,AC}$	< 2.1V	2.011V	Zoomed in
$V_{IL,AC}$	>-0.3 V	-240mV	
$V_{IH,DC}$	> V_{REF} + 0.125	Pass	
$V_{IL,DC}$	< V_{REF} – 0.125	Pass	

Conclusion: Read DQ SI is OK

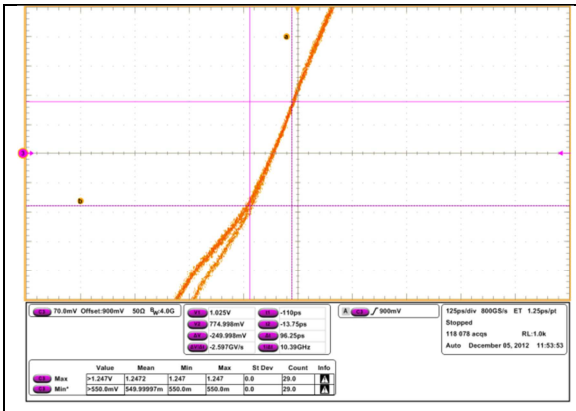


Figure 4.204: DDR_DQ_RISE

Goal: Verify the slew rate of the DQ

S3 (Pu, PA2366): DDR_DQ0 @U501(B9)
Scope SN2848

Param	Required	Measured
Rise	Used for derating	2.597V/ns

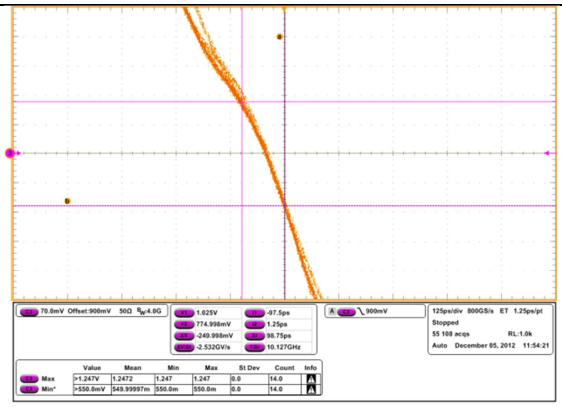


Figure 4.205: DDR_DQ_FALL

Goal: Verify the slew rate of the DQ

S3 (Pu, PA2366): DDR_DQ0 @U501(B9)
Scope SN2848

Param	Required	Measured
Fall	Used for derating	2.532V/ns

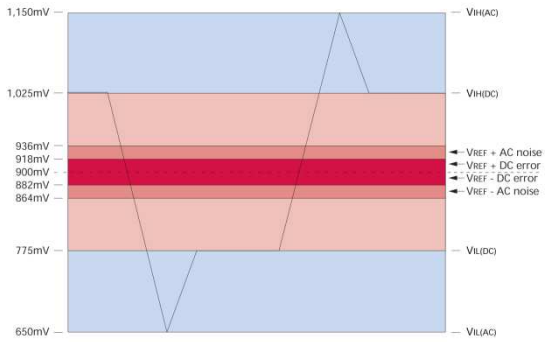
Conclusion: DQ levels are OK

4.4.4.1.4.Address/Control [PASS]

Initials	JVA		SN	12-30-011-400
Date	05-12-2012		POC DSP	

Measurement remarks:

- Measure Address and control as close as possible to the BGA balls
- Address and control must be measured single ended according to the picture below



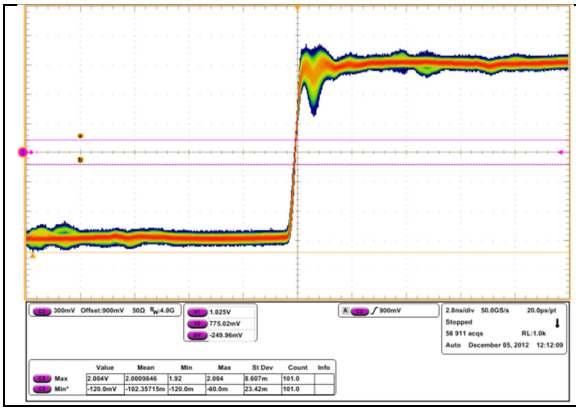


Figure 4.206: DDR_A0_SI_RISE

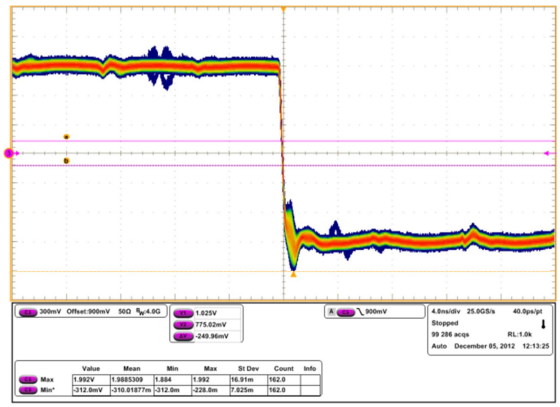


Figure 4.207: DDR_A0_SI_FALL

Goal: Verify the voltage levels of the address/control

S3 (Pu, PA2366): DDR_A0 @ U501(M8)
Scope SN2848

Param	Required	Measured	Remarks
$V_{IH,AC}$	< 2.1V	2.004V	
$V_{IL,AC}$	>-0.3 V	-0.28V	Zoomed in
$V_{IH,DC}$	> V_{REF} + 0.125	PASS	
$V_{IL,DC}$	< V_{REF} – 0.125	PASS	

Conclusion: SI of Address / Control is OK

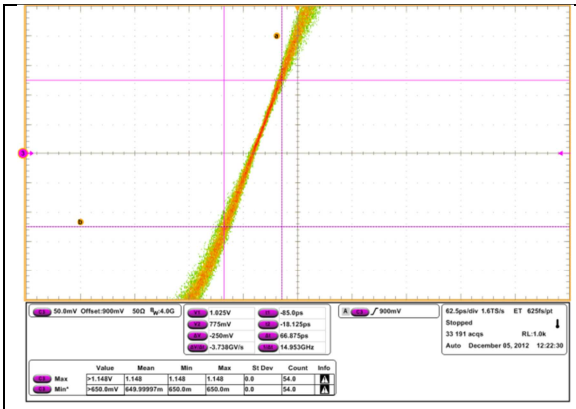


Figure 4.208: DDR_A0_RISE

Goal: Verify the slew rate of the address/control signals

S3 (Pu, PA2366): DDR_A0 @ U501(M8)
Scope SN2848

Param	Required	Measured
Rise	Used for derating	3.738V/ns

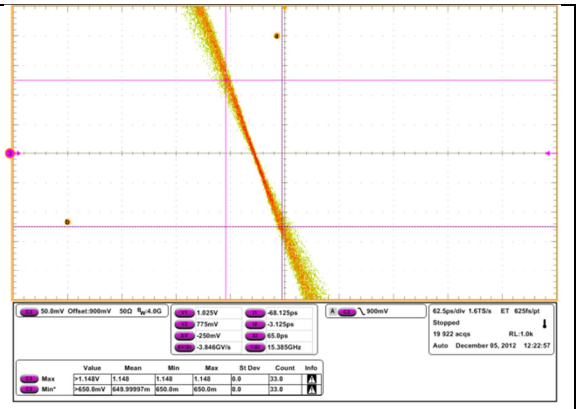


Figure 4.209: DDR_A0_FALL

Goal: Verify the slew rate of the address/control signals

S3 (Pu, PA2366): DDR_A0 @ U501(M8)
Scope SN2848

Param	Required	Measured
Fall	Used for derating	3.846V/ns

Conclusion: SI of Address /Control is OK

4.4.4.2.Timing [PASS]

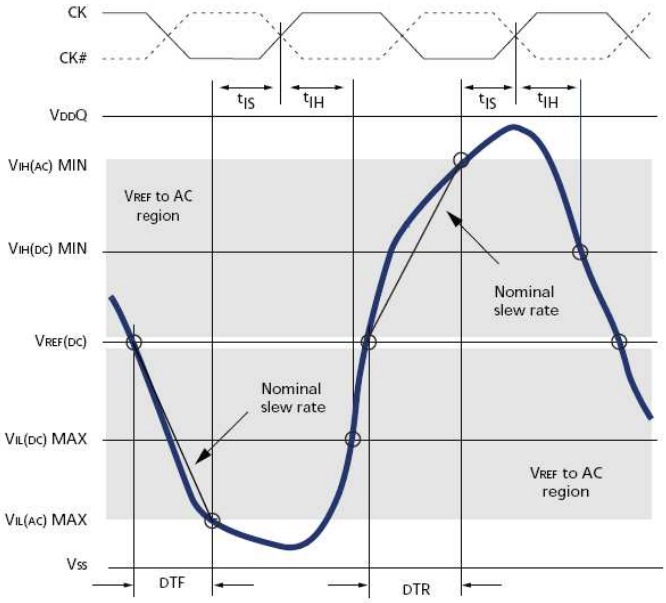
Goal: Measure the timing of the DDR2 interface

Initials	JVA		SN	12-30-011-400
Date	05-12-2012		POC DSP	

4.4.4.2.1.Address/Control [PASS]

Measurement remarks:

- Measure Address and control as close as possible to the BGA balls
- Address and control must be measured single ended
- t_{IS} is referenced from $V_{IH(AC)}$ for a rising signal and $V_{IL(AC)}$ for a falling signal, while t_{IS} is referenced from $V_{IL(DC)}$ for a rising signal and $V_{IH(DC)}$ for a falling signal (see the figure below).



- If the differential CK slew rate is not equal to 2 V/ns, then the baseline values must be derated as seen in the table below
- If the single ended address/command slew rate is not equal to 1 V/ns, then the baseline values must be derated as seen in the table below

Signal	Measured Slew Rate	Slew rate derating according to Ref [3.1] table 29	Derating value	Remarks
CK,CK#	2.34V/ns=4.68ns/2	2.0V/ns	Derating setup: +150ps Derating hold: +94ps	A lower slew rate corresponds to a higher setup/hold margin
Address	3.846V/ns	4V/ns		A higher slew rate corresponds to a higher setup/hold margin

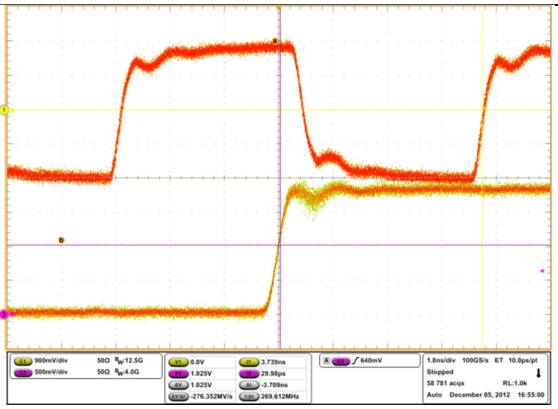


Figure 4.210: DDR_A0_SETUP

Goal: Verify setup time of the address/control bus

S1 (Ye, PD2375): DDR_CK @ U501(J8/K8) (diff)
S3 (Pu, PA2366): DDR_A0 @ U501(M8)
Scope SN2848

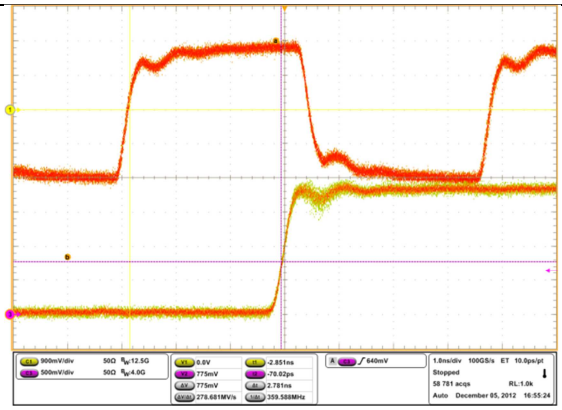


Figure 4.211: DDR_A0_HOLD

Goal: Verify hold time of the address/control bus

S1 (Ye, PD2375): DDR_CK @ U501(J8/K8) (diff)
S3 (Pu, PA2366): DDR_A0 @ U501(M8)
Scope SN2848

Param	Required	Measured
T_{IS}	>0.175ns +150ps (derating)	3.709ns

Conclusion: Setup time is OK

Param	Required	Measured
T_{IH}	>0.250ns + 94ps (derating)	2.78ns

Conclusion: Hold time is OK

Conclusion: Address/control timing is OK

4.4.4.2.2.Write timing (DQS to CK) [PASS]

Measurement remarks:

- Measure DQS and CK as close as possible to the BGA balls

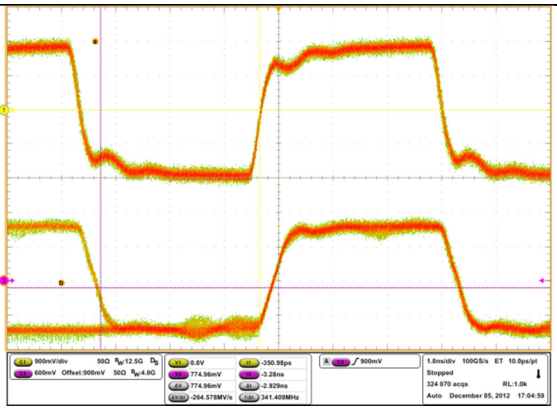


Figure 4.212: DDR_DQS_CK_SETUP

Goal: Verify the setup time of the DQS falling edge to the CLK rising edge

S1 (Ye, PD2375): DDR_CK @ U510(J8/K8)(diff)
S3 (Pu, PA2366): DDR_LDQS @ U510(B7)
Scope SN2848

Param	Required	Measured	Remarks
T_{DSS}	>1.33ns	2.929ns	0.2*T_{CK}

Conclusion: Setup time is OK

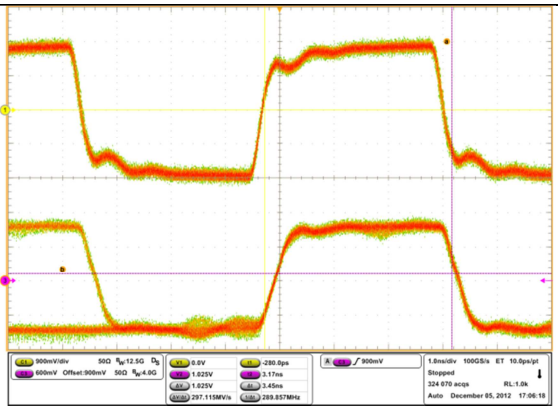


Figure 4.213: DDR_DQS_CK_HOLD

Goal: Verify the hold time of the DQS falling edge from the CLK rising edge

S1 (Ye, PD2375): DDR_CK @ U510(J8/K8)(diff)
S3 (Pu, PA2366): DDR_LDQS @ U510(B7)
Scope SN2848

Param	Required	Measured	Remarks
T_{DSS}	>1.33ns	3.45ns	0.2*T_{CK}

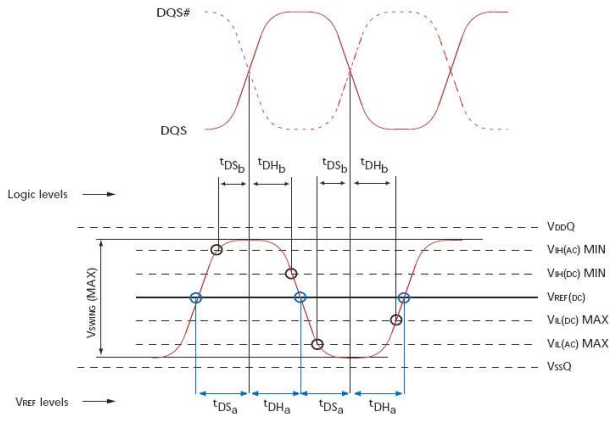
Conclusion: Hold time is OK

Conclusion: timing is OK

4.4.4.2.3.Write timing (DQ to DQS) [PASS]

Measurement remarks:

- Measure DQS and DQ as close as possible to the BGA balls
- Deskew probes
- t_{DSb} is referenced from $V_{IH(AC)}$ for a rising signal and $V_{IL(AC)}$ for a falling signal, while t_{DHb} is referenced from $V_{IL(DC)}$ for a rising signal and $V_{IH(DC)}$ for a falling signal (see the figure below).



- If the differential DQS slew rate is not equal to 2 V/ns, then the baseline values must be derated as seen in the table below
- If the single ended DQ slew rate is not equal to 1 V/ns, then the baseline values must be derated as seen in the table below

Signal	Measured Slew Rate	Slew rate derating	Derating value	Remarks
DQS	2.609V/ns	2.0V/ns	Derating setup: +330ps Derating hold: +291ps	A lower slew rate corresponds to a higher setup/hold margin. From Micron datasheet Table 33
DQ	2.597V/ns	2.0V/ns		A higher slew rate corresponds to a higher setup/hold margin From Micron datasheet Table 33

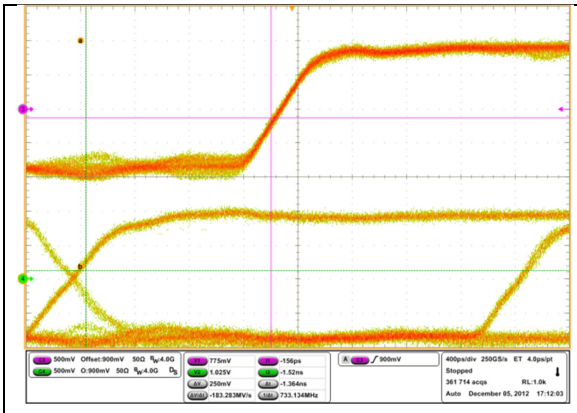


Figure 4.214: DDR_DQ_DQS_WRITE_SETUP_RISING

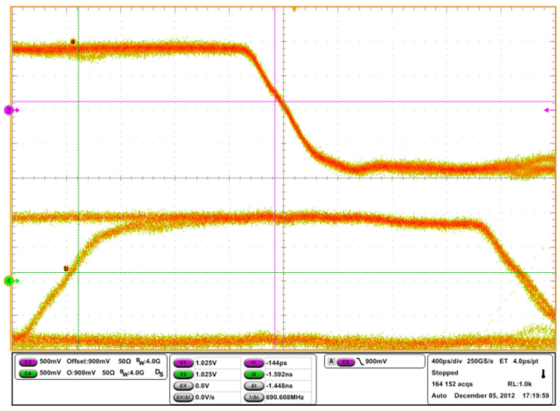


Figure 4.215: DDR_DQ_DQS_WRITE_SETUP_FALLING

Goal: Verify the setup time of DQ to DQS

S3 (Pu, PA2366): DDR_LDQS @ U501(B7)
S4 (Gn, PA827): DDR_DQ0 @ U501(B9)
Scope SN2848

Param	Required	Measured
T_{DSb}	>0.050ns + 330ps (derating)	1.36ns(R) 1.44ns(F)

Conclusion: Setup time is OK

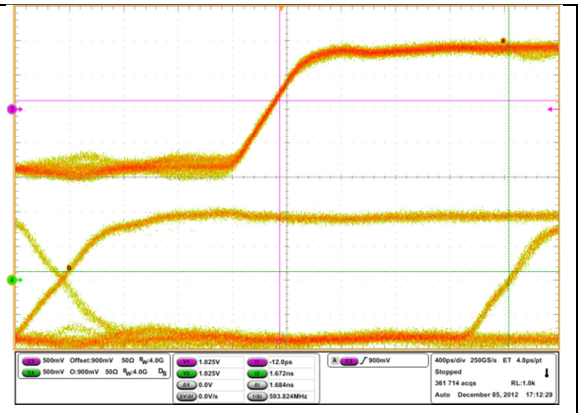


Figure 4.216: DDR_DQ_DQS_WRITE_HOLD_RISING

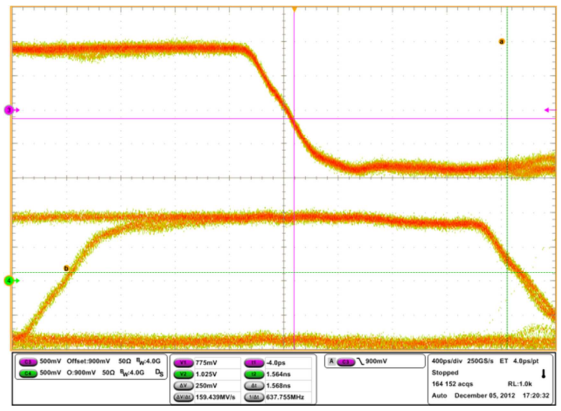


Figure 4.217: DDR_DQ_DQS_WRITE_HOLD__FALLING

Goal: Verify the hold time of DQ to DQS

S3 (Pu, PA2366): DDR_LDQS @ U501(B7)
S4 (Gn, PA827): DDR_DQ0 @ U501(B9)
Scope SN2848

Param	Required	Measured
T_{DHb}	>0.125ns + 291ps (derating)	1.68ns(R) 1.56ns(F)

Conclusion: Hold time is OK

Conclusion: Write timing is OK

4.4.4.2.4.Read timing (DQ to DQS) [PASS]

No read timing specified for DSP (only PCB requirements)

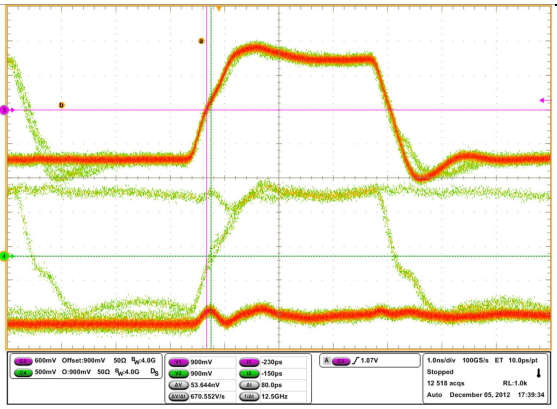


Figure 4.218: DDR_DQ_DQS_READ

Goal: Verify the alignment of DQ to DQS while reading

S3 (Pu, PA2366): DDR_LDQS @ U300(T14)
S4 (Gn, PA827): DDR_DQ0 @ U300(U15)
Scope SN2848

Conclusion: DQ and DQS are edge aligned as expected

Conclusion: No read timing requirements specified, DQ and DQS are edge aligned

4.4.5. Supply noise [Pass]

Goal: Verify noise on supplies of DSP (without DRAM activity)

Initials	JVA		SN	12-30-011-373
Date	01-11-2012		POC FPGA	R04
			POC DSP	R01

Measurement setup:
Master: Setup 1 – no master
EEQDM: Setup 1 – default

Measurement:

- Power EEDQM
- Connect 4 motors to RTME
- Run scrip for all four motors:
  - ./encoder_commutation X 50 0x803 0x803
- Measure the DSP Supplies.

Result:

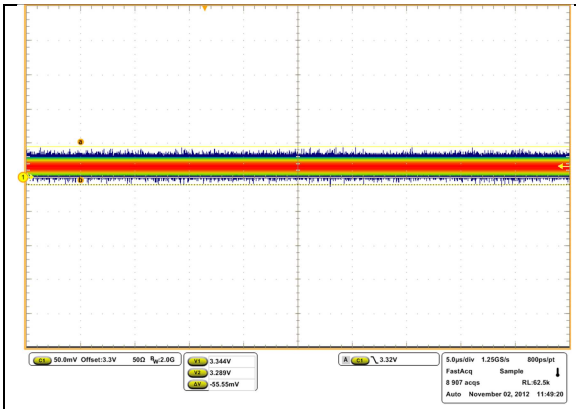


Figure 4-219: +3V3_noise

Goal: Verify noise on DVDD3318 supply of DSP.

S1 (Ye, PA2596): +3V3 @U300(P6)
Scope DPO7254; SN1799

Param	Min	Typ	Max	Measured
V_{CC}	3.15V	3.3V	3.45V	3.289…3.344V
Noise			100mV	55.55mV

Conclusion: Supply noise is OK (same result with DDR memory test)

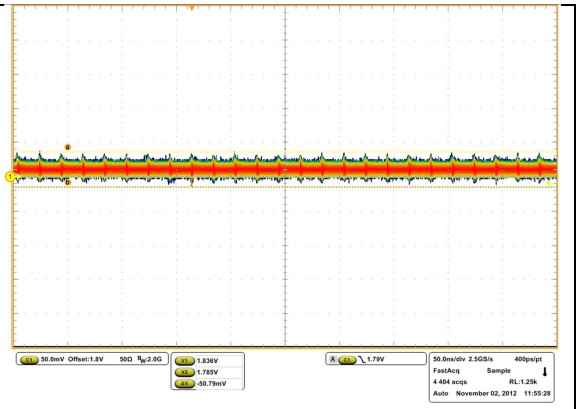


Figure 4-220: +1V8 _noise

Goal: Verify noise on DVDD18 supply of DSP.

S1 (Ye, PA2596): +1V8@U300(K5)
Scope DPO7254; SN1799

Param	Min	Typ	Max	Measured
V_{CC}	1.71V	1.8V	1.89V	1.785…1.836mV
Noise			100mV	50.79mV

Conclusion: Supply noise is OK (same result with DDR memory test)

Figure 4-221: +1V2 _noise

Goal: Verify noise on CVDD supply of DSP.

S1 (Ye, PA2596): +1V2@ U300 (J12)
Scope DPO7254; SN1799

Param	Min	Typ	Max	Measured
V_{CC}	0.9V	1.2V	1.32V	1.174…1.24V
Noise			100mV	66.67mV

Conclusion: Supply noise is OK (same result with DDR memory test)

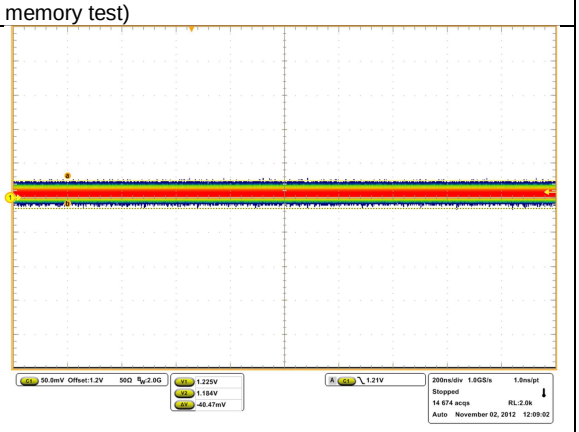


Figure 4-222: +1V2_PLL _noise

Goal: Verify noise on PLL supply of DSP.

S1 (Ye, PA2596): +1V2_DSP+PLL@ U300 (L15/M147)
Scope DPO7254; SN1799

Param	Min	Typ	Max	Measured
V_{CC}	1.14V	1.2V	1.32V	1.184…1.225V
Noise			100mV	40.47mV

Conclusion: Supply noise is OK (same result with DDR memory test)

Goal: Verify noise on supplies of DRAM and DSP

Initials	JVA		Board release:	R01
Date	17-12-2012		SN	12-30-011-410
			POC release	

5

Measurement setup:
Master: Setup 1 – no master
EEQDM: Setup 1 – default

Measurement:

- Power EEDQM
- Create DRAM activity
- Measure the DSP Supplies.

Result:

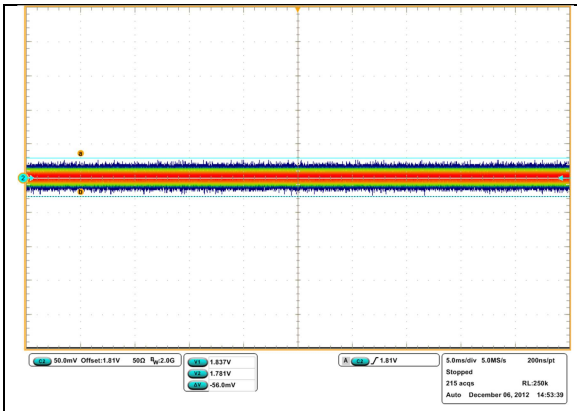


Figure 4-223: +1V8_noise_DDR

Goal: Verify noise on VDD supply of DRAM.

S3 (Pu, PA2366): +1V8 @U501(E1)
Scope SN2848

Param	Min	Typ	Max	Measured
V_{CC}	1.7V	1.8V	1.9	1.781…1.837V
Noise			100mV	56mV

Conclusion: OK

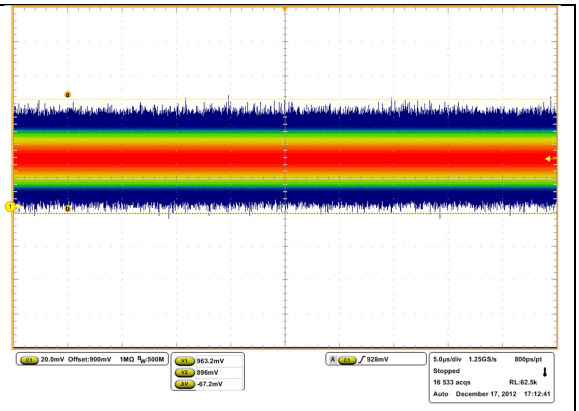


Figure 4-224: +DDR_VREF_noise_DRAM

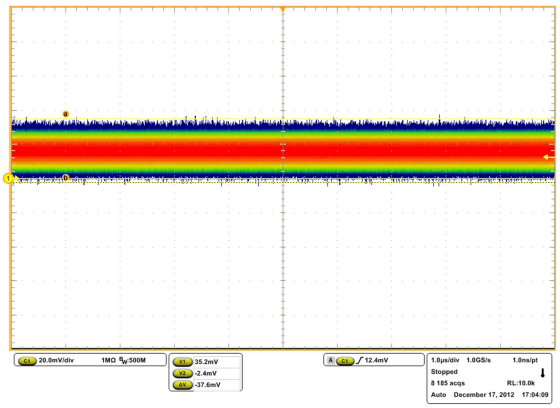


Figure 4-225: +DDR_VREF _Probe_noise

Goal: Verify noise on VREF supply of DRAM.

S1 (Ye, Passive): +1V8@U300(K5)
Scope SN0747

Param	Min	Typ	Max	Measured
V_{CC}	0.882	0.9	0.918	0.869…0.963V
Noise			48mV	67.2mV

Conclusion: ripple is too large. Taken the probe noise of 37mV into account the ripple is OK and Vcc is within range.

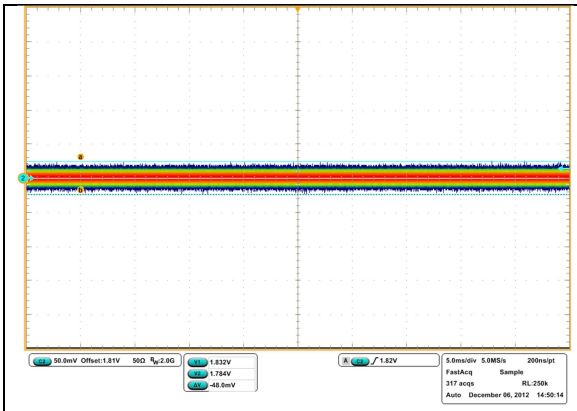


Figure 4-226: +1V8 _noise_DSP

Goal: Verify noise on DDR_DVDD18 supply of DSP.

S3 (Pu, PA2599): +1V8 @U300(K5)
Scope SN0748

Param	Min	Typ	Max	Measured
V_{CC}	1.71V	1.8V	1.89V	1.784…1.832V
Noise			100mV	48mV

Conclusion: OK

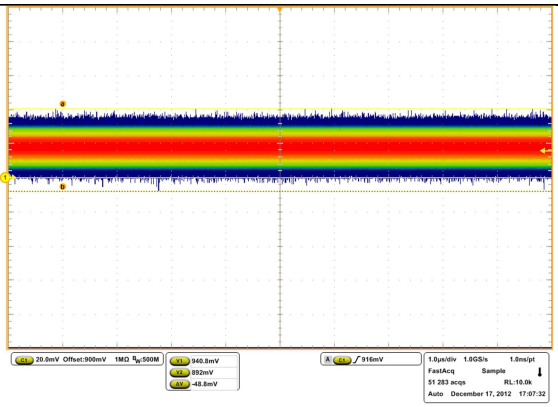


Figure 4-227: +DDR_VREF _noise_DSP

Goal: Verify noise on VREF supply of DSP.

S1 (Ye, Passive): +1V8@U300(R6)
Scope SN747

Param	Min	Typ	Max	Measured
V_{CC}	0.882	0.9	0.918	0.892…0.94V
Noise			48mV	48.8mV

Conclusion: ripple is too large. Taken the probe noise of 37mV into account the ripple is OK and Vcc is within range.

Conclusion: Supply noise is OK

4.5. EtherCAT [Pass]

4.5.1. Clocks [Pass]

Goal:
Qualify the PHY0/1 board clocks.

Initials	JVA		Board release:	R01
Date	24-10-2012		SN	12-28-001-828
			POC release	N/A

Measurement setup:
Master: Setup 1 – no master
EEQDM: Setup 1 – default

Method:

- Follow the measurement preparations as described with the setup.
- Measure at clock target
  - DC levels

Results: