Configuration of the DP130 for eDP Applications

ABSTRACT

Overview

The DP130 can be configured for an eDP (embedded DP) (1, 2, or 4 lane) application with standard DP (not the extended output voltage levels 400, 600, 800 and 1200 mV) and pre-emphasis (0, 3.5, 6, and 9 dB) for up to 5.4Gbps operation. Link training could be disabled for this application and all device configurations would need to be accomplished through I2C control. Through the I2C control, you will be able to configure lane by lane equalization, output Vod, pre-emphasis, as well as number of lanes, data rate.

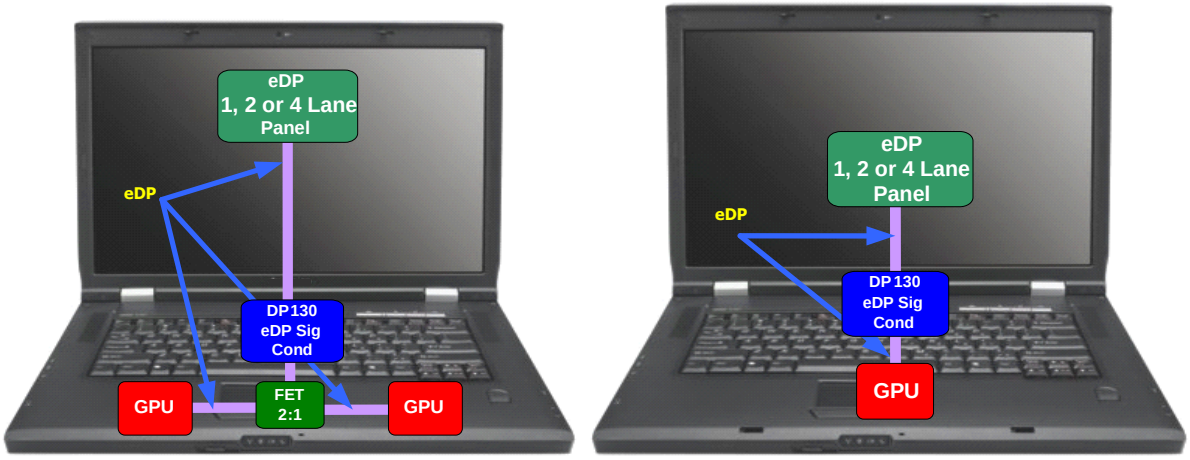

Figure 1. eDP configurations

Version	Date	Author	Notes
1.0	March 2013	Ken Shaw	First release

Figure 2. Document History

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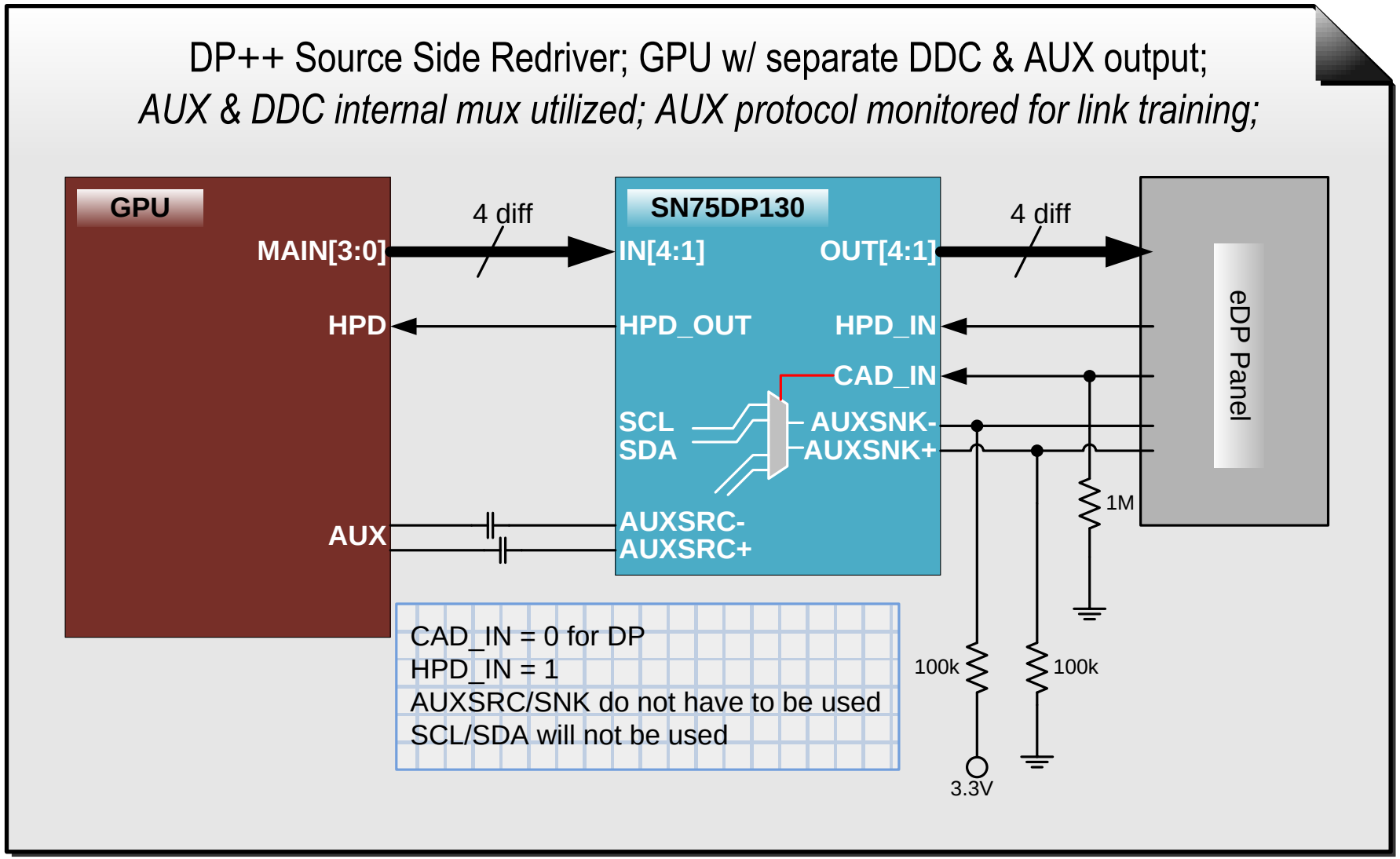


Figure 3. DP130 in an eDP configuration

Configuring the DPCD registers via I²C Overview

The configuration of these registers can be performed through the I²C interface, where three registers are used as address to the device memory (from 1Ch to 1Eh) and another one as a data to be read/written (1Fh); therefore, in order to perform a configuration on the DPCD, first of all is necessary store the address of the DPCD register to be configured and after the data or configuration value, all the above within the proper I²C registers. The following

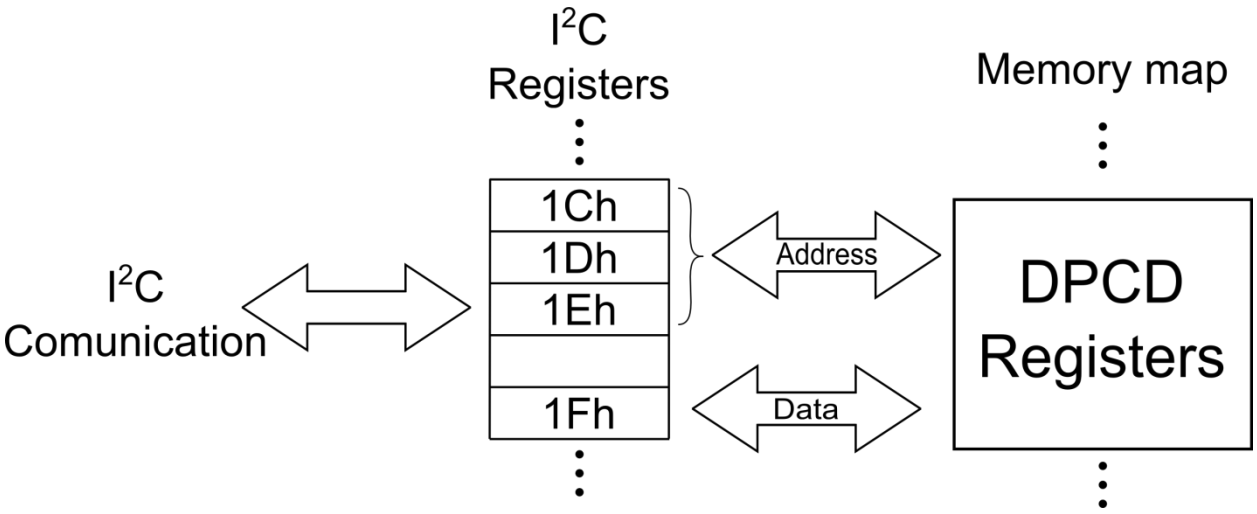


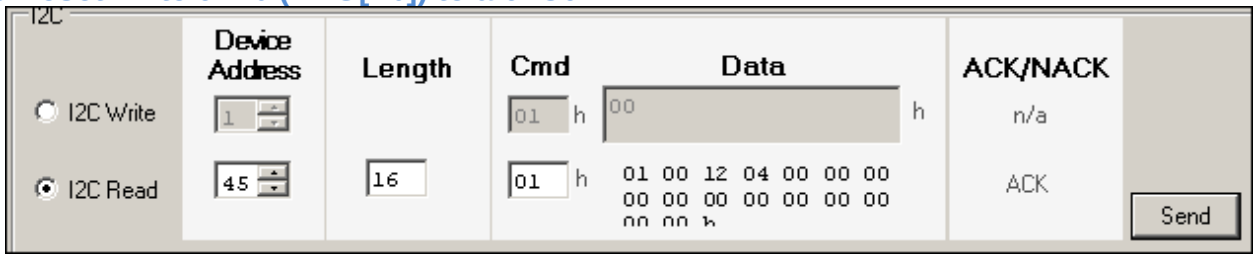
figure is a graphical description of the relationship between the I2C interface and the device memory.

Figure 4. Relationship between the I²C interface and the memory.

I2C Example Setup

The following I2C setup example is for a 4-lane configuration with HBR2 data rate, amplitude for all for lanes of 800 mV and 0 dB pre-emphasis and 8 dB of fixed equalization.

Device Reset write 0x1b (REG[1b]) to a 0xC0h



Default read

Turn off Link Training

Default read for register 0x04 (REG04) is a 0x04 (REG04[2] = 1) with link training enabled. To disable link training write REG04[2] = 0 by writing REG04 to a 0x00.

Table 1. DP130 REG04 Description

04h	3	TI_TEST. This field defaults to zero value, and should not be modified.
	2	LINK_TRAINING_ENABLE 0 – Link Training is disabled. V_{OD} and Pre-emphasis are configured through the I^2C register interface; the EQ is fixed when this bit is zero. 1 – Link Training is enabled (default)
	1:0	AUX_DDC_MUX_CFG. See Table 3 for details on the programming of this field. 00 – AUX_SNK is switched to AUX_SRC for DDC source side based on CAD_SNK (default) 01 – AUX_SNK is switched to AUX_SRC based on the CAD_SNK input, and used to short circuit AC coupling capacitors in the TMDS operating mode. 10 – AUX_SNK is switched to AUX_SRC side based on the HPD_SNK input, while the DDC source interface remains disabled. 11 – Undefined operation

DP130 Output Setup

The DPCD registers configure the device output. There will be no output of the device until these registers have been configured. Normal link training will populate to the link configuration, but when in the eDP application, it is possible that a quick or no link training can be used. Below is a table of the DPCD registers that the DP130 will monitor during link training.

Table 2. DP130 DPCD Registers Monitored

Address	name	Description
00100h	LINK_BW_SET	Bits 7:0 = Link Bandwidth Setting 06h – 1.62Gbps per lane 0Ah – 2.7Gbps per lane (default) 14h – (or any other value) 5.4Gbps per lane
00101h	LANE_COUNT_SET	Bits 4:0 = Lane Count 0h – All lanes disabled (default) 1h – One lane enabled 2h – Two lanes enabled 4h – Four lanes enabled Note: any other value is invalid and disables all Main Link output lanes
00103h	TRAINING_LANE0_SET	Bits 1:0 = Output Voltage VOD Level 00 – Voltage swing level 0 (default) 01 – Voltage swing level 1 10 – Voltage swing level 2 11 – Voltage swing level 3 Bits 4:3 = Pre-emphasis Level 00 – Pre-emphasis level 0 (default) 01 – Pre-emphasis level 1 10 – Pre-emphasis level 2 11 – Pre-emphasis level 3 Note: the following combinations are not allowed for bits [1:0]/[4:3]: 01/11, 10/10, 10/11, 11/01, 11/10, 11/11; setting to any of these invalid combinations disables all Main Link lanes until the register value is changed back to a valid entry
00104h	TRAINING_LANE1_SET	Sets the VOD and pre-emphasis levels for lane 1
00105h	TRAINING_LANE2_SET	Sets the VOD and pre-emphasis levels for lane 2
00106h	TRAINING_LANE3_SET	Sets the VOD and pre-emphasis levels for lane 3
0010F	TRAINING_LANE0_1_SET2	Bits 1:0 = Lane 0 Post Cursor 2 00 – IN0 expects post cursor2 level 0; OUT0 transmits at post cursor 2 level 0 01 – IN0 expects post cursor2 level 1; OUT0 remains at post cursor 2 level 0

		10 – IN0 expects post cursor2 level 2; OUT0 remains at post cursor 2 level 0 11 – IN0 expects post cursor2 level 3; OUT0 remains at post cursor 2 level 0 Bits 5:4 = Lane 1 Post Cursor 2 00 – IN1 expects post cursor2 level 0; OUT1 transmits at post cursor 2 level 0 01 – IN1 expects post cursor2 level 1; OUT1 remains at post cursor 2 level 0 10 – IN1 expects post cursor2 level 2; OUT1 remains at post cursor 2 level 0 11 – IN1 expects post cursor2 level 3; OUT1 remains at post cursor 2 level 0
0110F	TRAINING_LANE2_3_SET2	Bit definition identical to that of TRAINING_LANE_0_1_SET2 but for lanes 2 (IN2/OUT2) and lane 3 (IN3/OUT3)
00600h	SET_POWER	Bits 1:0 = Power Mode 01 – Normal mode (default) 10 – Power down mode; D3 Standby Mode The Main Link and all analog circuits are shut down and the AUX channel is monitored during the D3 Standby Mode. The device exits D3 Standby Mode by access to this register, when CAD_SNK goes high, or if HPD_SNK goes low for longer than $t_{T(HPD)}$, which indicates that the DP sink was disconnected. Note: setting the register to the invalid combination 0600h[1:0]=00 or 11 is ignored by the device and the device remains in normal mode

If link training is not used, the transactions below can be used to setup the DP130 for the following configuration:

DP130 HBR2, 4-lane, 800 mV at 0dB pre-emphasis

To write to the DPCD information, the DP130 as set up 4 8-bit registers that will be used to write the DPCD register and value. Below is a description of these registers

Table 3. DP130 REG1C –REG1F Description

1Ch	3:0	DPCD_ADDR_HIGH. This value maps to bits 19:16 of the 20-bit DPCD register address accessed through the DPCD_DATA register
1D	7:0	DPCD_ADDR_MID. This value maps to bits 15:8 of the 20-bit DPCD register address accessed through the DPCD_DATA register.
1E	7:0	DPCD_ADDR_LOW. This value maps to bits 7:0 of the 20-bit DPCD register address accessed through the DPCD_DATA register.
1F	7:0	DPCD_DATA. This register contains the data to write into or read from the DPCD register addressed by DPCD_ADDR_HIGH, DPCD_ADDR_MID, and DPCD_ADDR_LOW.

Write the link Data Rate

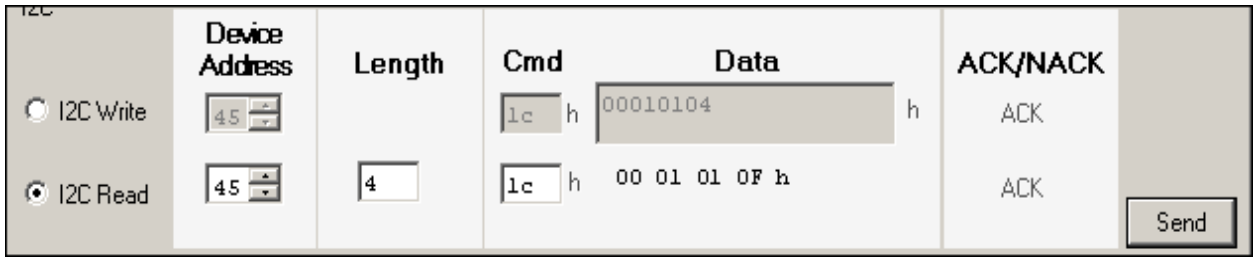
To write the link LINK_BW_SET, DPCD register 0x00100h, use the following instructions

1. Setup the link data rate for HBR2 a value of 0x14h
    a. Write REG1c to 0x00
    b. Write REG1d to 0x01
    c. Write REG1e to 0x00
    d. Write REG1f to 0x14 – this will write a 0x14 to the DPCD register 0x00100

Write the number of lanes to be enabled

To write the LANE_COUNT_SET, DPCD register 0x00101h, use the following instructions

2. Set up the number of lanes for 4 lanes, write a value of 0x04
    a. Write REG1c to0x 00
    b. Write REG1d to 0x01
    c. Write REG1e to 0x01
    d. Write REG1f to 0x04 – this will write a 0x04 to the DPCD register 0x00101



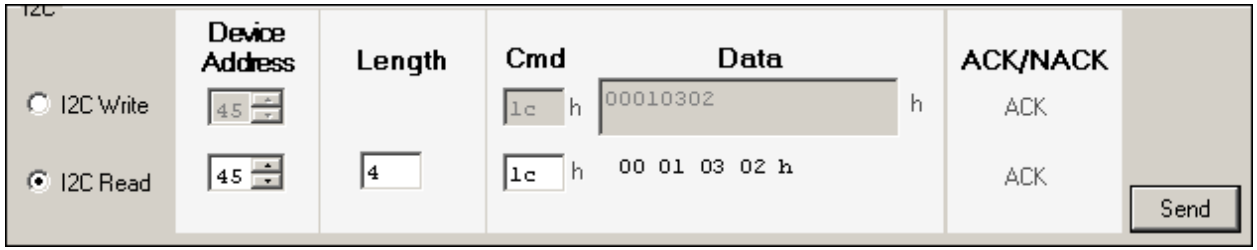
Note that a 0x04 was written, but a 0x0F was read. This is correct. Please refer to the mapping at the end of this document

Configure the output Voltage (V_{OD}) and Pre-emphasis

To write the TRAINING_LANE0_SET, DPCD register 0x00103h, use the following instructions

3. Set up Lane 0 with 800 mV and 0 dB pre-emphasis, write a value 0x02 (DPCD_REG00103[1:0] = 10 for Voltage swing level 2 and DPCD_REG00103[4:3] = 00 for Pre-emphasis level 0)
    a. Write REG1c to 0x00
    b. Write REG1d to 0x01
    c. Write REG1e to 0x03
    d. Write REG1F to 0x02 – this will write a 0x02 to the DPCD register 0x00103

    Below is a screenshot of the I2C write and read for DPCD register 0x000103 being set to a 0x02



4. Set up Lane 1 with 800 mV and 0 dB pre-emphasis, write a value 0x02 (DPCD_REG00104[1:0] = 10 for Voltage swing level 2 and DPCD_REG00104[4:3] = 00 for Pre-emphasis level 0)
    a. Write REG1c to 0x00
    b. Write REG1d to 0x01
    c. Write REG1e to 0x04
    d. Write REG1F to 0x02 – this will write a 0x02 to the DPCD register 0x00104
5. Set up Lane 2 with 800 mV and 0 dB pre-emphasis, write a value 0x02 (DPCD_REG00105[1:0] = 10 for Voltage swing level 2 and DPCD_REG00105[4:3] = 00 for Pre-emphasis level 0)

a. Write REG1c to 0x00

b. Write REG1d to 0x01

c. Write REG1e to 0x05

d. Write REG1F to 0x02 – this will write a 0x02 to the DPCD register 0x00105

6. Set up Lane 3 with 800 mV and 0 dB pre-emphasis, write a value 0x02 (DPCD_REG00106[1:0] = 10 for Voltage swing level 2 and DPCD_REG00106[4:3] = 00 for Pre-emphasis level 0)

    a. Write REG1c to 0x00

    b. Write REG1d to 0x01

    c. Write REG1e to 0x06

    d. Write REG1F to 0x02 – this will write a 0x02 to the DPCD register 0x00106

Setup EQ through I2C

Setup Lane 0 EQ and turn on I2C control of the EQ

1. Setup device for I2C control of the EQ and configure Lane 0 for 8 dB of Fixed EQ (link training is disabled)

    a. Write REG05[7] to a 1 to control EQ from I2C
    and configure Lane 0 EQ for 8 dB of fixed EQ at HBR2 REG05[2:0] =011 respectively

    b. Write REG05 to a 0x83 (1000 0011b)

Table 4. DP130 REG05 Description

05h	7	EQ_I2C_ENABLE 0 – EQ settings controlled by device inputs only (default) 1 – EQ settings controlled by I^2C register settings
	6:4	AEQ_L0_LANE0_SET. This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0dB EQ gain (default) 100 – 5dB (HBR); 10dB (HBR2) 001 – 1.5dB (HBR); 3.5dB (HBR2) 101 – 6dB (HBR); 13dB (HBR2) 010 – 3dB (HBR); 6dB (HBR2) 110 – 7dB (HBR); 15dB (HBR2) 011 – 4dB (HBR); 8dB (HBR2) 111 – 9dB (HBR); 18dB (HBR2)
	2:0	AEQ_L1_LANE0_SET. This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE RW is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results for Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ modes: • I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled • I2C_EQ_ENABLE is set and the TMDS sink is selected. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2

Setup Lane 1 EQ setting

1. Setup device configuration for Lane 1 with 8 dB of Fixed EQ (link training is disabled)

a. Write REG07[2:0] =011

b. Write REG07 to 0x03 (0000 0011b)

Table 5. DP130 REG07 Description

07	6:4	AEQ_L0_LANE1_SET. This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0dB EQ gain (default) 001 – 1.5dB (HBR); 3.5dB (HBR2) 010 – 3dB (HBR); 6dB (HBR2) 011 – 4dB (HBR); 8dB (HBR2) 100 – 5dB (HBR); 10dB (HBR2) 101 – 6dB (HBR); 13dB (HBR2) 110 – 7dB (HBR); 15dB (HBR2) 111 – 9dB (HBR); 18dB (HBR2)
	2:0	AEQ_L1_LANE1_SET. This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE RW is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results for Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non- AEQ modes: • I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled • I2C_EQ_ENABLE is set and the TMDS sink is selected. 000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2

Setup Lane 2 EQ setting

1. Setup device configuration for Lane 2 with 8 dB of Fixed EQ (link training is disabled)

   a. Write REG09[2:0] =011

   b. Write REG09 to 0x03 (0000 0011b)

Table 6. DP130 REG09 Description

09	6:4	AEQ_L0_LANE2_SET. This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis.

		000 – 0dB EQ gain (default)	100 – 5dB (HBR); 10dB (HBR2)
		001 – 1.5dB (HBR); 3.5dB (HBR2)	101 – 6dB (HBR); 13dB (HBR2)
		010 – 3dB (HBR); 6dB (HBR2)	110 – 7dB (HBR); 15dB (HBR2)
		011 – 4dB (HBR); 8dB (HBR2)	111 – 9dB (HBR); 18dB (HBR2)
	2:0	AEQ_L1_LANE2_SET. This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE RW is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results for Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ modes: • I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled • I2C_EQ_ENABLE is set and the TMDS sink is selected.	
		000 – 0 dB EQ gain (default)	100 – 5 dB (HBR); 10 dB (HBR2)
		001 – 1.5 dB (HBR); 3.5 dB (HBR2)	101 – 6 dB (HBR); 13 dB (HBR2)
		010 – 3 dB (HBR); 6 dB (HBR2)	110 – 7 dB (HBR); 15 dB (HBR2)
		011 – 4 dB (HBR); 8 dB (HBR2)	111 – 9 dB (HBR); 18 dB (HBR2

Setup Lane 3 EQ setting

1. Setup device configuration for Lane 3 with 8 dB of Fixed EQ (link training is disabled)

   a. Write REG0B[2:0] =011

   b. Write REG0B to 0x03 (0000 0011b)

Table 7. DP130 REG0B Description

0B	6:4	AEQ_L0_LANE3_SET. This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis.	
		000 – 0dB EQ gain (default)	100 – 5dB (HBR); 10dB (HBR2)
		001 – 1.5dB (HBR); 3.5dB (HBR2)	101 – 6dB (HBR); 13dB (HBR2)
		010 – 3dB (HBR); 6dB (HBR2)	110 – 7dB (HBR); 15dB (HBR2)
		011 – 4dB (HBR); 8dB (HBR2)	111 – 9dB (HBR); 18dB (HBR2)

	2:0	AEQ_L1_LANE3_SET. This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE RW is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results for Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ modes: • I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled • I2C_EQ_ENABLE is set and the TMDS sink is selected.
		000 – 0 dB EQ gain (default) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2

Appendix A. Reference Information

References

Table A-1. DP130 DPCD Register Read and Write Information

Write 1D to 01
Write 1E to 03
then
Read 1F for the DPCD info

decim	Register	Write 1C	Write 1D	Write 1E	Register Description	**WRITE** DPCD 7	5	4	3	2	1	0	1F	**READ** DP126 7	5	4	3	2	1	0	1F	Write Notes	Read Notes	
256	000100	00	01	00	LINK_BW_SET	0	0	0	0	1	1	0	**06**	0	0	0	0	0	0	0	**00**	06h – 1.62Gbps per lane	00h – 1.62Gbps per lane	
						0	0	0	1	0	1	0	**0A**	0	0	0	0	0	0	1	**01**	0Ah – 2.7Gbps per lane (default)	01h – 2.7Gbps per lane (default)	
						0	0	1	0	1	0	0	**14**	0	0	0	0	0	1	0	**02**	14h – 5.4Gbps per lane	02h – 2.7Gbps per lane	
257	000101	00	01	01	LANE_COUNT_SET	0	0	0	0	0	0	0	**00**	0	0	0	0	0	0	0	**00**	0h – All lanes disabled (default)	0h – All lanes disabled (default)	
						0	0	0	0	0	0	1	**01**	0	0	0	0	0	0	1	**01**	1h – One lane enabled	1h – One lane enabled	
						0	0	0	0	0	1	0	**02**	0	0	0	0	0	1	1	**03**	2h – Two lanes enabled	3h – Two lanes enabled	
						0	0	0	0	1	0	0	**04**	0	0	0	1	1	1	1	**0F**	4h – Four lanes enabled	Fh – Four lanes enabled	
259	000103	00	01	03	TRAINING_LANE0_SET																			Write Bits 4:3 = Pre-emphasis Level Read Bits 3:2 = Pre-emphasis Level
						0	0	0	0	0	0	0	**00**	0	0	0	0	0	0	0	**00**	Vod L0 Pre 0		00 – Pre-emphasis level 0 (default)
						0	0	0	1	0	0	0	**08**	0	0	0	0	1	0	0	**04**	Vod L0 Pre 1	Write & Read Bits	01 – Pre-emphasis level 1
						0	0	1	0	0	0	0	**10**	0	0	0	1	0	0	0	**08**	Vod L0 Pre 2	1:0 = Output Voltage VOD Level	10 – Pre-emphasis level 2
						0	0	1	1	0	0	0	**18**	0	0	0	1	1	0	0	**0C**	Vod L0 Pre 3	00 – Voltage swing level 0 (default)	11 – Pre-emphasis level 3
						0	0	0	0	0	0	1	**01**	0	0	0	0	0	0	1	**01**	Vod L1 Pre 0		00 – Pre-emphasis level 0 (default)
						0	0	0	1	0	0	1	**09**	0	0	0	0	1	0	1	**05**	Vod L1 Pre 1		01 – Pre-emphasis level 1
						0	0	1	0	0	0	1	**11**	0	0	0	1	0	0	1	**09**	Vod L1 Pre 2	01 – Voltage swing level 1	10 – Pre-emphasis level 2
						0	0	0	0	0	1	0	**02**	0	0	0	0	0	1	0	**02**	Vod L2 Pre 0		00 – Pre-emphasis level 0 (default)
						0	0	0	1	0	1	0	**0A**	0	0	0	0	1	1	0	**06**	Vod L2 Pre 1	10 – Voltage swing level 2	01 – Pre-emphasis level 1
						0	0	0	0	0	1	1	**03**	0	0	0	0	0	1	1	**03**	Vod L3 Pre 0	11 – Voltage swing level 3	00 – Pre-emphasis level 0 (default)
260	000104	00	01	04	TRAINING_LANE1_SET	Same as 000103 above for 104, 105, & 106 for lanes 1, 2, and 3																		
261	000105	00	01	05	TRAINING_LANE2_SET																			
262	000106	00	01	06	TRAINING_LANE3_SET																			
271	00010F	00	01	0F	TRAINING_LANE0_1_SET2	0	0	0	0	0	0	0	00	0	0	0	0	0	0	0	00	00 – IN0 expects post cursor2 level 0; OUT0 transmits at post cursor 2 level 0	Write and Read are the Same	
4367	00110F	00	11	0F	TRAINING_LANE2_3_SET2	0	0	0	0	0	0	1	01	0	0	0	0	0	0	1	01	01 – IN0 expects post cursor2 level 1; OUT0 transmits at post cursor 2 level 0	Write and Read are the Same	
																						10 – IN0 expects post cursor2 level 2; OUT0 transmits at post cursor 2 level 0	Write and Read are the Same	
																						11 – IN0 expects post cursor2 level 3; OUT0 transmits at post cursor 2 level 0	Write and Read are the Same	
																						Bits 5:4 = Lane 1 Post Cursor 2		
																						00 – IN1 expects post cursor2 level 0; OUT1 transmits at post cursor 2 level 0	Write and Read are the Same	
																						01 – IN1 expects post cursor2 level 1; OUT1 transmits at post cursor 2 level 0	Write and Read are the Same	
																						10 – IN1 expects post cursor2 level 2; OUT1 transmits at post cursor 2 level 0	Write and Read are the Same	
																						11 – IN1 expects post cursor2 level 3; OUT1 transmits at post cursor 2 level 0	Write and Read are the Same	

Table A-2. eDP Reference Schematic

The following pages are the schematic pages from the eDP reference schematic

REVISIONS		
ECR	ECR NUMBER -------	DATE --/--/--

THIS SCHEMATIC IS DESIGNED TO BE USED AS A REFERENCE FOR THE DP130SS IN AN eDP APPLICATION

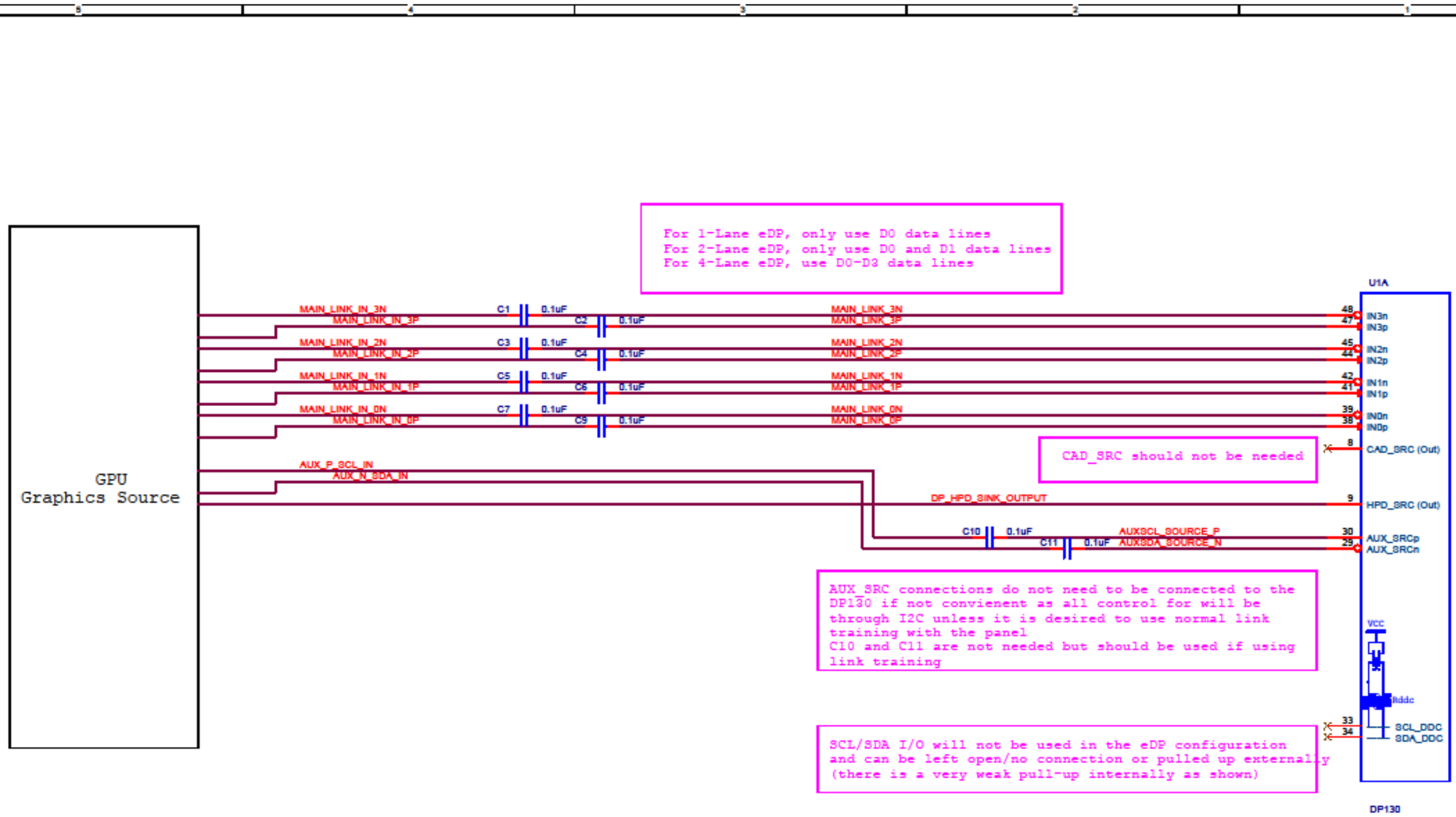
ENGINEER	DATE
K SHAW	11/30/12
LAYOUT	DATE
RELEASED	DATE

TEXAS INSTRUMENTS

SCHEMATIC TITLE: DP130 eDP REFERENCE SCHEMATIC

PAGE TITLE:

SIZE	DOCUMENT NUMBER	REV	SHEET
B	xxxxx	0	1 of 5



TEXAS INSTRUMENTS

PAGE TITLE			
DP130 eDP SOURCE CONNECTION			
SIZE	DOCUMENT NUMBER	REV	PAGE
B	XXXXXXX	0	2 of 5

For 1-Lane eDP, only use D0 data lines
For 2-Lane eDP, only use D0 and D1 data lines
For 4-Lane eDP, use D0-D3 data lines

U1B

OUT0p 23 DP0_P — C12 0.1uF — C13 0.1uF — DP_OUTPUT_0_P
OUT0n 22 DP0_N — DP_OUTPUT_0_N
OUT1p 20 DP1_P — C14 0.1uF — C15 0.1uF — DP_OUTPUT_1_P
OUT1n 19 DP1_N — DP_OUTPUT_1_N
OUT2p 17 DP2_P — C16 0.1uF — C17 0.1uF — DP_OUTPUT_2_P
OUT2n 16 DP2_N — DP_OUTPUT_2_N
OUT3p 14 DP3_P — C18 0.1uF — C19 0.1uF — DP_OUTPUT_3_P
OUT3n 13 DP3_N — DP_OUTPUT_3_N

CAD_SINK (In) 10 CAD — R13 1M

CAD_SINK should be pulled low for DP operation

3P3V — R14 100K

AUX_SNKp 28 AUX_SINK_P — AUX_SINK_OUTPUT_P
AUX_SNKn 27 AUX_SINK_N — AUX_SINK_OUTPUT_N

AUX_SNK connections do not need to be connected to the DP130 if not convienent as all control will be through I2C unless it is desired to use normal link training with the panel
R14 and R17 are not needed but should be used if using link training

R17 100K

3P3V — R19 100K

HPD_SINK (IN) 11 HPD — HPD_SINK

HPD_SNK should be pulled up always for the eDP configuration unless system application needs to control for power options

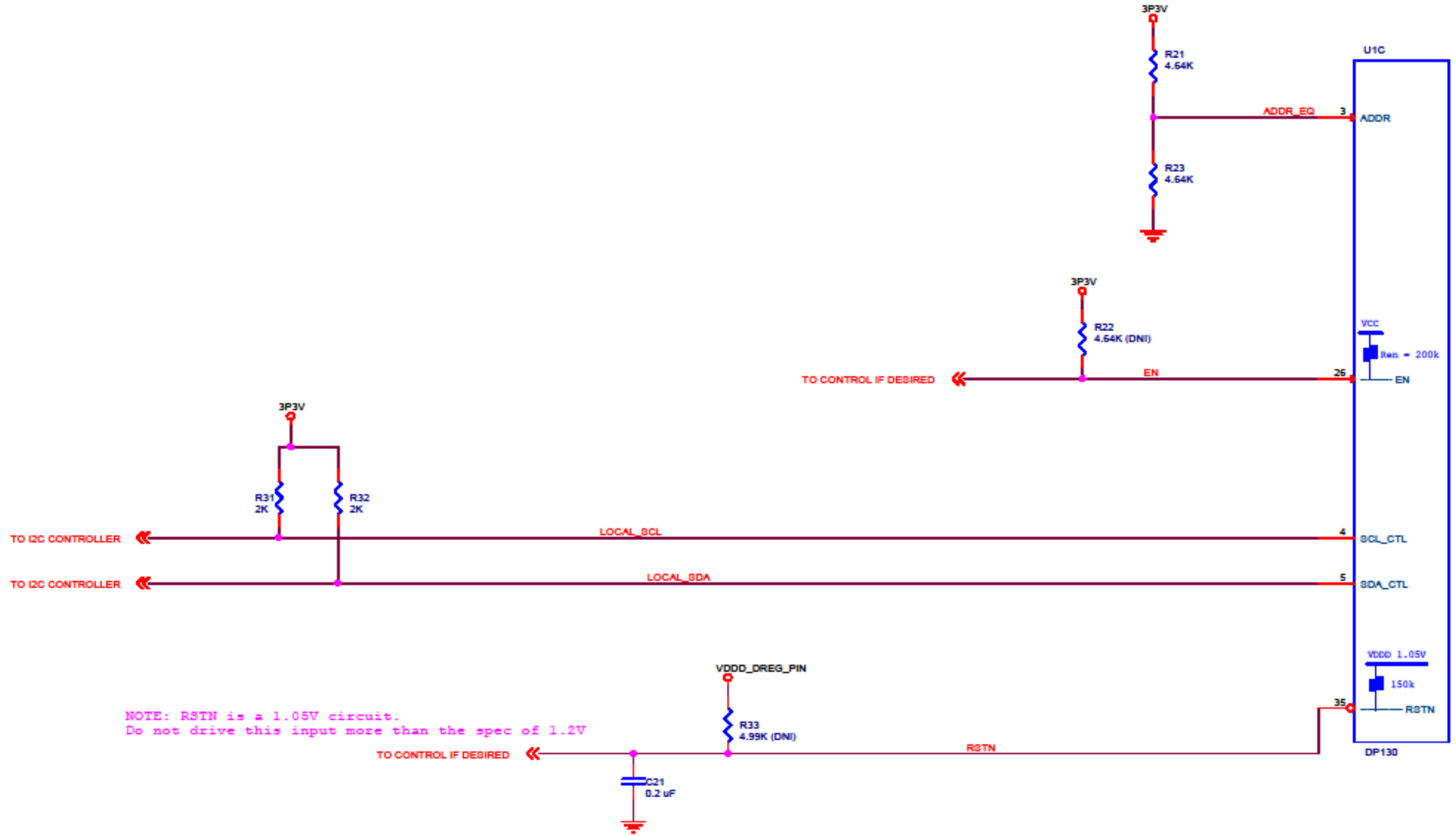
C22 0.2 uF

DP130

DP Panel

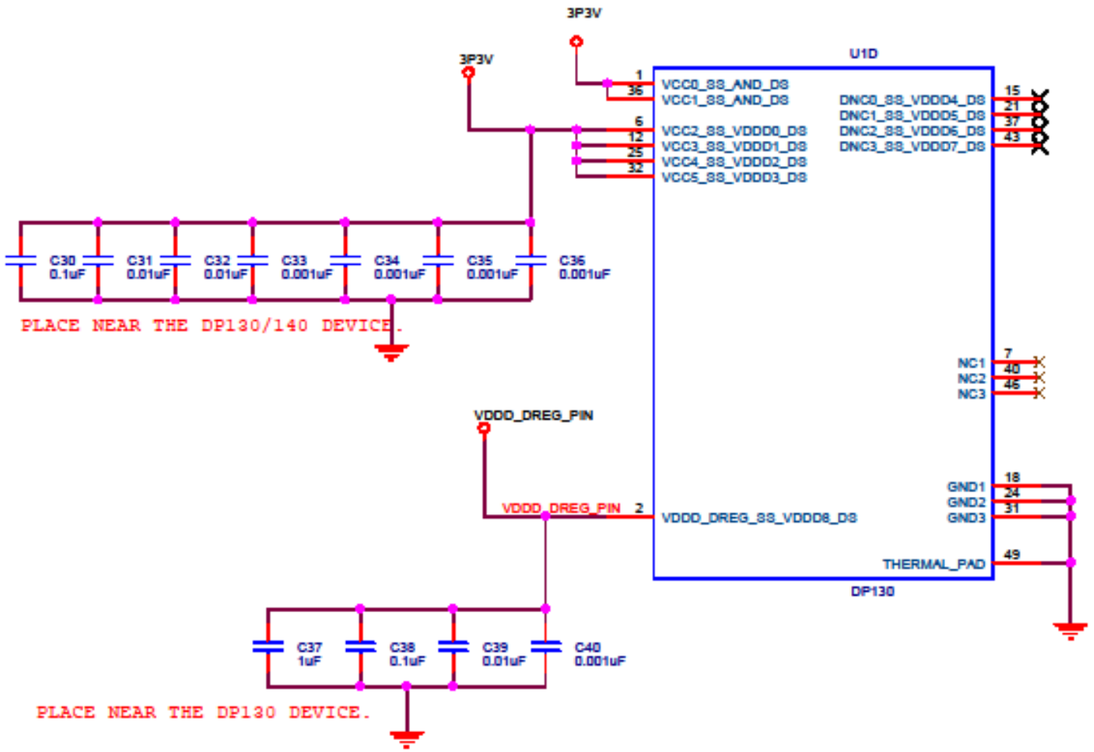
TEXAS INSTRUMENTS

PAGE TITLE			
DP130 eDP PANEL CONNECTION			
SIZE	DOCUMENT NUMBER	REV	PAGE
B	XXXXXX	0	3 of 5



TEXAS INSTRUMENTS

PAGE TITLE			
DP140 CONTROL			
SIZE	DOCUMENT NUMBER	REV	PAGE
B	XXXXX	0	4 of 5



TEXAS INSTRUMENTS

PAGE TITLE			
DP130 POWER			
SIZE	DOCUMENT NUMBER	REV	PAGE
B	XXXXXX	0	5 of 5