Table 7–1. Serial EEPROM Map

BYTE ADDRESS	BYTE DESCRIPTION							
00	PCI maximum latency (PCI offset 3Eh)					PCI minimum grant (PCI offset 3Fh)		
01	PCI subsystem vendor ID alias (lsbyte) (PCI offset F8h)							
02	PCI subsystem vendor ID alias (msbyte) (PCI offset F9h)							
03	PCI subsystem ID alias (lsbyte) (PCI offset FAh)							
04	PCI subsystem ID alias (msbyte) (PCI offset FBh)							
05	[7] Link_enhancement Control.enab_unfair (PCI offset F4h, bit 7)	[6] HCControl. ProgramPhy Enable (OHCI offset 50h, bit 23)	[5–3] RSVD			[2] Link_enhancement Control.enab_ insert_idle (PCI offset F4h, bit 2)	[1] Link_enhancement Control.enab_accel (PCI offset F4h, bit 1)	[0] RSVD
06	[7–6] RSVD		[5] † MiniRom enable (OHCI offset 04h, bit 5)			[4–0] RSVD		
07	1394 GUID high (lsbyte 0) (OHCI offset 24h)							
08	1394 GUID high (byte 1) (OHCI offset 25h)							
09	1394 GUID high (byte 2) (OHCI offset 26h)							
0A	1394 GUID high (msbyte 3) (OHCI offset 27h)							
0B	1394 GUID low (lsbyte 0) (OHCI offset 28h)							
0C	1394 GUID low (byte 1) (OHCI offset 29h)							
0D	1394 GUID low (byte 2) (OHCI offset 30h)							
0E	1394 GUID low (msbyte 3) (OHCI offset 31h)							
0F	Checksum							
10	[15] Link Enhancement.dis_ at_pipeline (PCI offset F4h, bit 15)	[14] Enab_draft (PCI offset F4h, bit 14)	[13–12] Link Enhancement.atx_ thresh (PCI offset F4h, bits 13–12)		[11–8] RSVD			
11	[7] RSVD	[6] MiscConfig. cardbus (PCI offset F0h, bit 6)	[5] RSVD	[4] MiscConfi g.dis_tgt_ abt (PCI offset F0h, bit 4	[3] RSVD	[2] MiscConfig.disable _sclkgate (PCI offset F0h, bit 2)	[1] MiscConfig.disable _pcigate (PCI offset F0h, bit 1)	[0] MiscConfi g.keep_pcl k (PCI offset F0h, bit 0)
12	[15] MiscConfig.PME_D 3cold (PCI offset F0h, bit 15)	[14–11] RSVD				[10] ignore_IntEvent. MasterIntEnable_ for_pme (PCI offset F0h, bit 10)	[9–8] MR_Enhance (PCI offset F0h, bits 9–8)	
13	[7–4] BusOptions.Max_Rec (OHCI offset 20h, bits 15–12)				[3–0] RSVD			
14	[7–3] CIS offset (PCI offset 28h, bits 7–3)					[2–0] RSVD		
15–16	[7–0] RSVD							
17	[7–3] RSVD					[2–0] MultifunctionSelect.MFunc_Sel (PCI offset E8h, bits 2–0)		
18–1F	RSVD							

† If bit 5 at EEPROM byte offset 06h is set, the mini-ROM is enabled and the starting address is 20h.