SN65LVPE502A/ SN65LVPE502B Application Note

Abstract

The SN65LVPE502A redriver and SN65LVPE502B redriver are dual channel, single lane USB 3.0 redrivers and signal conditioners supporting data rates of 5.0Gbps. All errata for the previous part, SN65LVPE502CP, are fixed in these devices. This application note provides information on implementation of the SN65LVPE502A/SN65LVPE502B devices based on changes from the SN65LVPE502CP device.

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Introduction

The errata observed on the SN65LVPE502CP device are fixed on the SN65LVPE502A and SN65LVPE502B devices. In addition to the errata fixes, connections are now defined as host side and device side. Connections between the host, redriver, and connector should be verified. The SN65LVPE502A or the SN65LVPE502B should be chosen based on the layout of the board. The errata fixes include the false detect with VBUS powered devices and termination remaining enabled in certain situations.

Terminal Definition Changes

The host side and device side connections are now defined for the SN65LVPE502A and SN65LVPE502B devices. Please reference Table 1 SN65LVPE502A Pin Functions, for a list of pin definition changes.

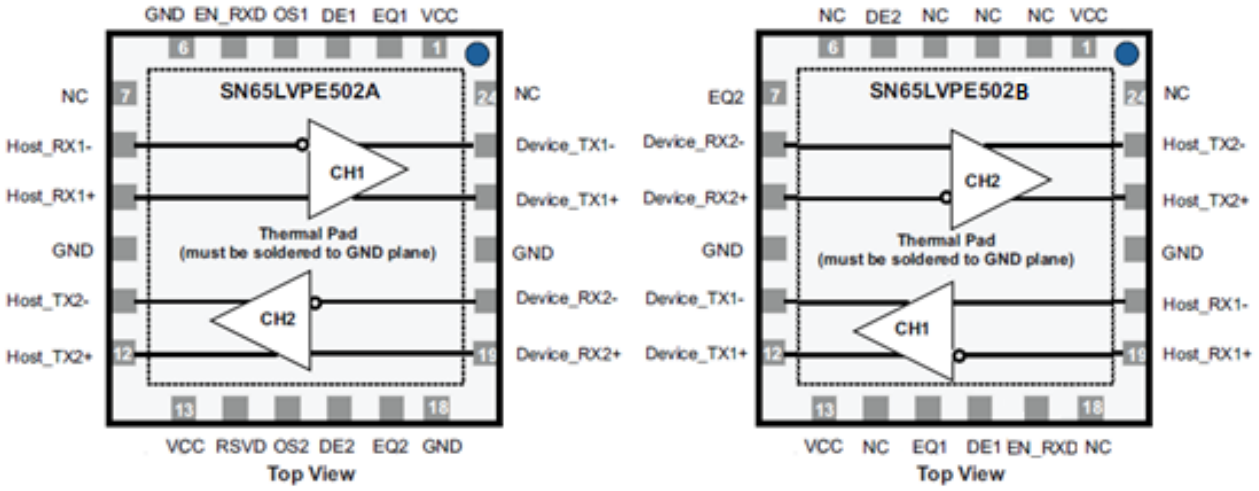

Figure 1 SN65LVPE502A/ SN65LVPE502B Pin-Out

Table 1 SN65LVPE502A / SN65LVPE502B Pin Functions

Pin			I/O Type	Description
SN65LVPE502A Number	**SN65LVPE502B Number**	**Name**		
HIGH SPEED DIFFERENTIAL I/O PINS				
8	18	Host_RX1-	I, CML	Non-inverting and inverting CML differential input for CH 1 and CH 2. These pins are tied to an internal voltage bias by dual
9	19	Host_RX1+	I, CML	

20	8	Device_RX2-	I, CML	termination resistor circuit. All pins labeled Host should be connected to the host. Pins labeled Device should be connected to the device or connector.
19	9	Device_RX2+	I, CML	
23	11	Device_TX1-	O, CML	Non-inverting and inverting CML differential output for CH 1 and CH 2. These pins are tied to an internal voltage bias by termination resistors. All pins labeled Host should be connected to the host. Pins labeled Device should be connected to the device or connector.
22	12	Device_TX1+	O, CML	
11	23	Host_TX2-	O, CML	
12	22	Host_TX2+	O, CML	
DEVICE CONTROL PIN				
5	17	EN_RXD	I, LVCMOS	Sets device operation modes. Internally pulled to VCC
14	-	RSVD	I, LVCMOS	RSVD, internally pulled to GND. Can be left as No-connect.
7, 24	2, 3, 4, 14, 24	NC	No-connect	Pads are not internally connected
EQ CONTROL PINS				
3, 16	16, 5	DE1, DE2	I, LVCMOS	Selects de-emphasis settings for CH 1 and CH 2. Internally tied to Vcc/2
2, 17	15, 7	EQ1, EQ2	I, LVCMOS	Selects equalization settings for CH 1 and CH 2. Internally tied to Vcc/2
4, 15	-	OS1, OS2	I, LVCMOS	Selects output amplitude for CH 1 and CH 2. Internally tied to Vcc/2
POWER PINS				
1, 13	1, 13	VCC	Power	Positive supply should be 3.3V ± 10%
6, 10, 18, 21	10, 21	GND	Power	Supply ground

Preliminary

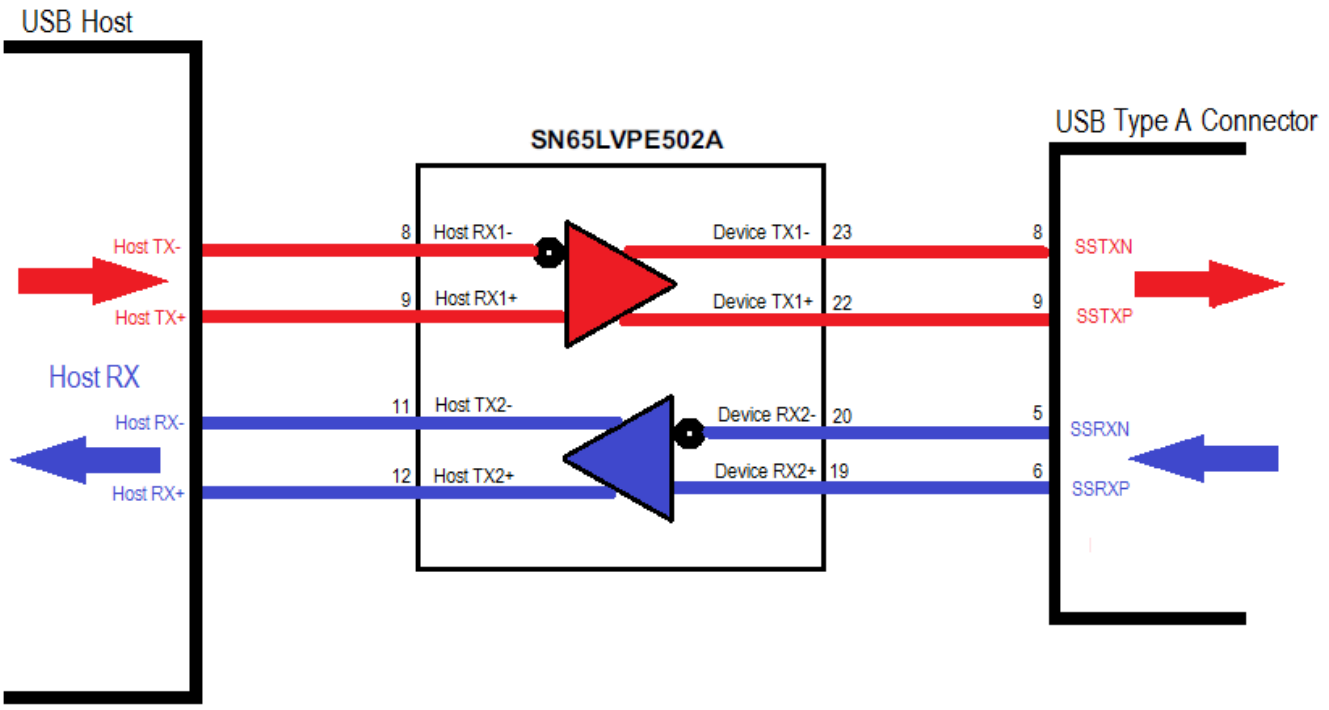

Figure 2 System Connection SN65LVPE502A

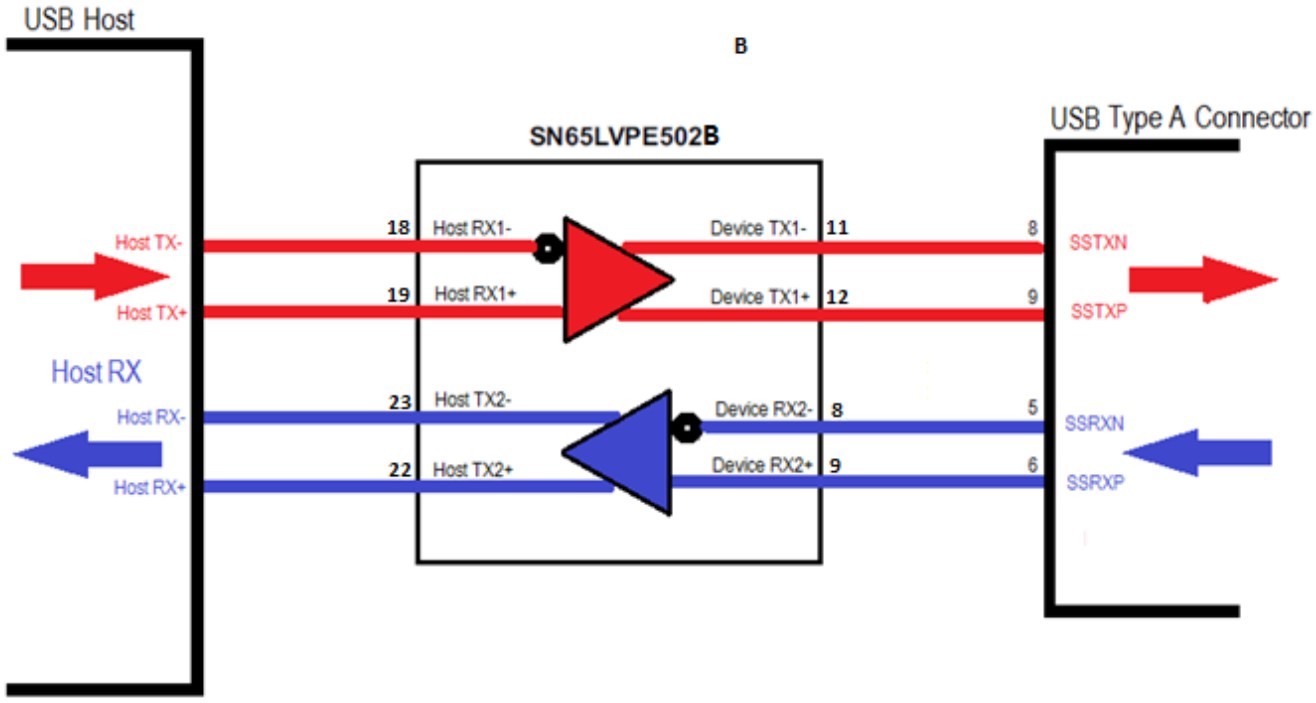

Figure 3 System Connection SN65LVPE502B

Errata Fixes

False Detect

Some VBUS powered devices create noise on plug-in and cause the SN65LVPE502CP to falsely detect the device and enable termination early. After termination is enabled, the host begins polling before the device is ready. Polling will timeout and the host will enter compliance mode. This issue is fixed on the SN65LVPE502A device. Figure 2 Connection of VBUS Powered Device below shows a successful connection after a glitch is observed when the VBUS powered device is attached.

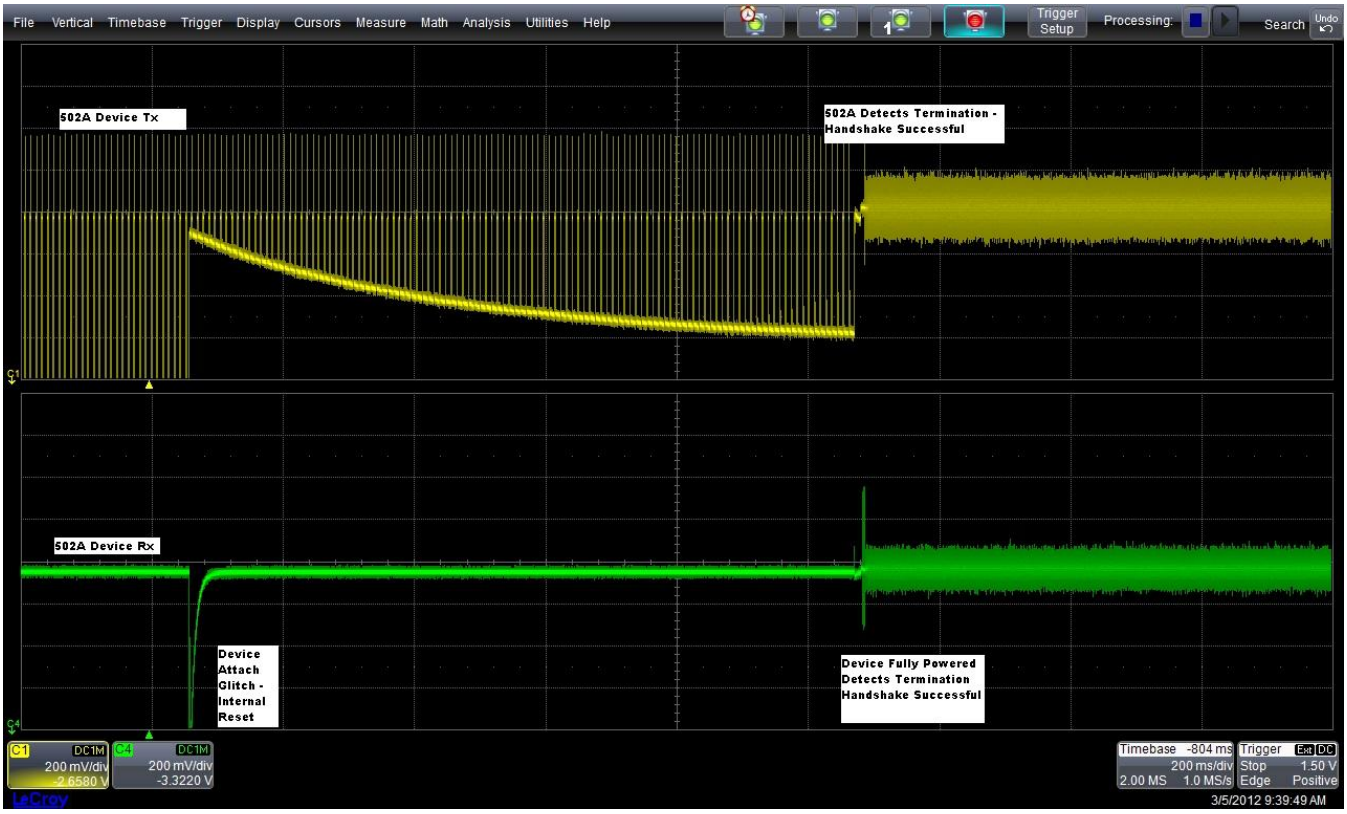

Figure 4 Connection of VBUS Powered Device

Termination Remains Enabled

In certain conditions the termination remains enabled after a device is disconnected from the SN65LVPE502CP. This issue is host software driver dependant. If host issues a warm reset within ~300ms of device disconnect the termination will remain enabled. No functional issues are observed, but the power consumption is increased while no devices are connected. This issue is no longer driver dependant and is fixed in the SN65LVPE502A. A successful disconnect may be observed in Figure 3 SN65LVPE502A Successful Disconnect below.

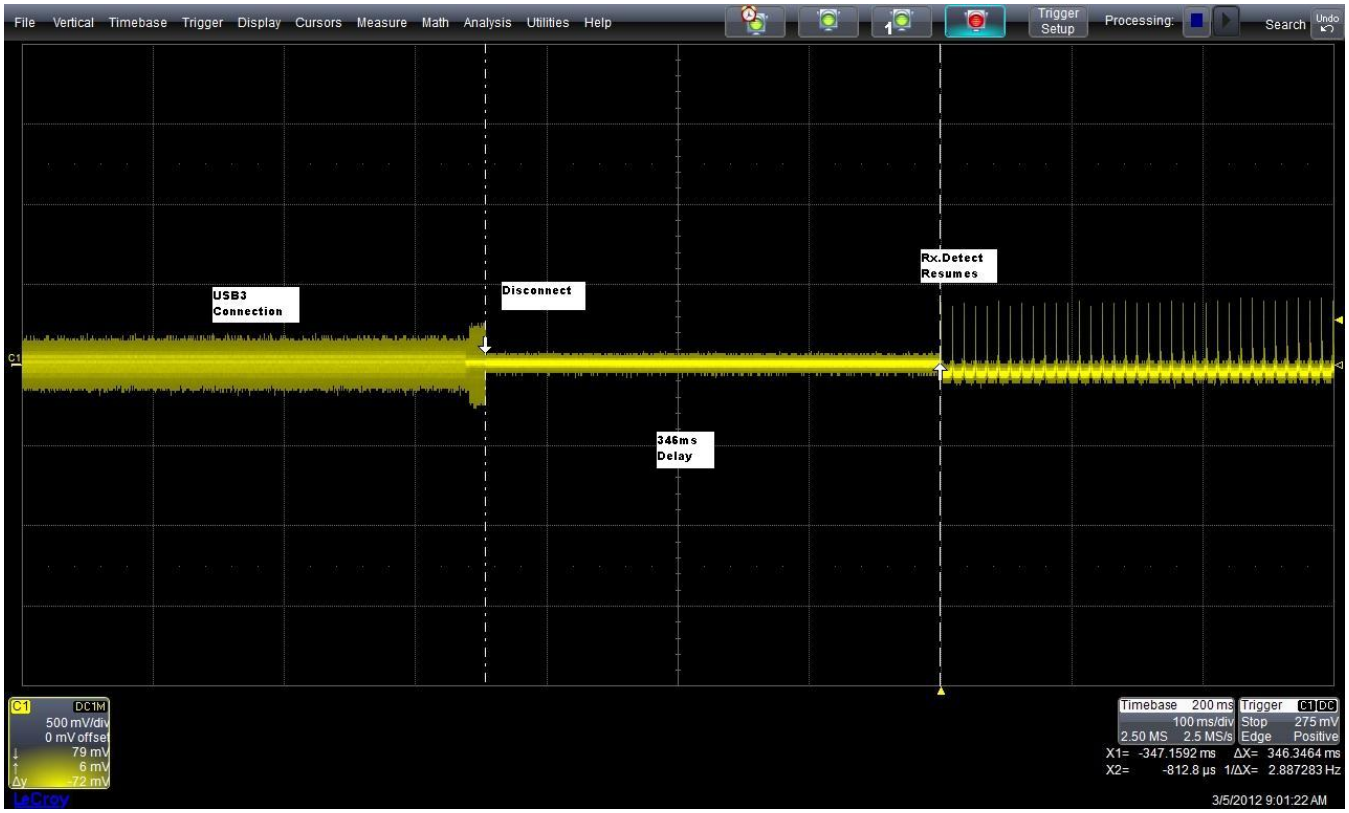

Figure 5 SN65LVPE502A Successful Disconnect

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