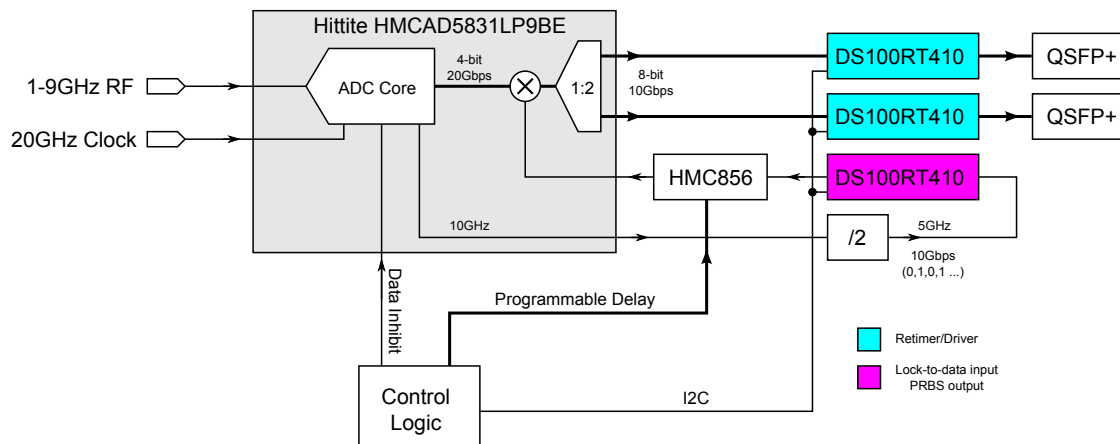# Hittite HMCAD5831LP9BE 3-bit plus over-range 20GHz ADC XOR Modulation Source

The Hittite ADC uses logic levels with a negative common-mode voltage. Connections to logic with a different common-mode voltage, eg., the TI retimer and Altera Stratix IV GT FPGA transceivers, requires AC-coupling and data modulation so that the serial data stream has no DC bias.

The Hittite ADC provides an XOR modulation port, so that data can be modulated with a user-defined pattern. The XOR port is sampled at 20GHz, so the timing margins of the external XOR source are very tight.

In the figure above, the ADC 10GHz output clock is divided-by-2 to generate a 10Gbps data stream consisting of a repeating 0, 1, 0, 1, ... serial data pattern. A single channel of a DS100RT410 would be configured to lock to the serial data pattern and output a PRBS pattern. The PRBS pattern would be synchronous to the ADC, but would have an arbitrary delay offset relative to the ADC clock. The HMC856 delay line would be used to adjust the timing of the PRBS pattern relative to the ADC clock.

The PRBS pattern is sampled at 20GHz clock rate, i.e., the 100ps period samples in the PRBS pattern are each sampled twice. The DS100RT410 total output jitter is specified as 10ps (typical) and the ADC samples the pattern every 50ps. The delay line will be used to adjust the relative timing of the PRBS pattern to the ADC clock, to provide a maximum timing margin of 40ps (20ps relative to the PRBS pattern edge transitions).

The Hittite ADC output drivers are not adequate for driving a QSFP+ cable. The figure shows two additional DT100RT410 devices used as QSFP+ drivers. In addition to providing cable driving, the eye monitor feature of the devices can be used to look at the ADC transmitter eye patterns.

The ADC output data is received and processed using Altera Stratix IV GT FPGAs. The FPGA transceivers are aligned using the PRBS pattern generator. To perform alignment, the data from the ADC core is disabled, so that the ADC output data lanes contain only the PRBS pattern. The receiving FPGA uses a common internal PRBS that uses the same PRBS9 polynomial. The PRBS is seeded from the first ADC receiver lane, and then the FPGA receiver delay (bit-slip) features are used to align all other lanes to the FPGA PRBS. At that point, all FPGA receivers lanes are aligned to the ADC+FPGA PRBS generators. This alignment is required, so that the FPGA can convert the ADC serial data back to 4-bit ADC samples for subsequent digital processing.

The FPGA XORs the ADC lanes the FPGA PRBS generator. When the data from the ADC core is inhibited and the ADC lanes contain only the PRBS pattern, the output of the FPGA XOR logic is a static zero - bit-error-rate counters in the FPGA will be used to check lanes remain synchronized. When the data from the ADC core is enabled, the output of the FPGA XOR logic is the ADC core data, i.e., the PRBS modulation is removed (demodulated) by the FPGA XOR logic.