・DS80PCI102

RXDET_A[1:0] ?

RXDET_B[1:0] ?

Table 7. Single EEPROM Header + Register Map with Default Value (continued)

Description	6	Ovrd_IDLE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Register		0x08 [4]							
Value		0	0	0	0	0	1	1	1
Description	7	Reserved	Reserved	Reserved	Reserved	Idle auto A	Idle sel A	Reserved	Reserved
Register						0x0E [5]	0x0E [4]		
Value		0	0	0	0	0	0	0	0
Description	8	CHA EQ[7]	CHA EQ[6]	CHA EQ[5]	CHA EQ[4]	CHA EQ[3]	CHA EQ[2]	CHA EQ[1]	CHA EQ[0]
Register		0x0F [7]	0x0F [6]	0x0F [5]	0x0F [4]	0x0F [3]	0x0F [2]	0x0F [1]	0x0F [0]
Value		0	0	1	0	1	1	1	1
Description	9	A Sel scp	A Sel lim	CHA VID[2]	CHA VID[1]	CHA VID[0]	Reserved	Reserved	Reserved
Register		0x10 [7]	0x10 [6]	0x10 [5]	0x10 [4]	0x10 [3]			
Value		1	0	1	0	1	1	0	1
Description	10	DEMA[2]	DEMA[1]	DEMA[0]	CHA Slow	IDLE tha[1]	IDLE tha[0]	IDLE thd[1]	IDLE thd[0]
Register		0x11 [2]	0x11 [1]	0x11 [0]	0x12 [7]	0x12 [3]	0x12 [2]	0x12 [1]	0x12 [0]
Value		0	1	0	0	0	0	0	0
Description	11	Idle auto B	Idle sel B	Reserved	Reserved	CHB EQ[7]	CHB EQ[6]	CHB EQ[5]	CHB EQ[4]
Register		0x15 [5]	0x15 [4]			0x16 [7]	0x16 [6]	0x16 [5]	0x16 [4]
Value		0	0	0	0	0	0	1	0
Description	12	CHB EQ[3]	CHB EQ[2]	CHB EQ[1]	CHB EQ[0]	B Sel scp	B Sel lim	CHB VID[2]	CHB VID[1]
Register		0x16 [3]	0x16 [2]	0x16 [1]	0x16 [0]	0x17 [7]	0x17 [6]	0x17 [5]	0x17 [4]
Value		1	1	1	1	1	0	1	0
Description	13	CHB VID[0]	Reserved	Reserved	Reserved	CHB DEM[2]	CHB DEM[1]	CHB DEM[0]	CHB Slow
Register		0x17 [3]				0x18 [2]	0x18 [1]	0x18 [0]	0x19 [7]
Value		1	1	0	1	0	1	0	0
Description	14	IDLE tha[1]	IDLE tha[0]	IDLE thd[1]	IDLE thd[0]	Reserved	Reserved	Reserved	Reserved
Register		0x19 [3]	0x19 [2]	0x19 [1]	0x19 [0]				
Value		0	0	0	0	0	0	0	0

・DS80PCI402(参考)

Table 6. EEPROM Register Map - Single Device with Default Value

EEPROM Address Byte		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Description	0	CRC EN	Address Map Present	EEPROM > 256 Bytes	RES	DEVICE COUNT[3]	DEVICE COUNT[2]	DEVICE COUNT[1]	DEVICE COUNT[0]
Value		0	0	0	0	0	0	0	0
Description	1	RES	RES	RES	RES	RES	RES	RES	RES
Value		0	0	0	0	0	0	0	0
Description	2	Max EEPROM Burst size[7]	Max EEPROM Burst size[6]	Max EEPROM Burst size[5]	Max EEPROM Burst size[4]	Max EEPROM Burst size[3]	Max EEPROM Burst size[2]	Max EEPROM Burst size[1]	Max EEPROM Burst size[0]
Value		0	0	0	0	0	0	0	0
Description	3	PWDN_ch7	PWDN_ch6	PWDN_ch5	PWDN_ch4	PWDN_ch3	PWDN_ch2	PWDN_ch1	PWDN_ch0
Value		0	0	0	0	0	0	0	0
Description	4	lpbk_1	lpbk_0	PWDN_INPUTS	PWDN_OSC	Ovrd_PRSNT	RES	RES	RES
Value		0	0	0	0	0	0	0	0
Description	5	RES	RES	RES	RES	RES	rxdet_btb_en	Ovrd_idle_th	Ovrd_RES
Value		0	0	0	0	0	1	0	0
Description	6	Ovrd_IDLE	Ovrd_RX_DET	Ovrd_RATE	Ovrd_RES	Ovrd_RES	rx_delay_sel_2	rx_delay_sel_1	rx_delay_sel_0
Value		0	0	0	0	0	1	1	1
Description	7	RD_delay_sel_3	RD_delay_sel_2	RD_delay_sel_1	RD_delay_sel_0	ch0_Idle_auto	ch0_Idle_sel	ch0_RXDET_1	ch0_RXDET_0
Value		0	0	0	0	0	0	0	0
Description	8	ch0_BST_7	ch0_BST_6	ch0_BST_5	ch0_BST_4	ch0_BST_3	ch0_BST_2	ch0_BST_1	ch0_BST_0
Value		0	0	1	0	1	1	1	1
Description	9	ch0_Sel_scp	ch0_Sel_mode	ch0_RES_2	ch0_RES_1	ch0_RES_0	ch0_VOD_2	ch0_VOD_1	ch0_VOD_0
Value		1	0	1	0	1	1	0	1
Description	10	ch0_DEM_2	ch0_DEM_1	ch0_DEM_0	ch0_Slow	ch0_idle_tha_1	ch0_idle_tha_0	ch0_idle_thd_1	ch0_idle_thd_0
Value		0	1	0	0	0	0	0	0
Description	11	ch1_Idle_auto	ch1_Idle_sel	ch1_RXDET_1	ch1_RXDET_0	ch1_BST_7	ch1_BST_6	ch1_BST_5	ch1_BST_4
Value		0	0	0	0	0	0	1	0
Description	12	ch1_BST_3	ch1_BST_2	ch1_BST_1	ch1_BST_0	ch1_Sel_scp	ch1_Sel_mode	ch1_RES_2	ch1_RES_1
Value		1	1	1	1	1	0	1	0
Description	13	ch1_RES_0	ch1_VOD_2	ch1_VOD_1	ch1_VOD_0	ch1_DEM_2	ch1_DEM_1	ch1_DEM_0	ch1_Slow
Value		1	1	0	1	0	1	0	0
Description	14	ch1_idle_tha_1	ch1_idle_tha_0	ch1_idle_thd_1	ch1_idle_thd_0	ch2_Idle_auto	ch2_Idle_sel	ch2_RXDET_1	ch2_RXDET_0
Value		0	0	0	0	0	0	0	0
Description	15	ch2_BST_7	ch2_BST_6	ch2_BST_5	ch2_BST_4	ch2_BST_3	ch2_BST_2	ch2_BST_1	ch2_BST_0
Value		0	0	1	0	1	1	1	1