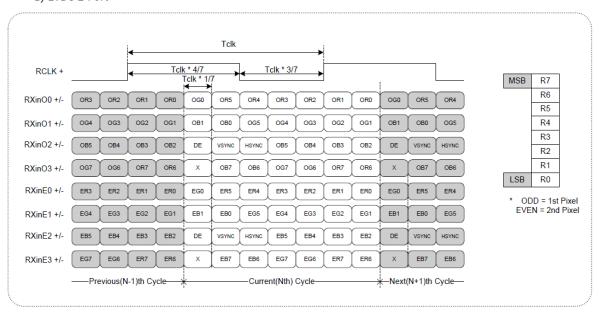
## TFP403/DS90C387A configuration (old mode snlu036)

PLLSEL	High
DUAL	High
!PD	High
R_FDE	High
DFO	LOW
OCK_INV	High
PIXS	High
R_FB	LOW
PRE	LOW

# 3. Data Format 1) LVDS 2 Port

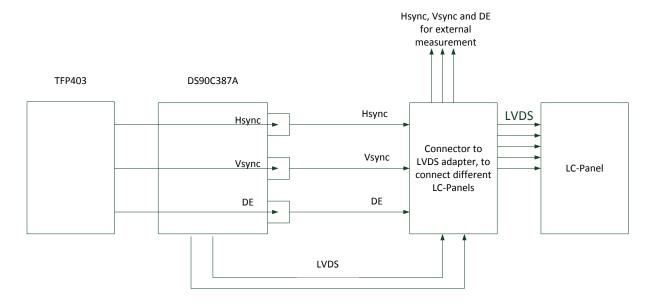


< LVDS Data Format >

#### Successfully checked

- Supply voltage = 3.29V, no swing
- All soldered pins are checked
- EEPROM works fine and PC detects bridge with correct values
- GND plane shows only a small offset voltage

#### Connection between TFP401, DS90C387A and adapter pcb



**Abbildung 1 Connection schematic** 

The above picture shows the signal way of Hsync, Vsync and DE. The signals come from TFP403 and goes to the input of DS90C387A. After that Hsync, Vsync and DE goes to an adapter pcb where an OP amplified the signal for external measurement (unfortunately I got no signal on OP output). I tapped the signals to use in future with an FPGA or other microprocessor. I decided to use an OP to prevent changing impedance of these 3 signal lines. I used 50 ohm termination on OP's input. See next picture. I attached the whole schematic on the last pages.

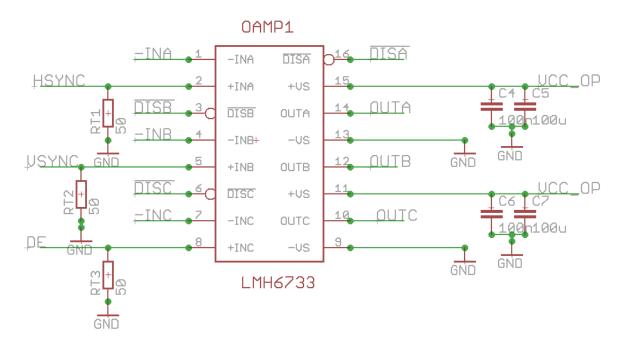


Abbildung 2 Hsync, Vsync, DE amplifying

### Measured signals

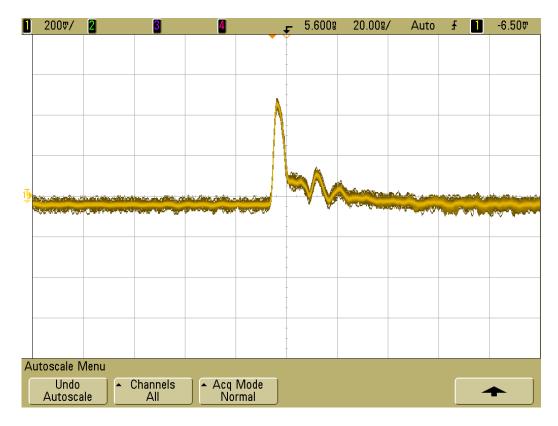
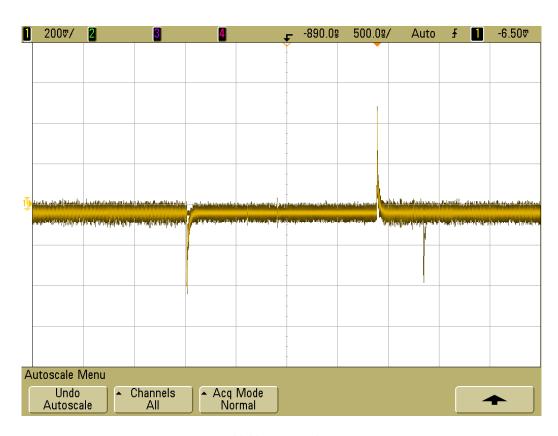
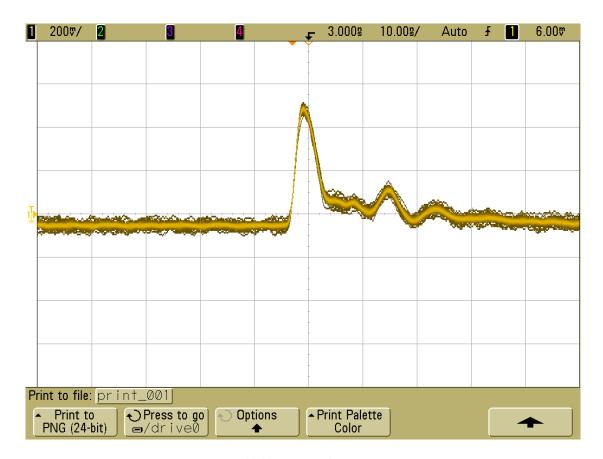


Abbildung 3 Signal: DE



**Abbildung 4 Signal: DE** 



**Abbildung 5 Signal: Hsync** 

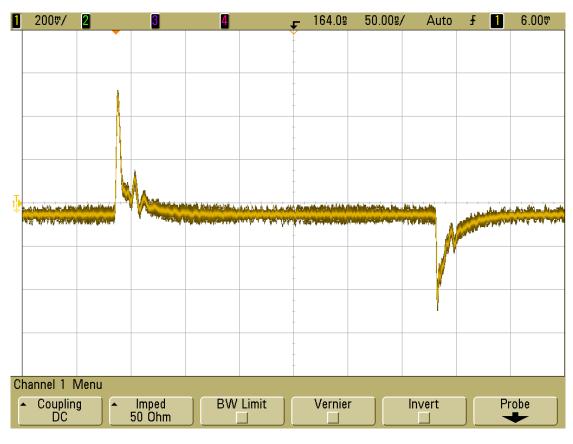


Abbildung 6 Signal: Hsync

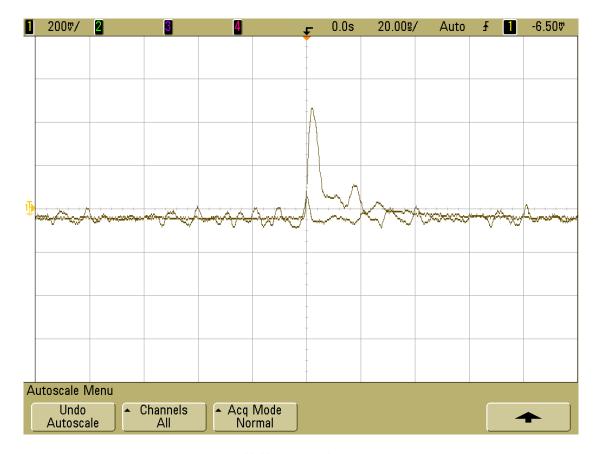


Abbildung 7 Signal: Vsync

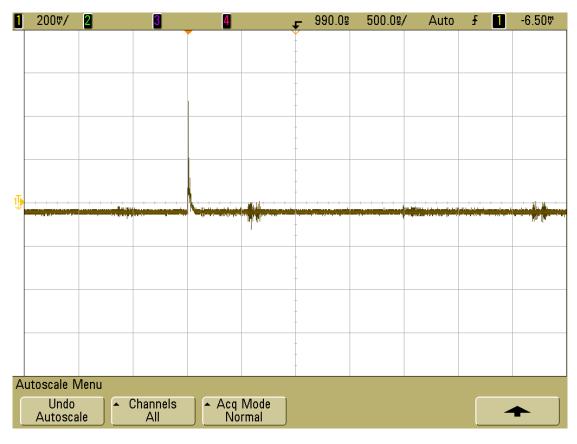


Abbildung 8 Signal: Vsync

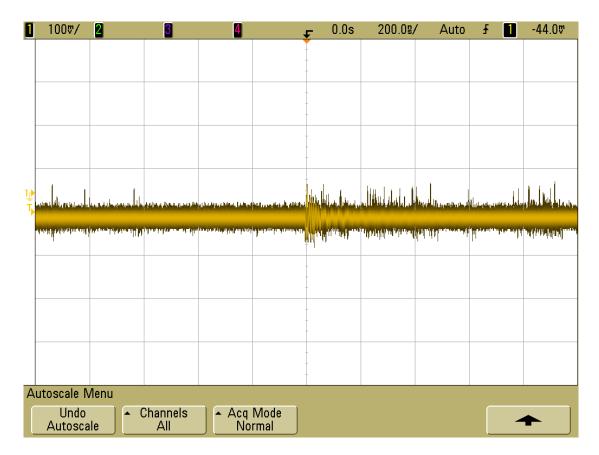


Abbildung 9 Signal: GND

The following two pages show the schematics for DVItoLVDS bride and the adapter schematic.

