

TP1
VCC

TP2
GND

+3.6V MAX

J2

J1

- RXOUT27 GND
- RXOUT26 GND
- RXOUT25 GND
- RXOUT24 GND
- RXOUT23 GND
- RXOUT22 GND
- RXOUT21 GND
- RXOUT20 GND
- RXOUT19 GND
- RXOUT18 GND
- RXOUT17 GND
- RXOUT16 GND
- RXOUT15 GND
- RXOUT14 GND
- RXOUT13 GND
- RXOUT12 GND
- RXOUT11 GND
- RXOUT10 GND
- RXOUT 9 GND
- RXOUT 8 GND
- RXOUT 7 GND
- RXOUT 6 GND
- RXOUT 5 GND
- RXOUT 4 GND
- RXOUT 3 GND
- RXOUT 2 GND
- RXOUT 1 GND
- RXOUT 0 GND
- RXCLKOUT GND
- GND

26

R4 R5 R6

U1

R7
R9
R11
R13
R15
R17
R19
R21
R23
R25
R27

IN0 R3
+ R2
- IN1 R1
+ R30
- IN2 R31
+ R34
R33
CLK R32
+ R29
- IN3 R28

JP1

VCC GND
/PD

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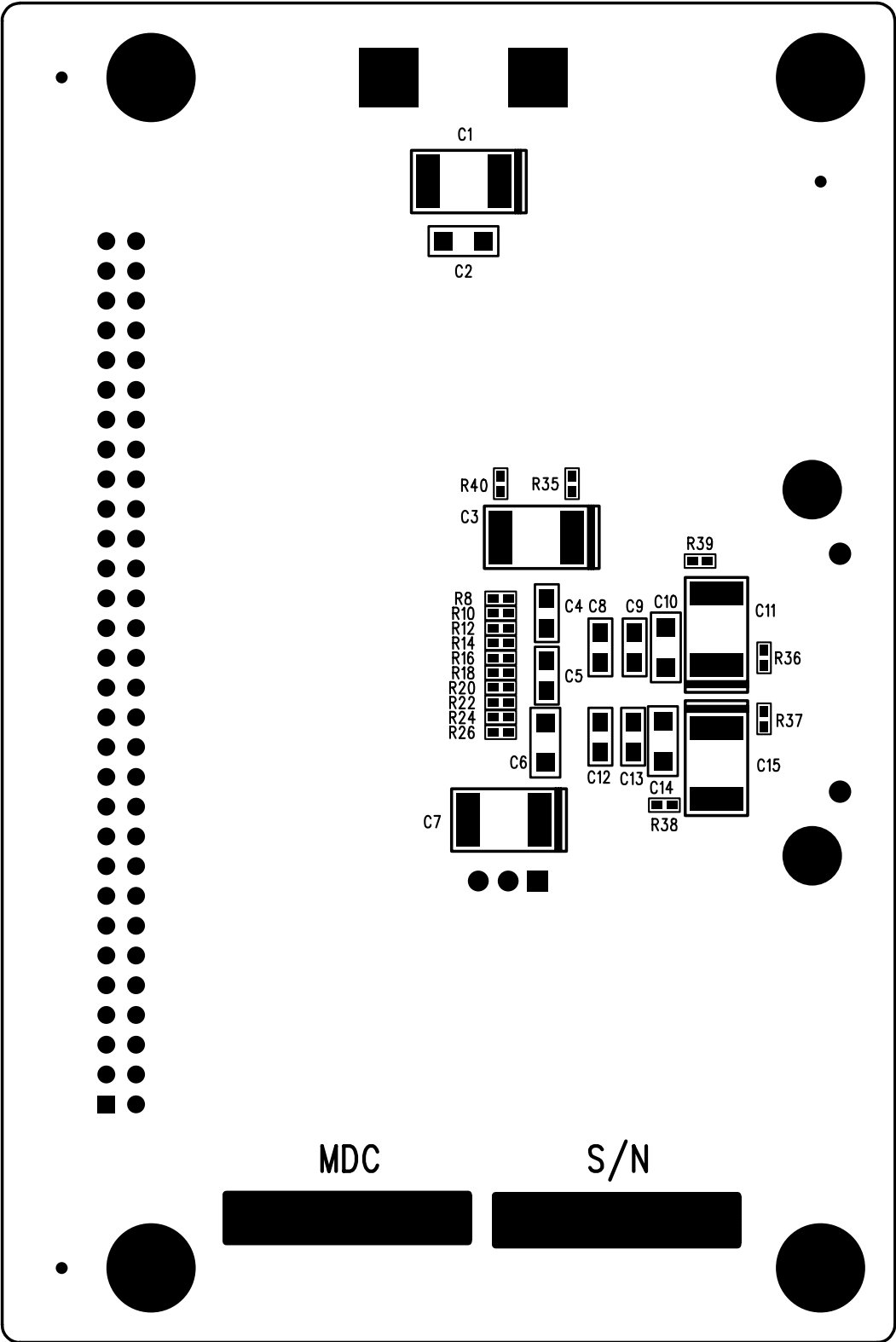
HSL RX 8 BIT

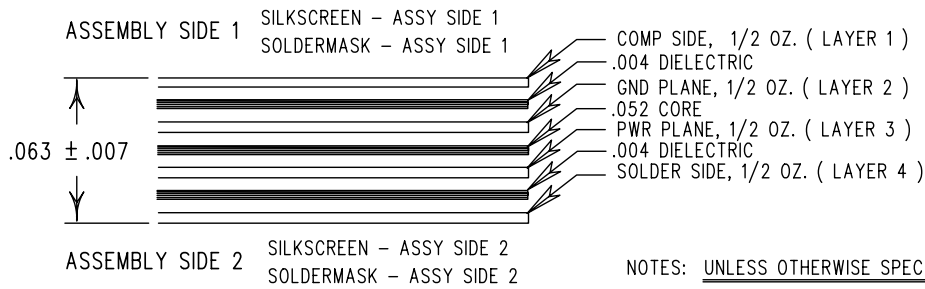
MADE IN U.S.A.

ASSY HSL RX 8 BIT REV

60 59

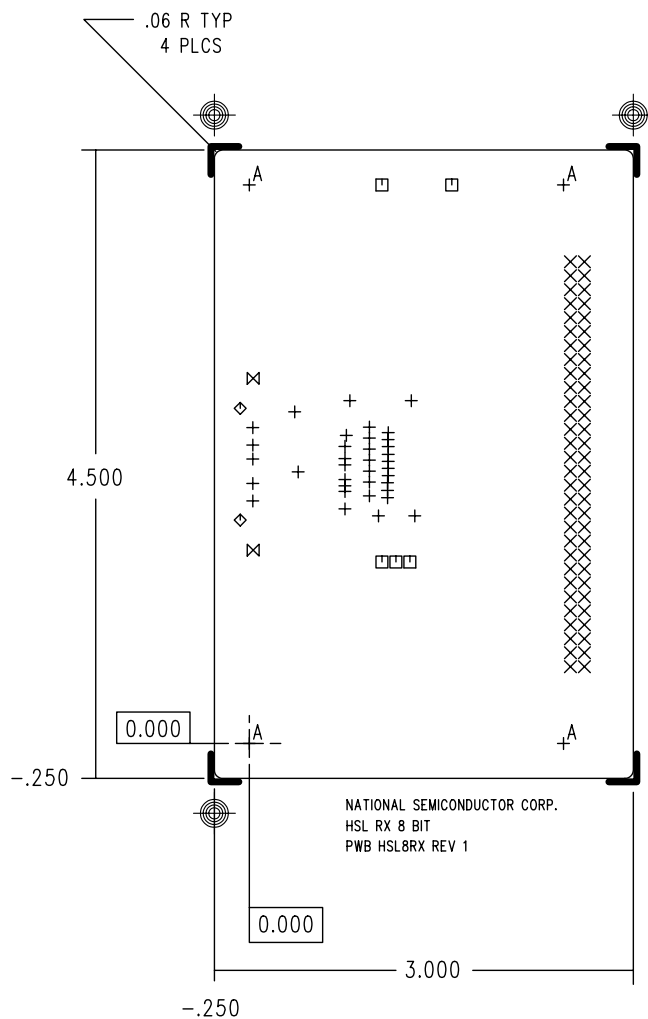
2 1



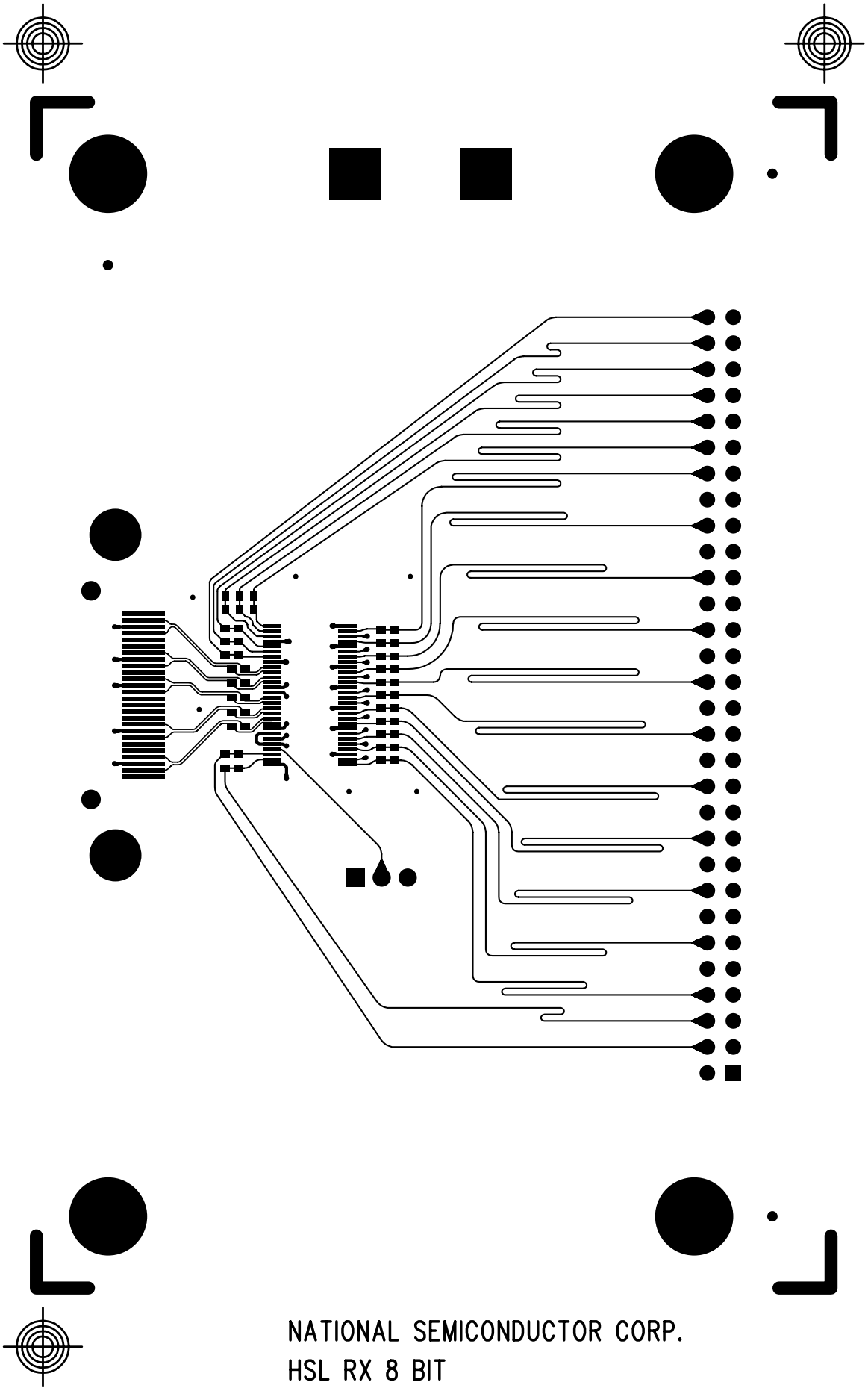


NOTES: UNLESS OTHERWISE SPECIFIED

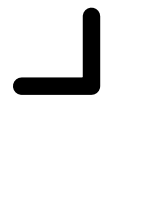
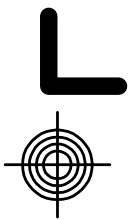
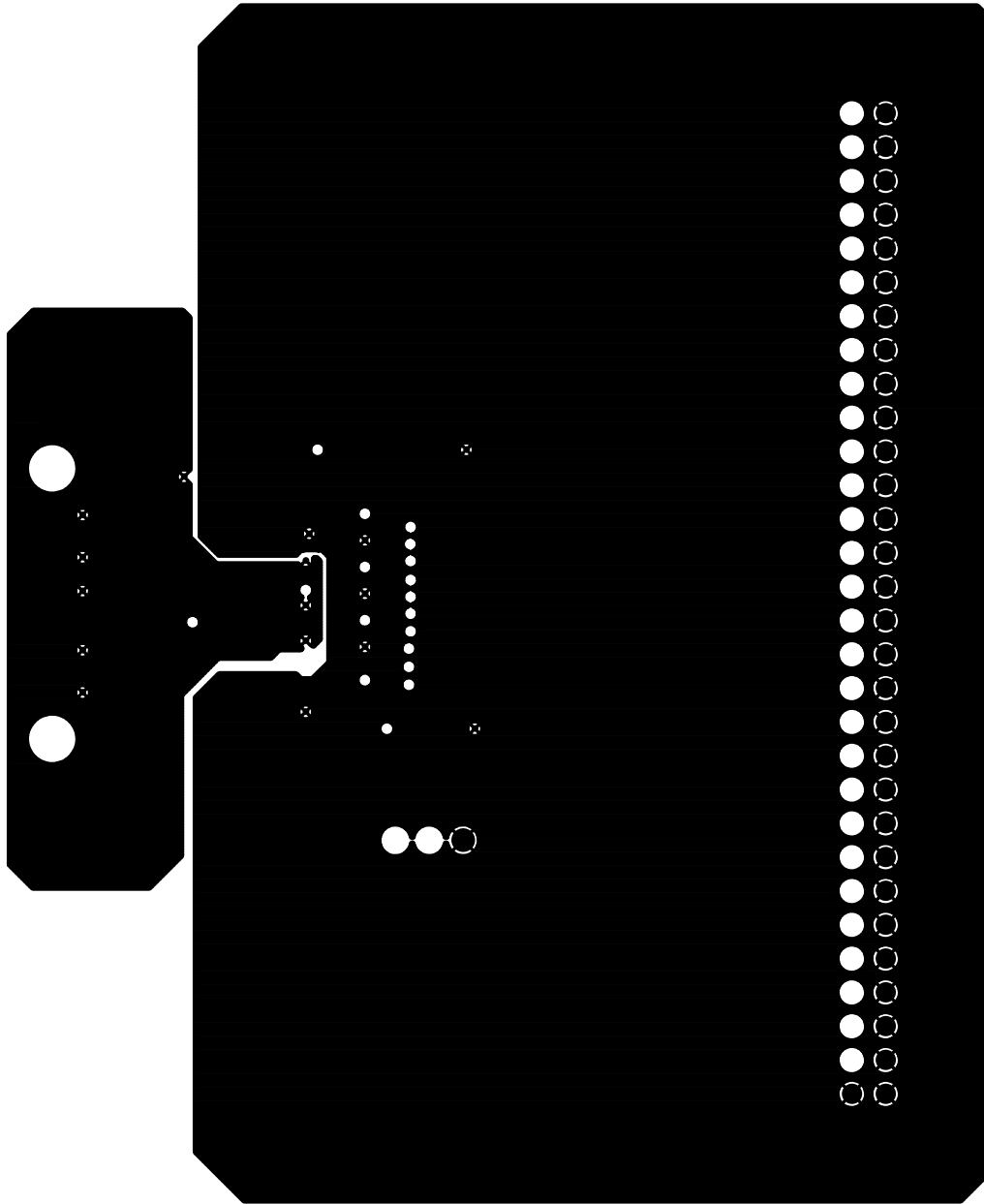
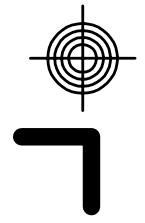
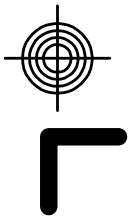
1. COMPONENT SIDE IS SHOWN.
2. DELETED.
3. FABRICATE USING MASTER FILM HSL RX 8 BIT REV 1.
4. ACCEPTABILITY SHALL BE BASED ON IPC-A-600, CLASS 2
5. MATERIAL: BASE MATERIAL IS NEMAL-1 GRADE FR4, COLOR GREEN, 0.063 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1/2 OZ.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER; .0005 MIN OVER-PLATED WITH TIN / LEAD, 60-40; HASL.
7. FABRICATION TOLERANCES:
END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .003 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC-SM-840, TYPE A, CLASS B. COLOR-GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR-WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE 0.00675 MILL TRACES TO BE 50 OHM IMPEDANCE AND THE FIVE MILL (.005) TRACES TO BE 100 OHM DIFFERENTIAL PAIRS. THE 4 MILL (.004) DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO-MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/- 5%.



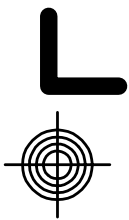
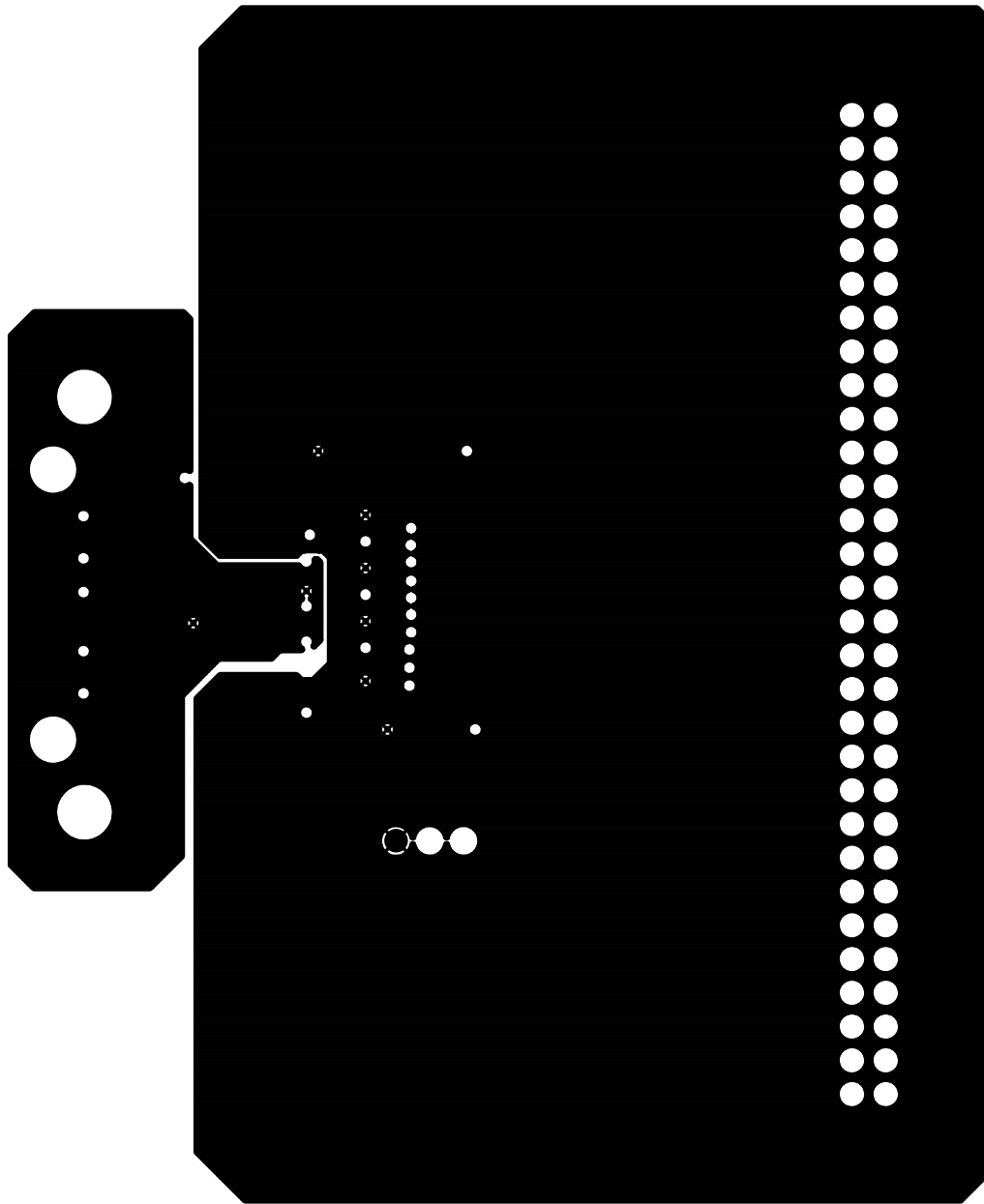
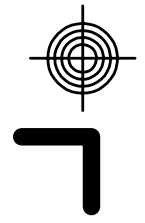
HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.009	36	YES	± .003
X	0.038	60	YES	± .003
□	0.043	5	YES	± .003
◇	0.079	2	NO	± .003
⊠	0.109	2	YES	± .003
A	0.156	4	YES	± .005



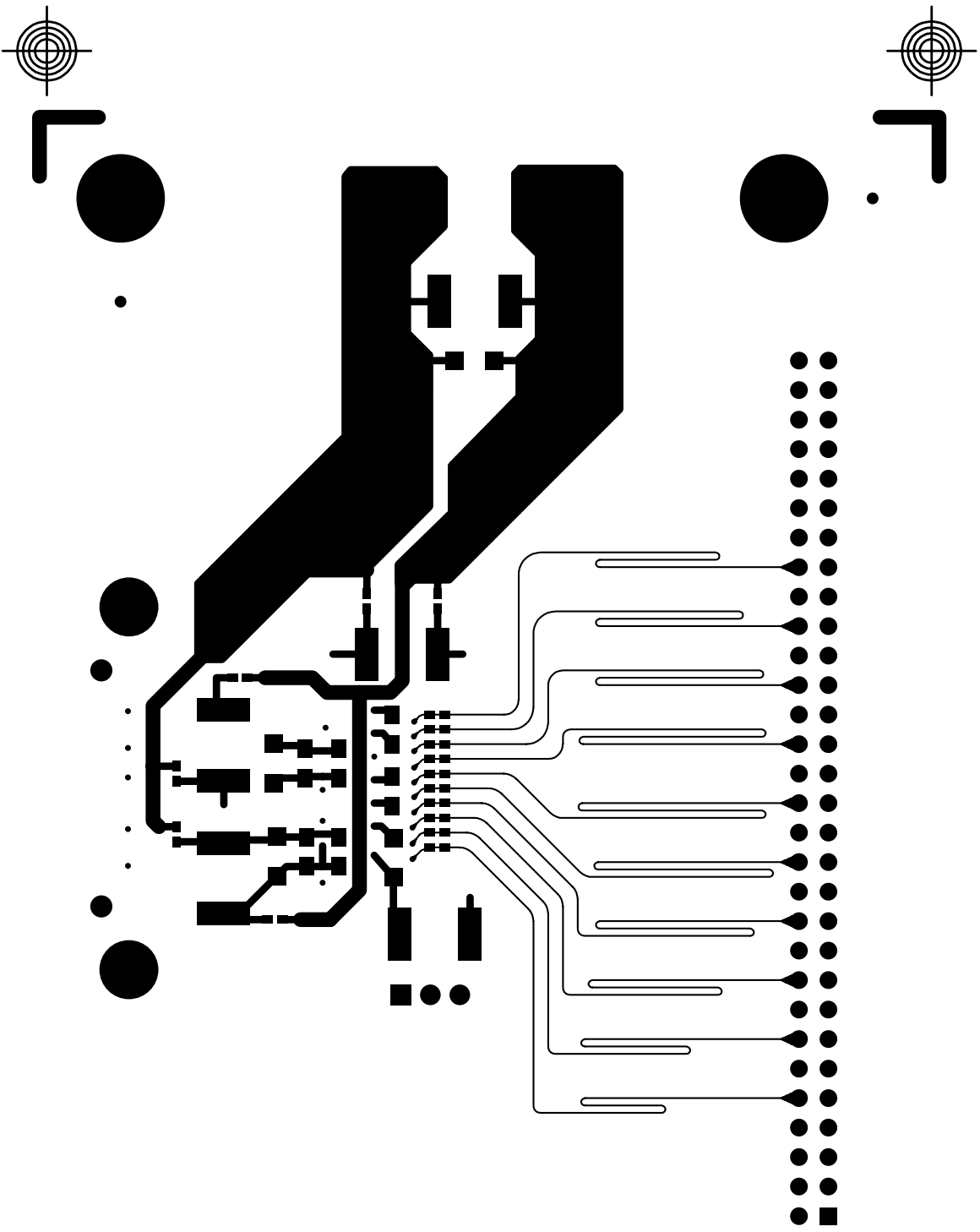
NATIONAL SEMICONDUCTOR CORP.
HSL RX 8 BIT
PWB HSL8RX REV 1
LAYER 1 - PRIMARY ASSY SIDE



NATIONAL SEMICONDUCTOR CORP.
HSL RX 8 BIT
PWB HSL8RX REV 1
LAYER 2 - GROUND PLANE

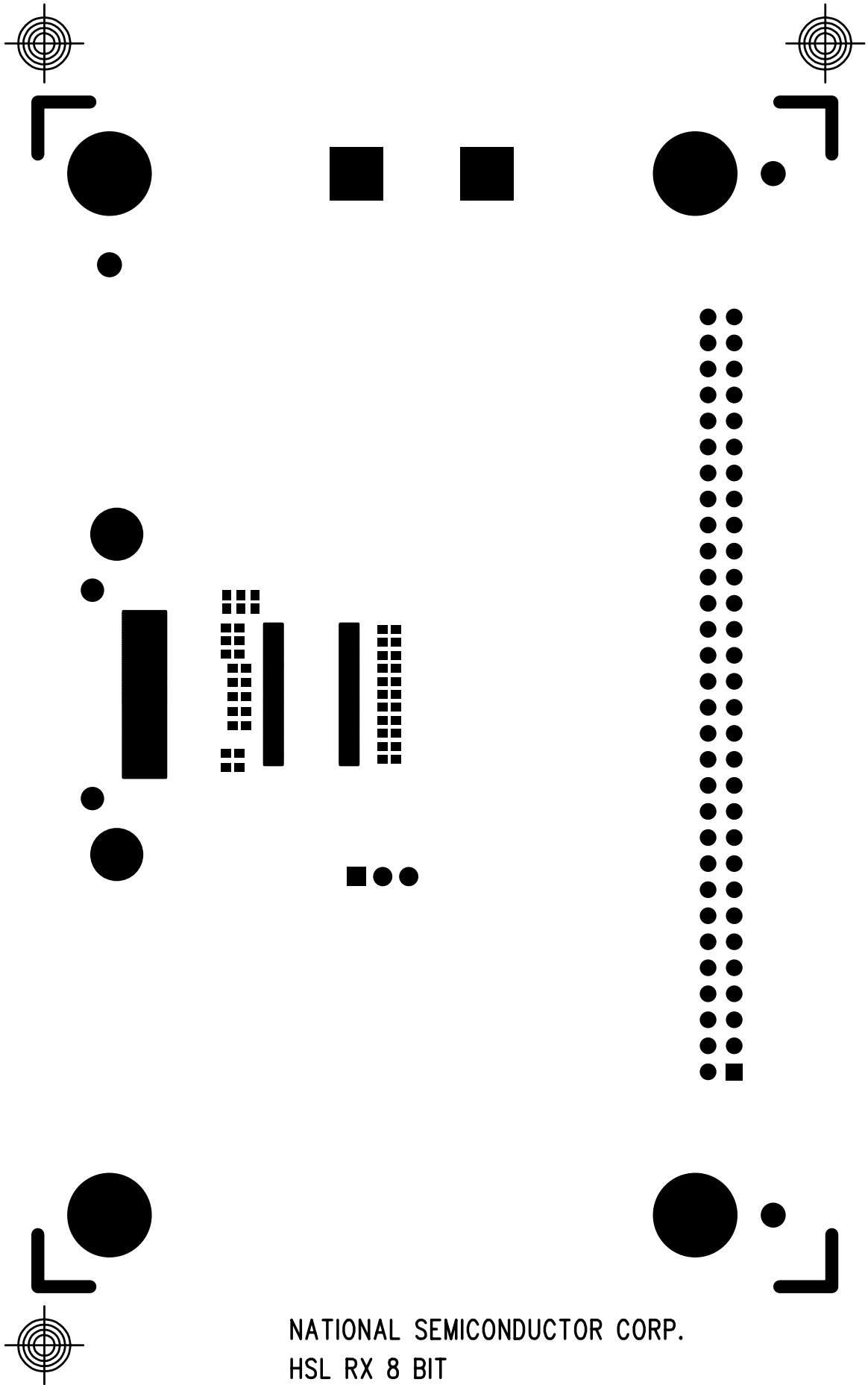


NATIONAL SEMICONDUCTOR CORP.
HSL RX 8 BIT
PWB HSL8RX REV 1
LAYER 3 - POWER PLANE

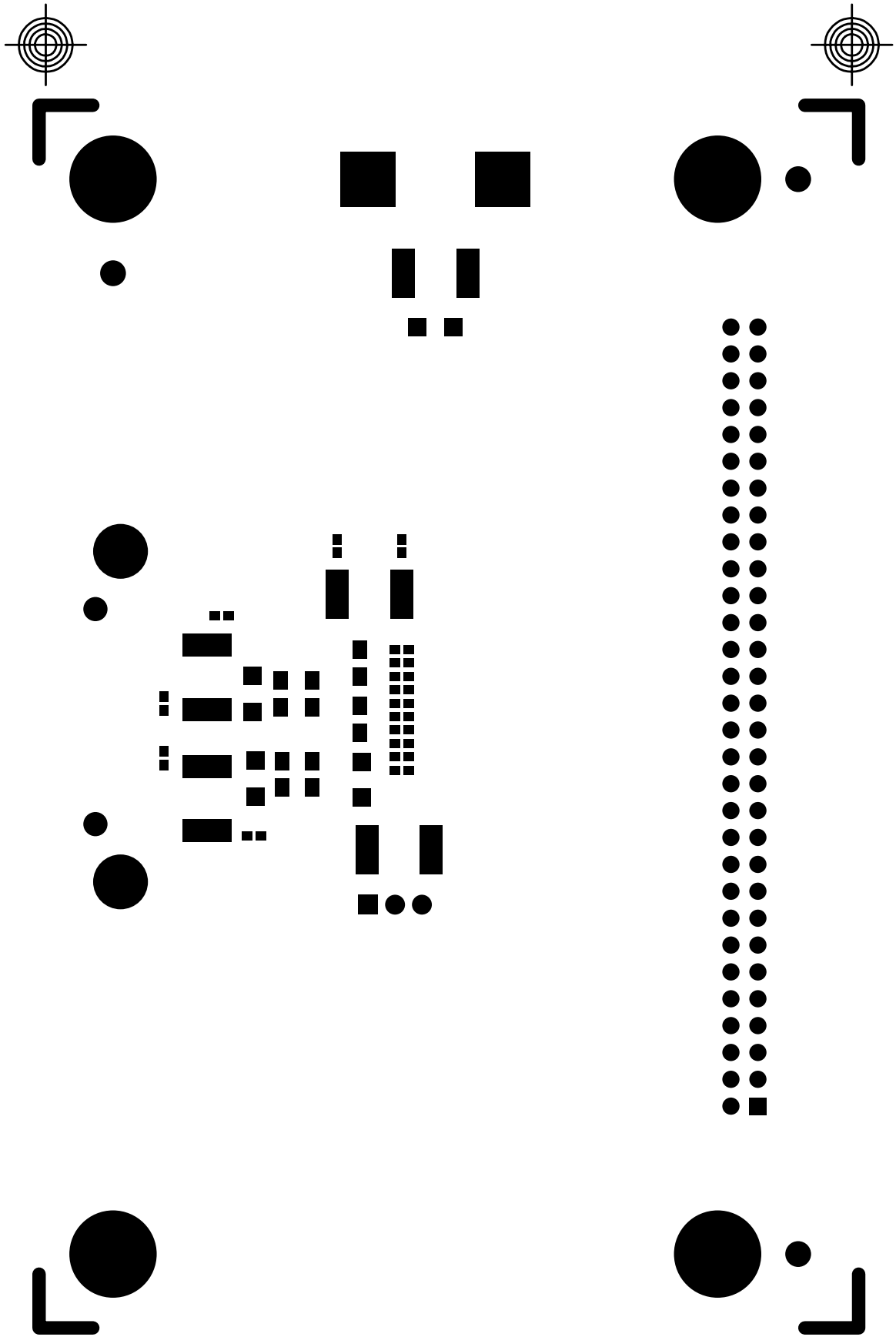


PWB H2L RX 8 BIT REV 1

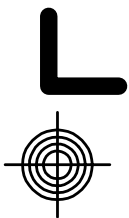
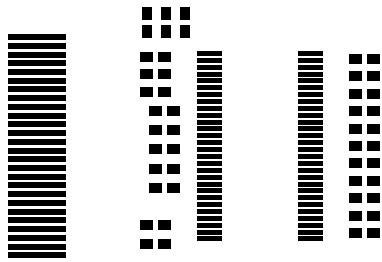
NATIONAL SEMICONDUCTOR CORP.
HSL RX 8 BIT
PWB HSL8RX REV 1
LAYER 4 - SECONDARY ASSY SIDE



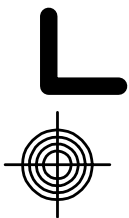
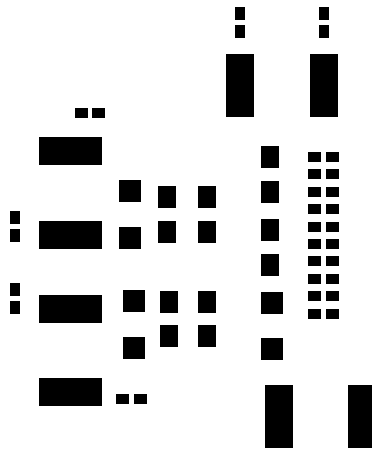
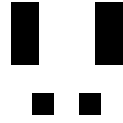
NATIONAL SEMICONDUCTOR CORP.
HSL RX 8 BIT
PWB HSL8RX REV 1
SOLDER MASK - PRIMARY SIDE



NATIONAL SEMICONDUCTOR CORP.
HSL RX 8 BIT
PWB HSL8RX REV 1
SOLDER MASK - SECONDARY SIDE



NATIONAL SEMICONDUCTOR CORP.
HSL RX 8 BIT
PWB HSL8RX REV 1
PASTE MASK - PRIMARY SIDE



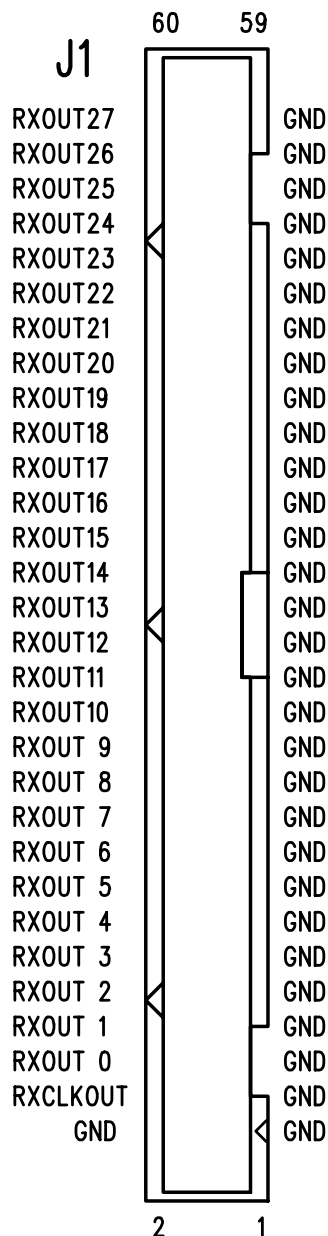
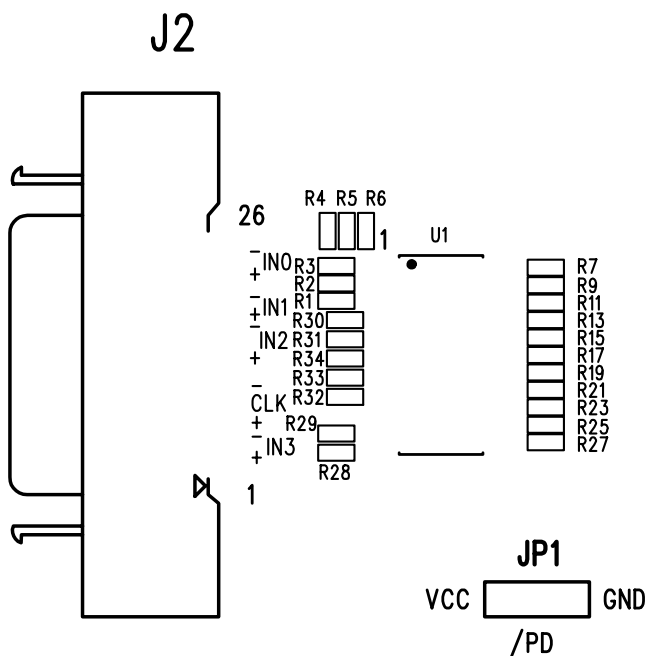
NATIONAL SEMICONDUCTOR CORP.
HSL RX 8 BIT
PWB HSL8RX REV 1
PASTE MASK - SECONDARY SIDE



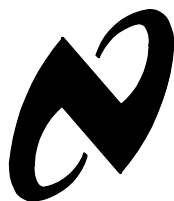
TP1
VCC

TP2
GND

+3.6V MAX



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HSL RX 8 BIT

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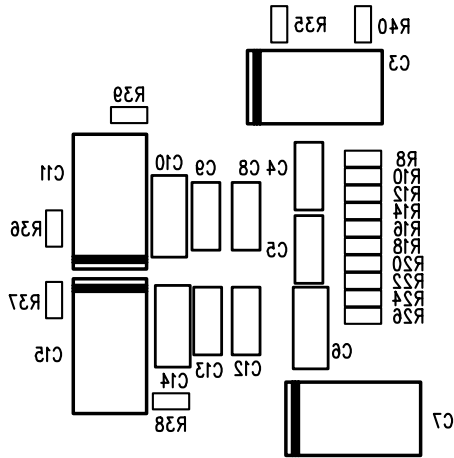
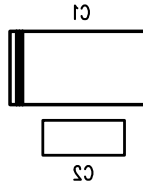
ASSY HSL RX 8 BIT

REV

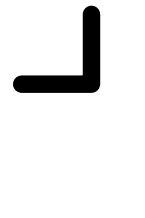
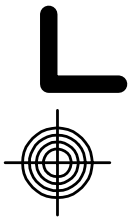


NATIONAL SEMICONDUCTOR CORP.
HSL RX 8 BIT
PWB HSL8RX REV 1
SILKSCREEN - PRIMARY SIDE





MDC 2\N



NATIONAL SEMICONDUCTOR CORP.
 HSL RX 8 BIT
 PWB HSL8RX REV 1
 SILKSCREEN - SECONDARY SIDE