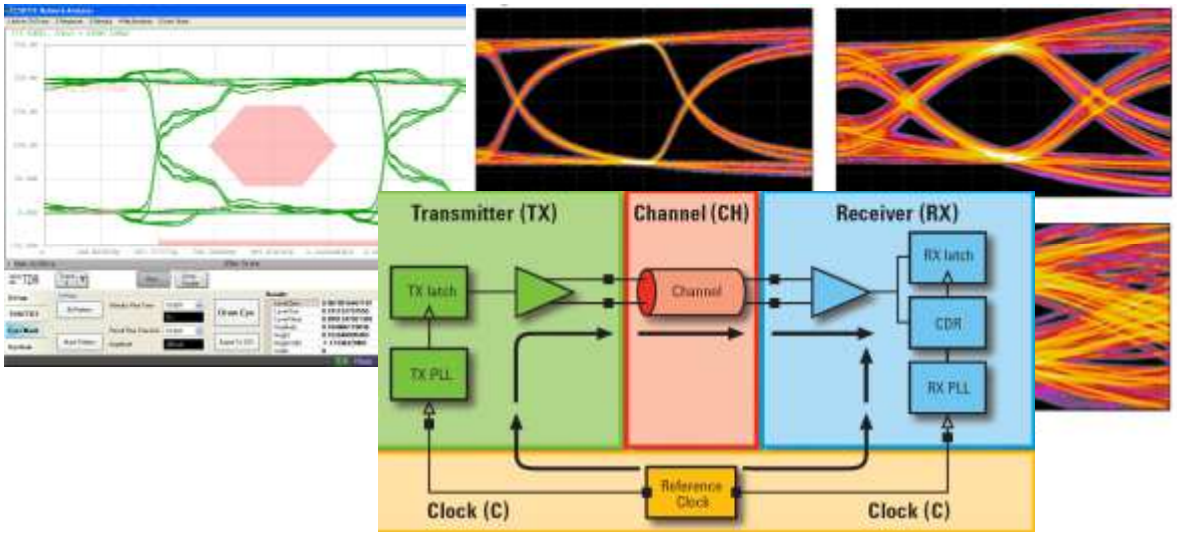
Cleaning the Rusty Channel

Emphasis, Equalization & Embedding



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Agenda

1. Introduction
2. Emphasis
3. Equalization
4. Virtual probing / De-Embedding
5. Probing Hardware
6. Practical examples (see next page)
7. Summary

Agenda continued

6. Practical Examples

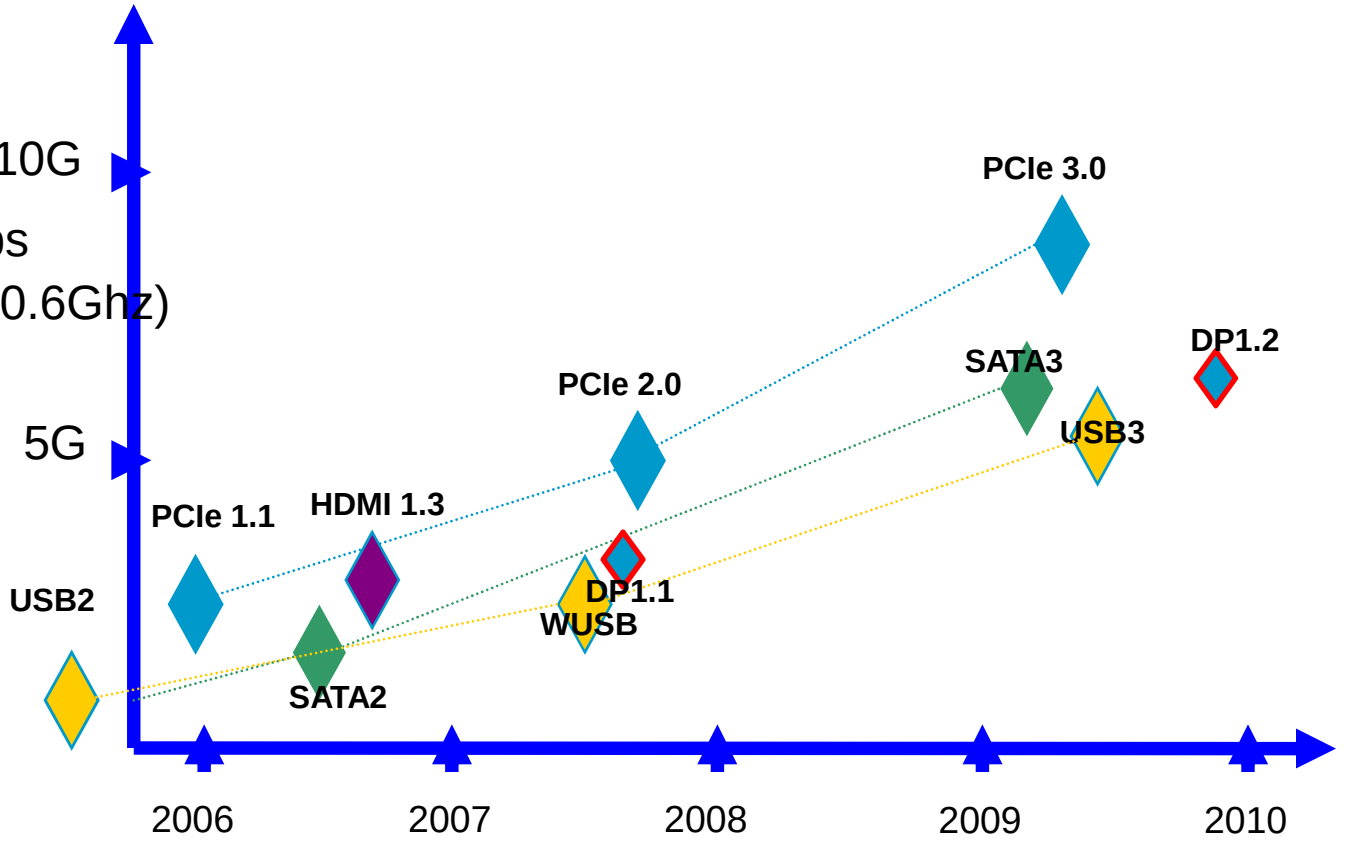
1. High-Speed Characterization (effect of 4.5 GHz Notch in test fixture)
2. BGA probe setup in infiniisim Virtual Probe
3. Tuned, measurement enhanced, IBIS parameters for DDR
4. Creating S2P (touchstone) files from Gerber files
5. Basic Steps for Optimizing a Serial Link
6. Serial Data Analysis Solutions: 8b10b Trigger, Decode, Search and Listing Feature
7. Small peek inside the 90.000 X 32 GHz scope

Agenda

1. ***Introduction***
2. **Pre-Emphasis**
3. **Equalization**
4. **Virtual probing / De-Embedding**
5. **Probing Hardware**
6. **Practical examples (see next page)**
7. **Summary**

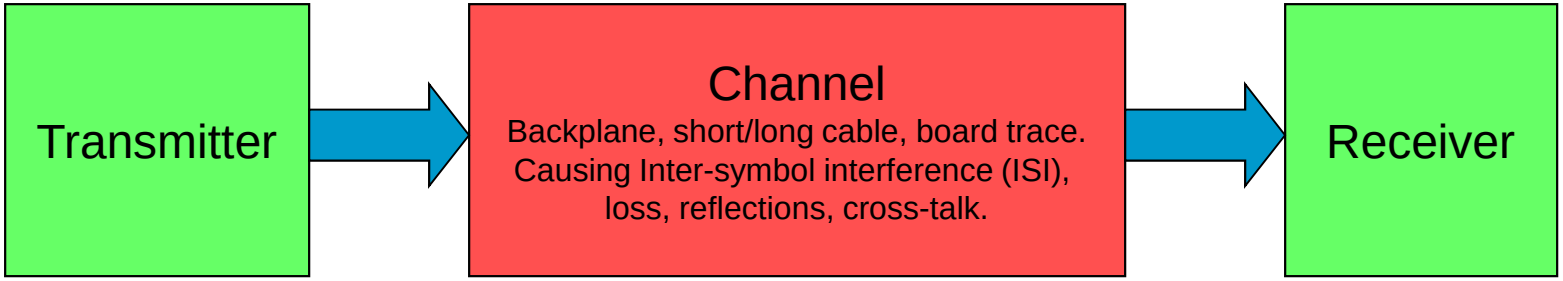
Generic Trend: Rates Going Higher & Higher

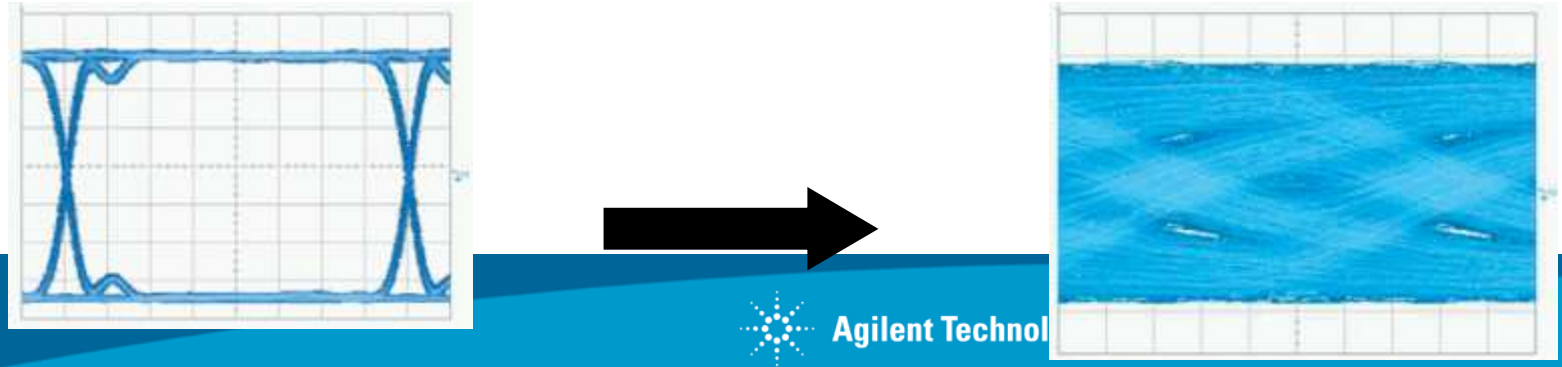
- **PCI Express**
  - 2.5 GT/s
  - (2.0) 5 GT/s
  - (3.0) 8 GT/s
- **USB Technologies**
  - USB 2.0 480Mbps
  - WUSB (RF 3.1-10.6Ghz)
  - USB 3.0 5GT/s
- **SATA**
  - 1.5Gbps
  - 3Gbps
  - 6Gbps
- **HDMI 1.3**
  - 3.4Gbps
- **DisplayPort**
  - 2.7 Gbps
  - 5.4Gbps



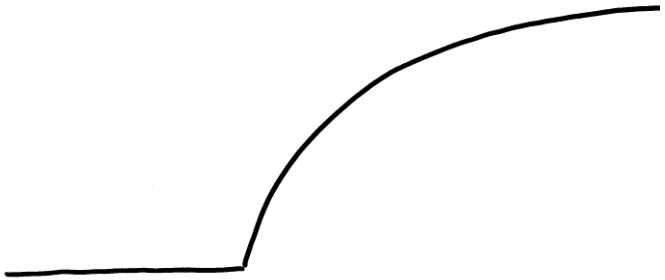
Generic Trend: Focus on Signal Integrity

Example ISI Jitter in Serial system:

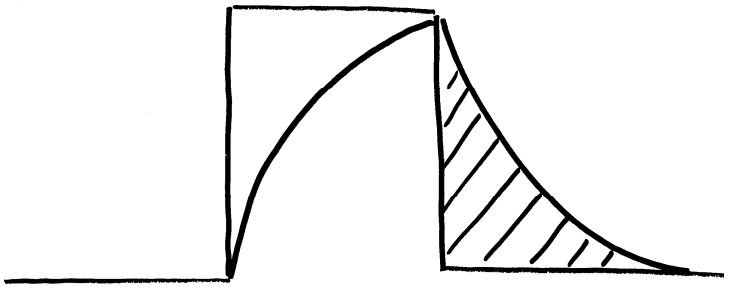




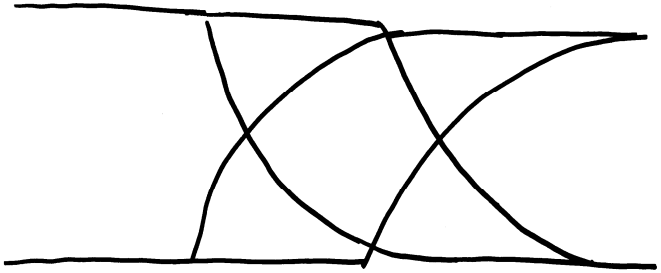
Intersymbol Interference (ISI)



Single-pole RC time constant



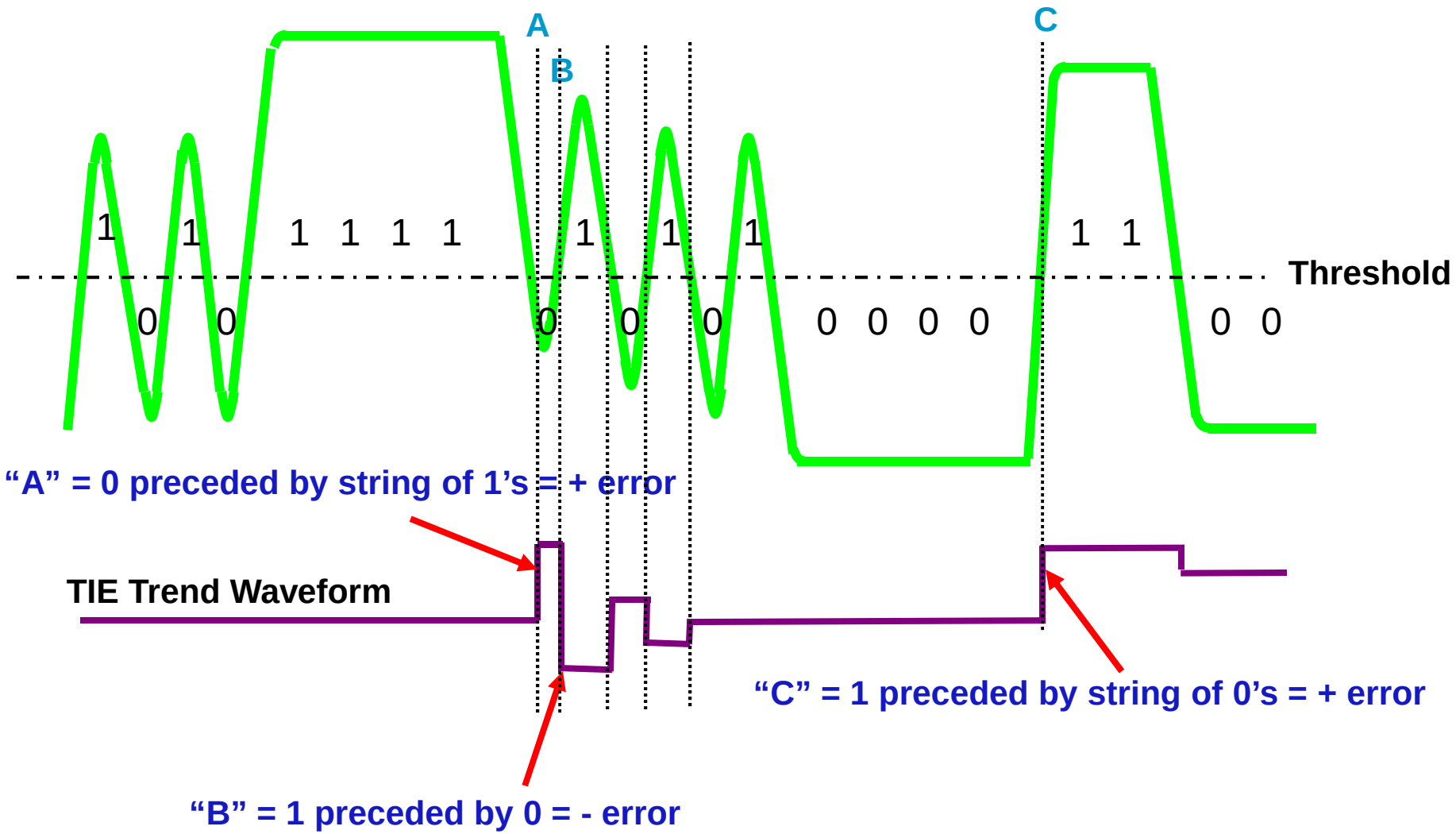
Effect on an isolated “1”



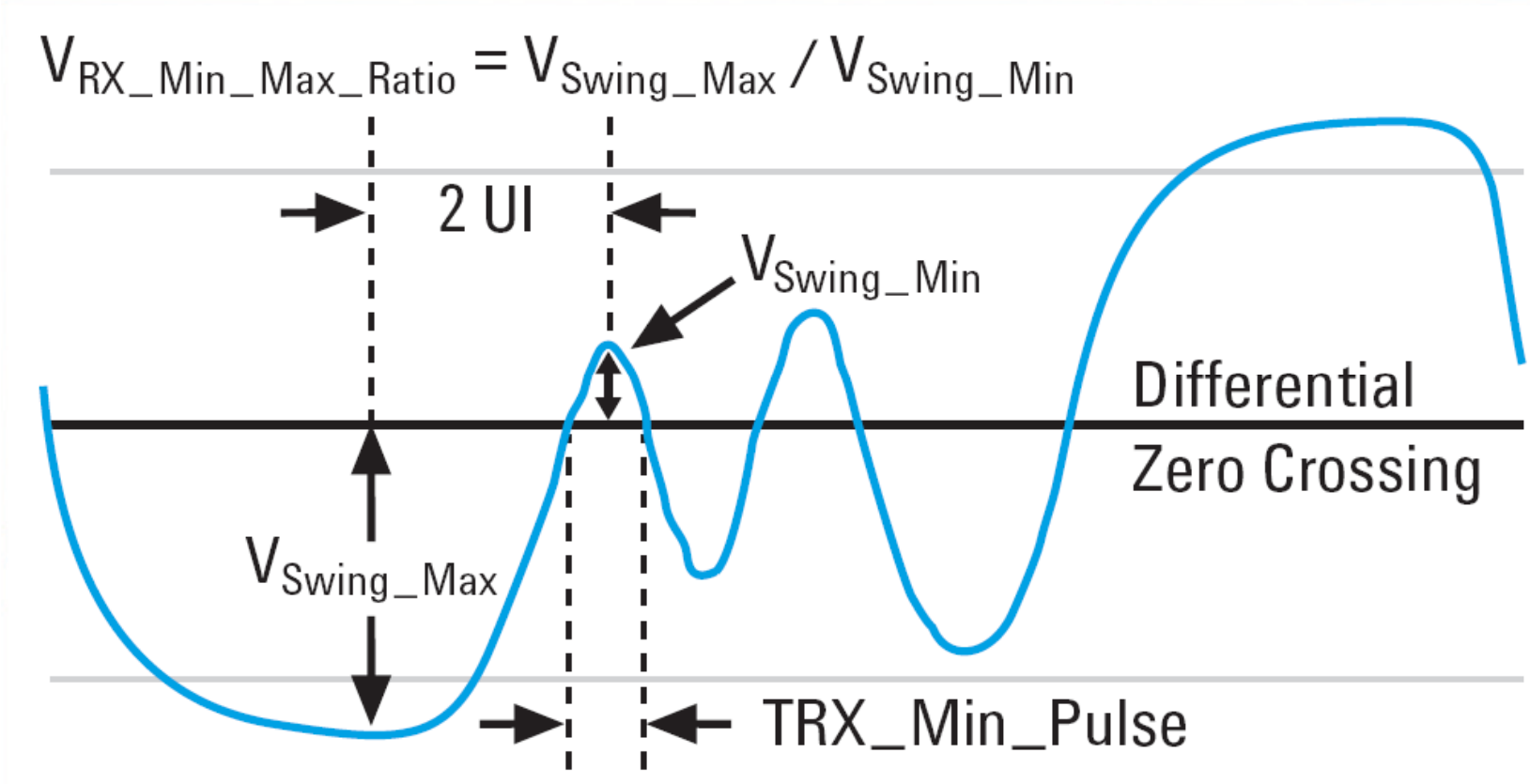
Effect on data eye

Inter-Symbol Interference (ISI)

Transmission Line Bandwidth Limitation Problem



Definition of ISI

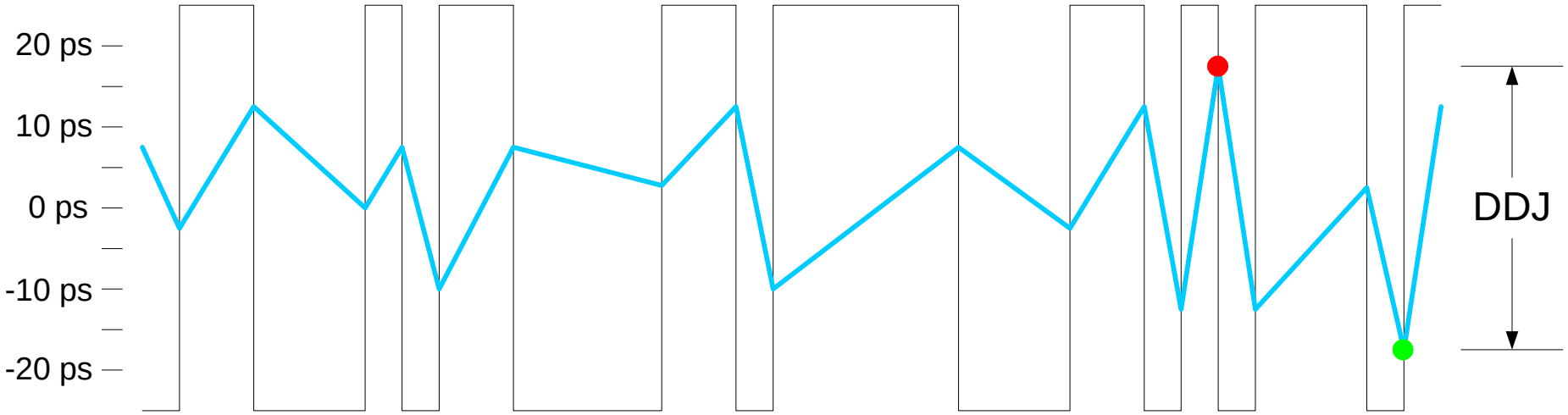


Data Dependent Jitter

Interaction of ISI and DCD means

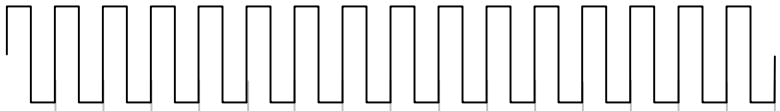
The characterization of a backplane changes with

- DCD
- Data rate
- Data pattern

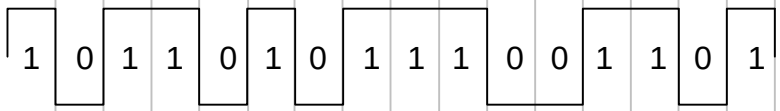


Effect of Jitter on the Eye Diagram

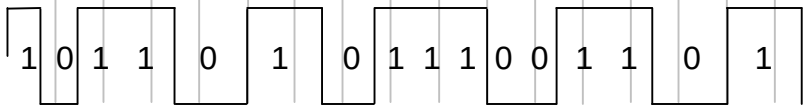
Ideal Trigger Signal:



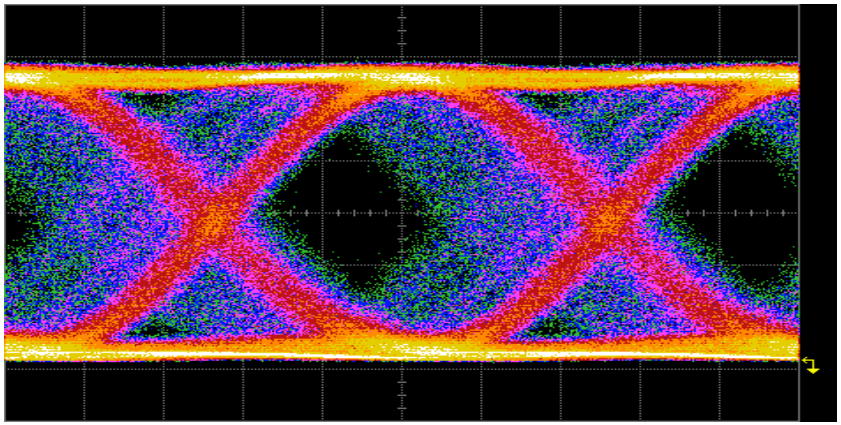
Ideal Data:



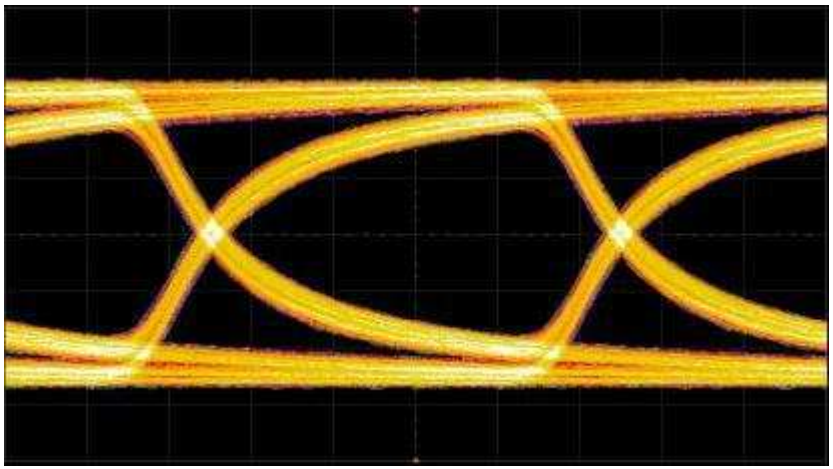
Jittered Data:



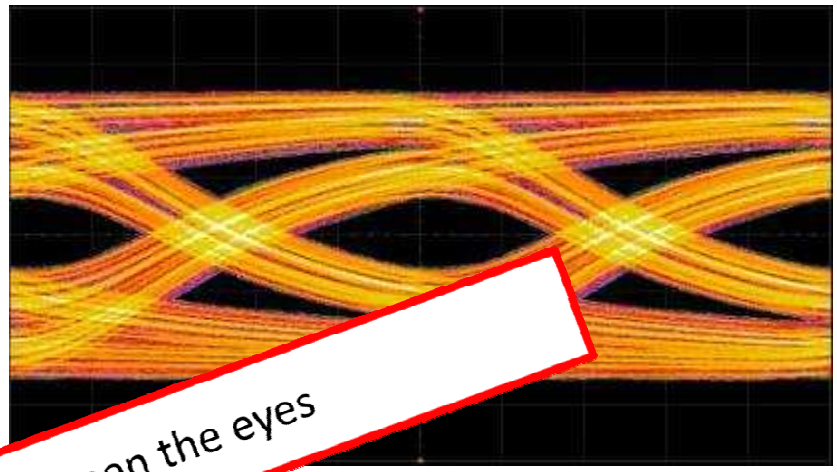
Jitter in the Eye Diagram:



Key measure is eye quality

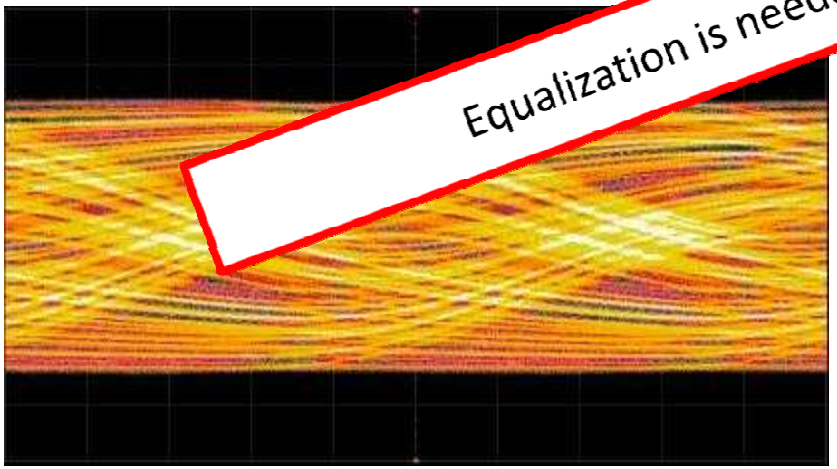


Unequalized 1Gb/s

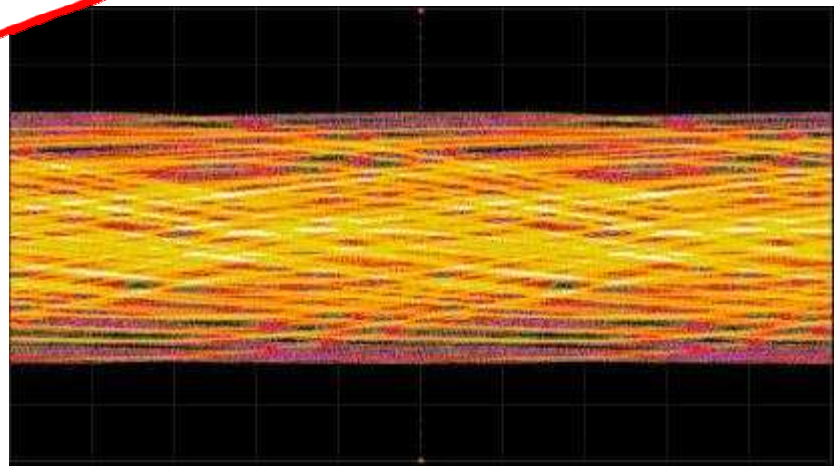


Unequalized 3Gb/s

Equalization is needed to open the eyes

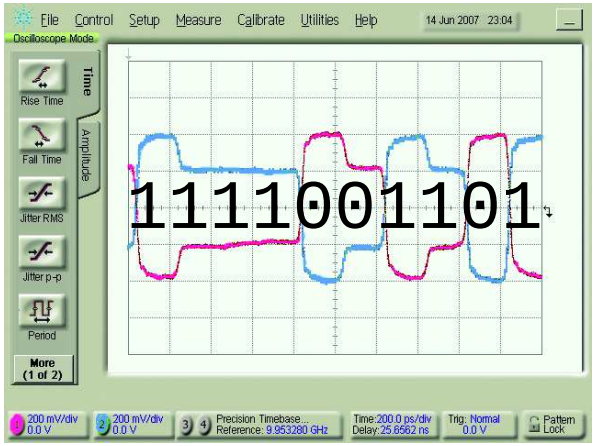


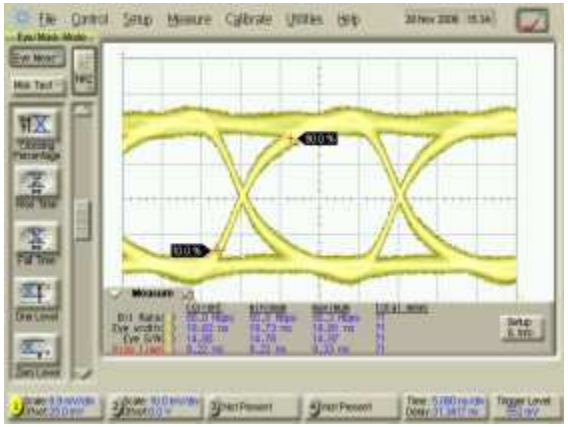
Unequalized 5Gb/s



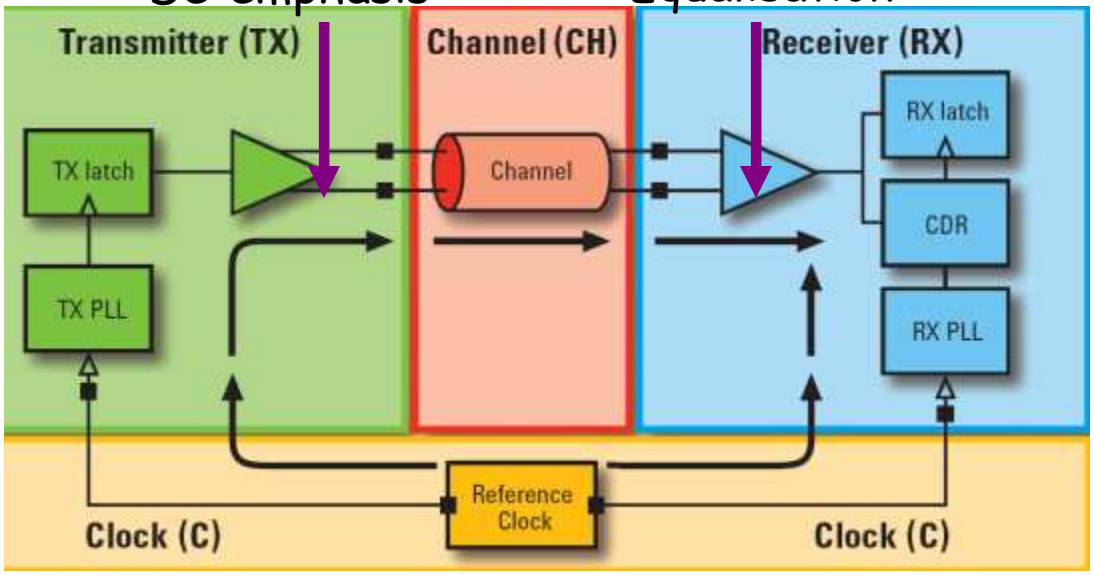
Unequalized 8Gb/s

How to clean the ‚rusty' channel





De-emphasis Equalisation



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2. ***Pre-Emphasis***
3. Equalization
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6. Practical examples
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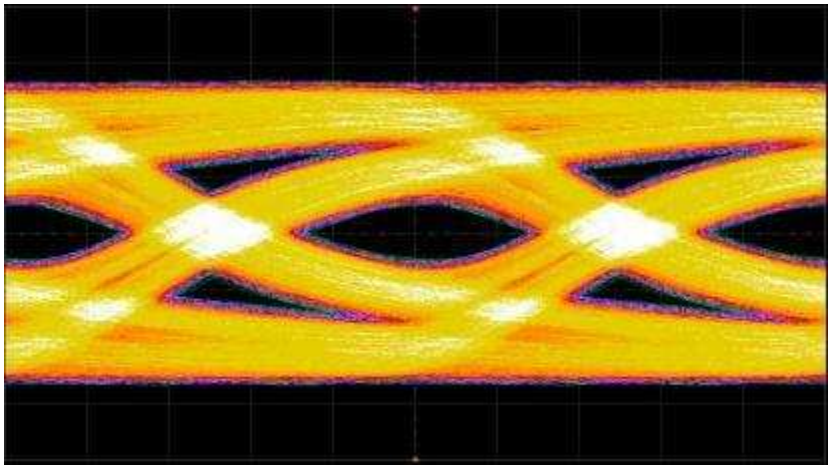
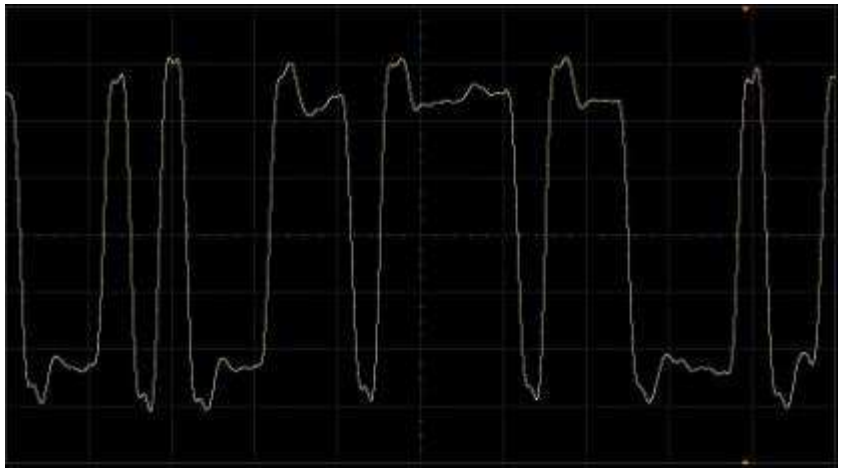
Transmitter De-emphasis

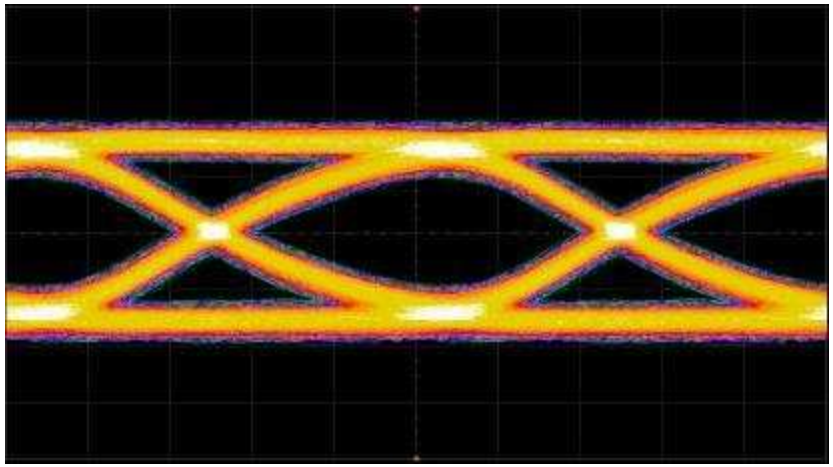
- We can account for loss through the channel at the transmitter with transmitter de-emphasis.
- De-emphasis is also called pre-emphasis.
- The amount of de-emphasis may be programmable.



De-emphasis off, measured at receiver



De-emphasis on, measured at transmitter



De-emphasis on, measured at receiver

Emphasis

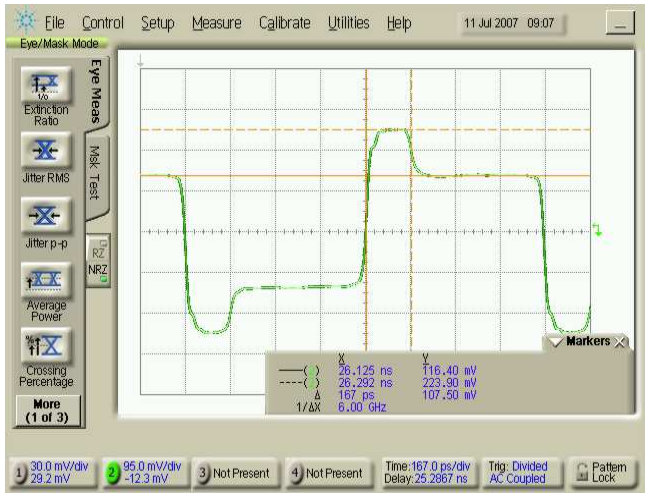
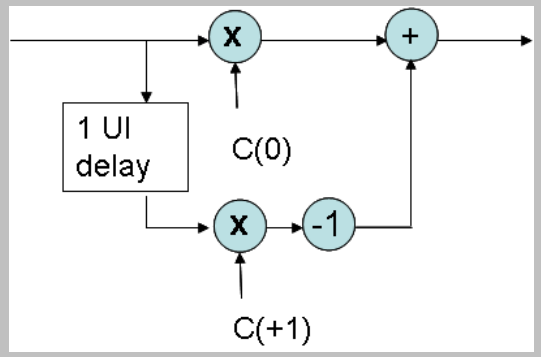


Figure above shows the waveform of a de-emphasized signal. Sometimes this is called pre-emphasis, as one could see it as boosting the first cycle after a transition. However, usually the signal's amplitude is reduced after a delay of one unit interval (UI), if the data content does not change,so the method is called de-emphasis.

Loss can be compensated for at the transmitting and the receiving end. At the transmitter the loss can be compensated either by boosting the higher frequency content ***(pre-emphasis)*** or by decreasing the low frequency content ***(de-emphasis***).

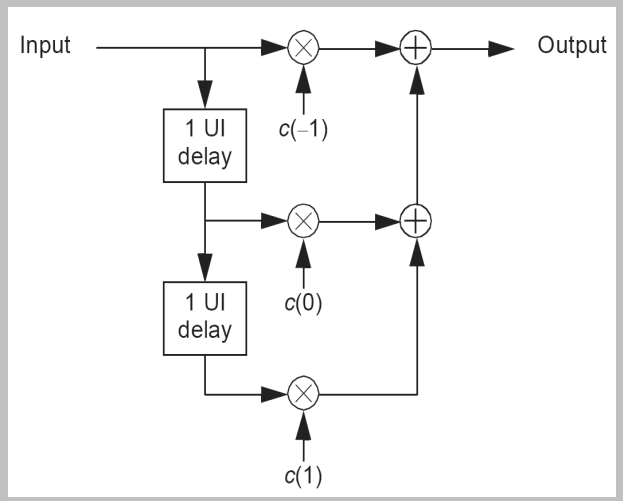
Definitions

- De-Emphasis:
- Two taps:



Computer Busses like PCIe, AMB (<= 5 Gb/s)

- Three Taps:



IEEE802.3ap 10 GbE–KR (10 Gb/s)

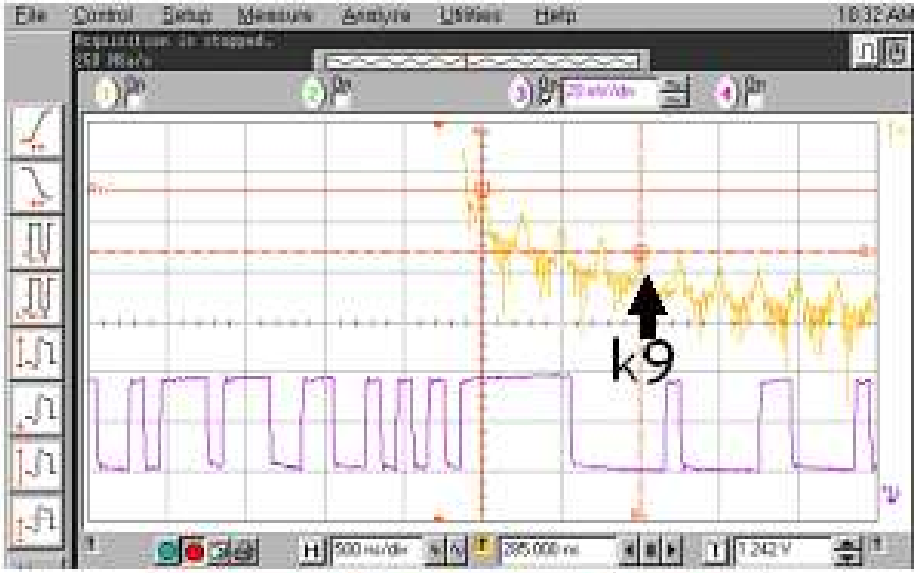
Example De-Emphasis on a digital signal in the frequency domain

Source http://cp.literature.agilent.com/litweb/pdf/989-7193EN.pdf

Channel Input signal

+ .7 dB de-emphasis on the 9th harmonic k9

Channel Output signal



In order to compensate for 6.2 dB attenuation of k9 by the channel

Example No Emphasis

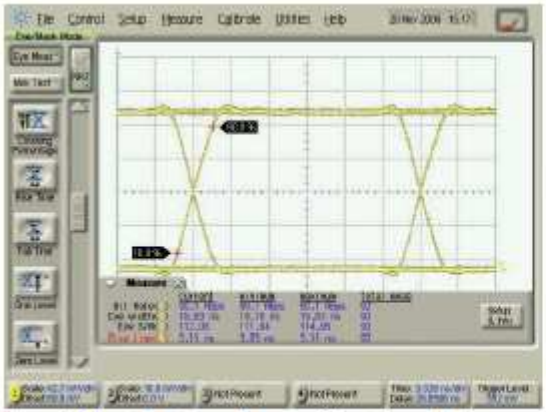


Figure 11: Input signal eye diagram, without de-emphasis

Channel Input signal

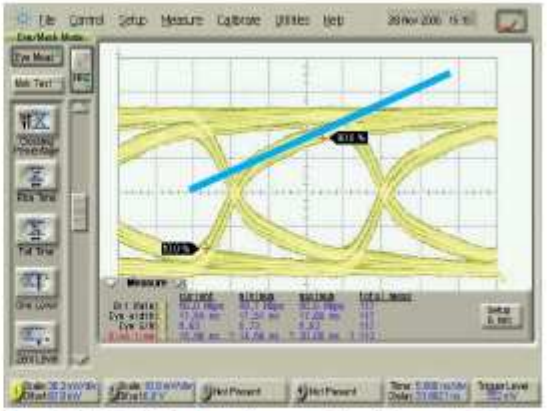


Figure 13: Output signal eye diagram, without de-emphasis

Channel Output signal

Figure 12: Input signal without de-emphasis, FFT mode measurement

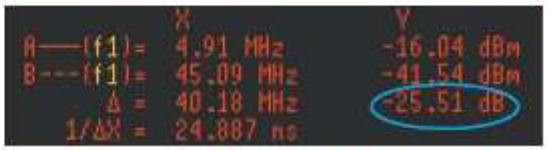


Figure 14: Output signal without de-emphasis, FFT mode measurement

Example De-Emphasis

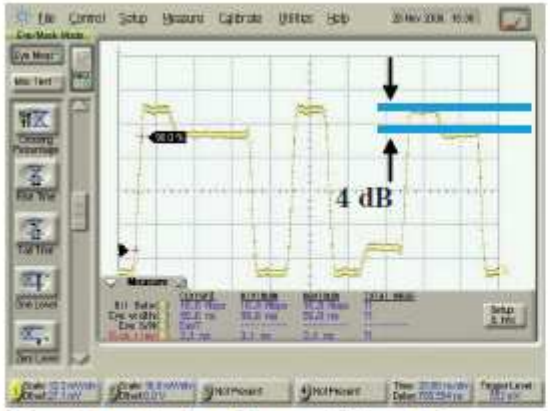


Figure 15: Input signal eye diagram, with de-emphasis

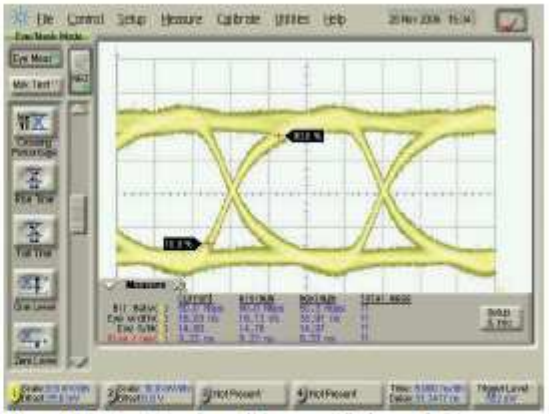
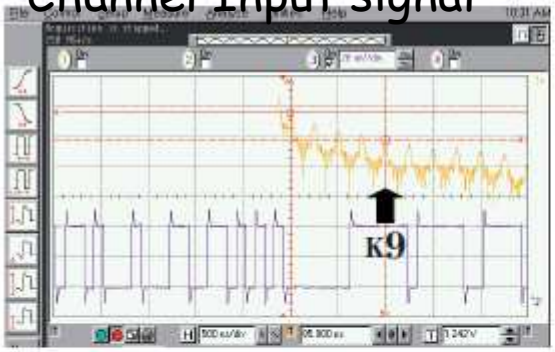


Figure 17: Output signal eye diagram, with de-emphasis

Channel Input signal



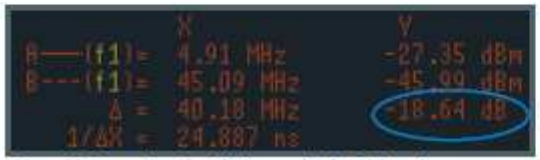
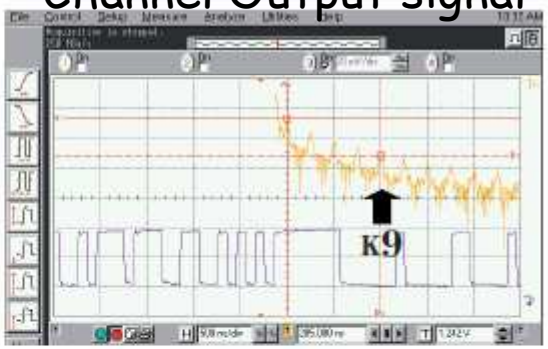


Figure 16: Input signal with de-emphasis, FFT mode measurement

Channel Output signal



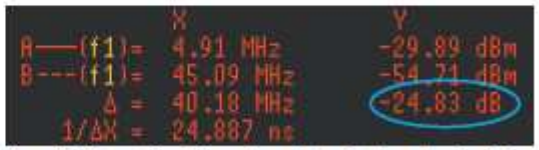
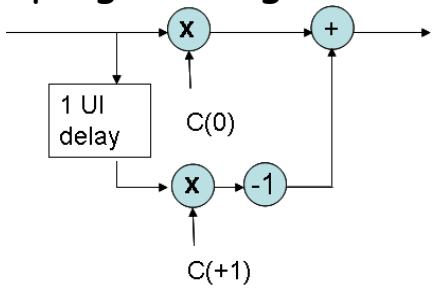


Figure 18: Output signal from the cable with de-emphasis, FFT mode measurement

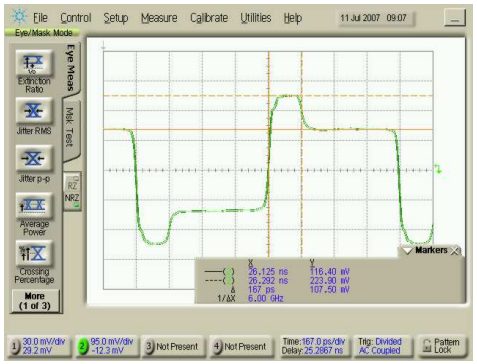
Source: appnote on emphasis http://cp.literature.agilent.com/litweb/pdf/989-7193EN.pdf

De-Emphasis with N4916A
(De-Emphasis Signal Converter)

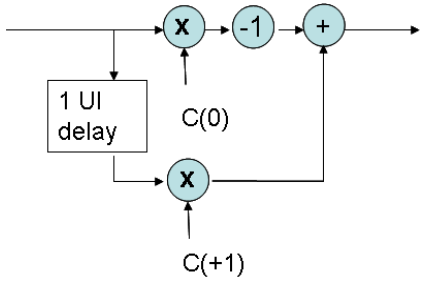
Positive de-emphasis programming



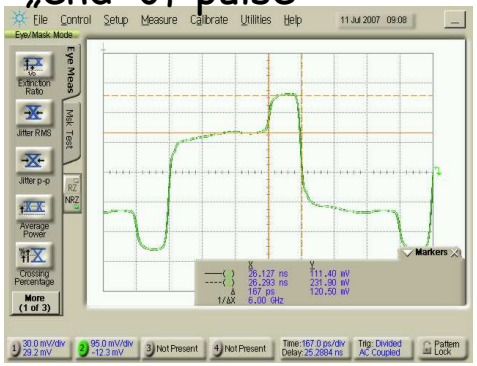
„start of pulse"



Negative de-emphasis programming



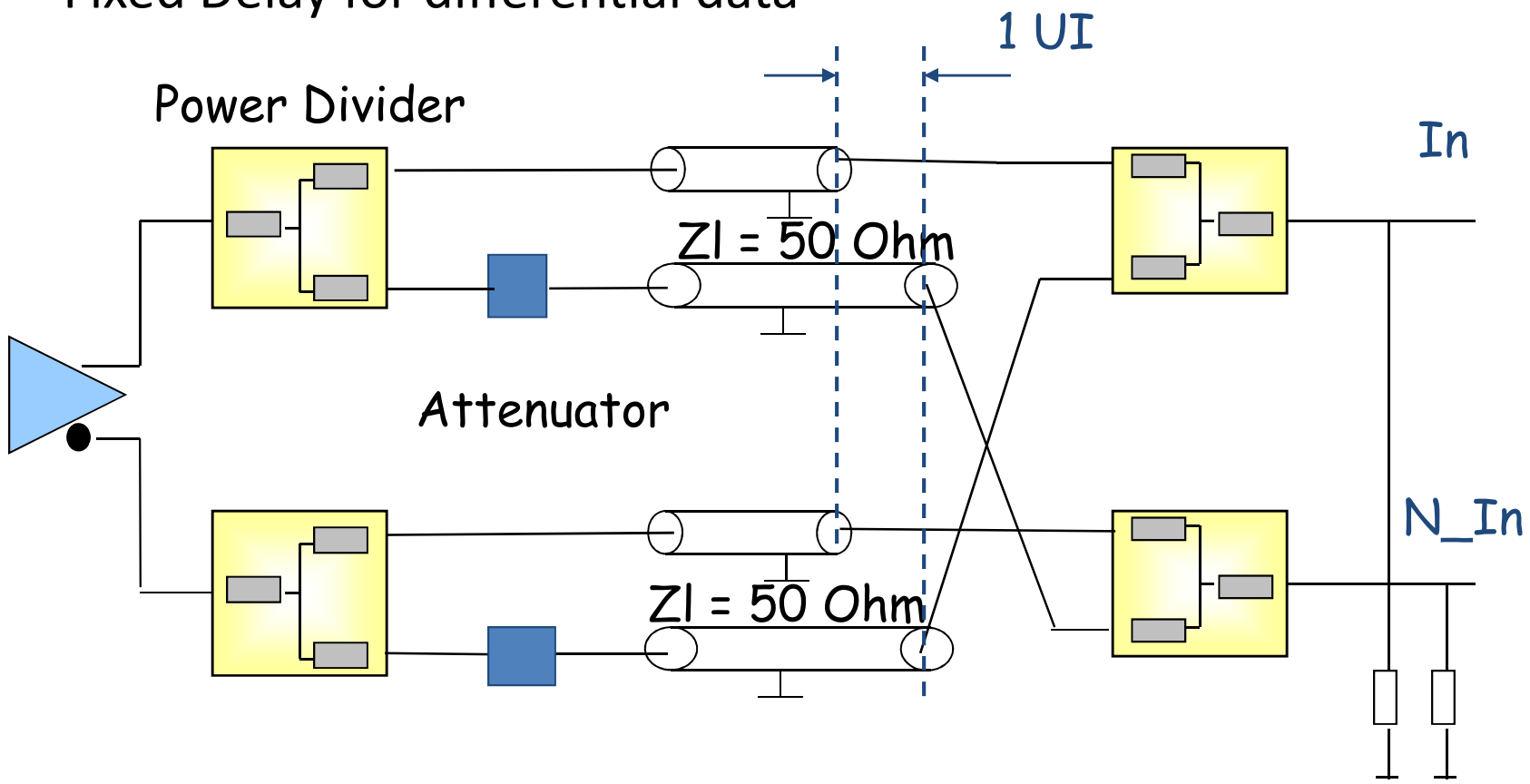
„end of pulse"



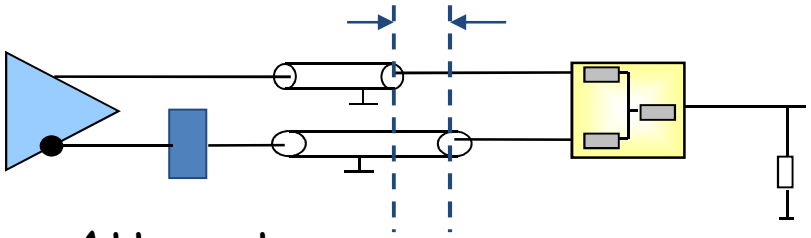
Note:
de-emphasis is sometimes called also pre-emphasis.
Used in standards: PCI Express 1 and 2, SATA 3G b/s, fully buffered DIMM, Hypertransport, CEI 6/11G, 10 Gb Ethernet.

Alternative De-emphasis solutions

- Fixed Delay for differential data



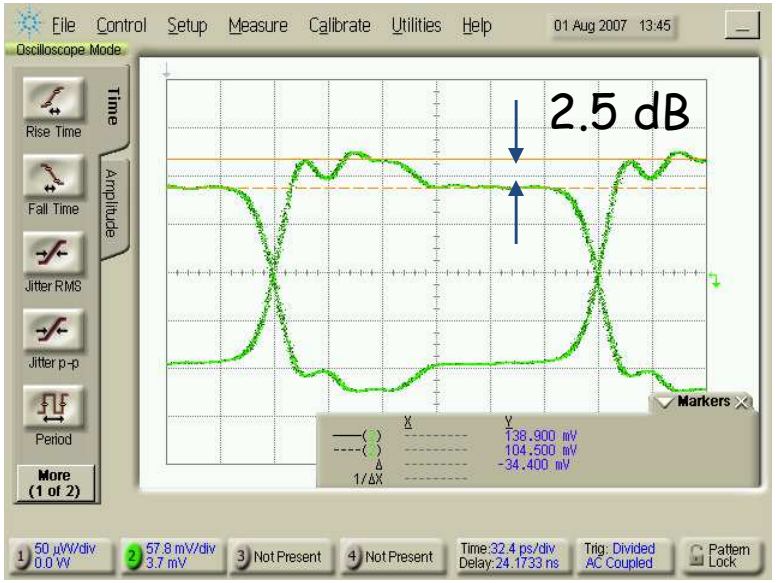
Alternative De-emphasis solutions



Attenuator

Attenuator	De-emphasis
10 dB	5 dB
12 dB	3.5 dB
15 dB	2.5 dB
20 dB	1.2 dB

De-emphasis



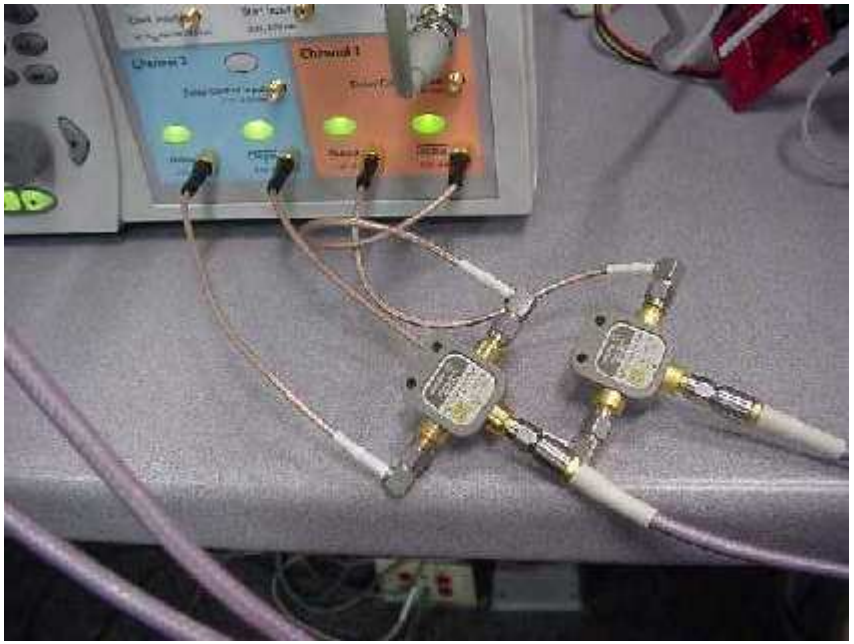
10.3 Gb/s, 1100 pattern

Alternative De-emphasis solutions: 81134A

Use a power divider (Agilent 11636B) to physically combine channel 1 and channel 2

On channel 1 program the voltage levels to achieve voltage levels in the “middle” of the pre- and de-emphasis ·

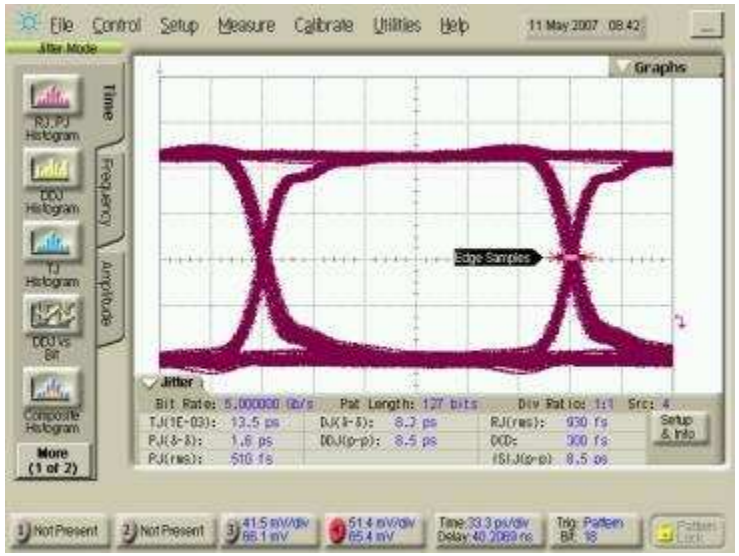
With channel 2 the de-emphasis is realized: Program the levels without any DC offset and generate the pre- or de-emphasis.

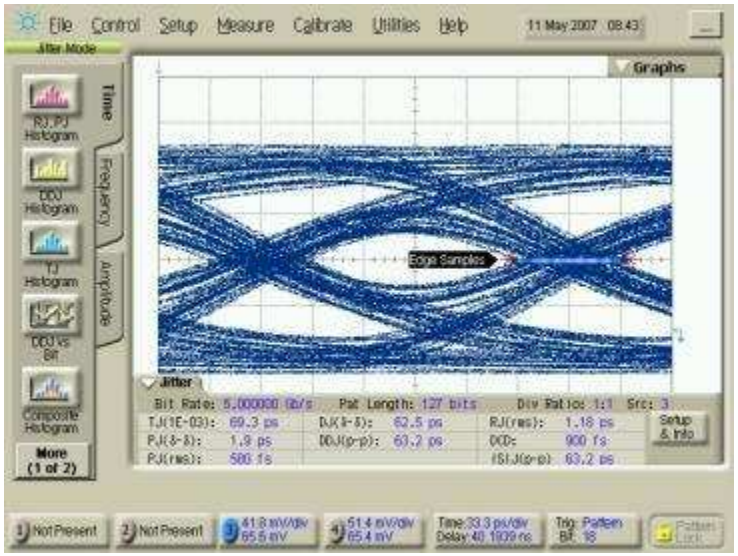


Example Backplane @ 5 Gb/s

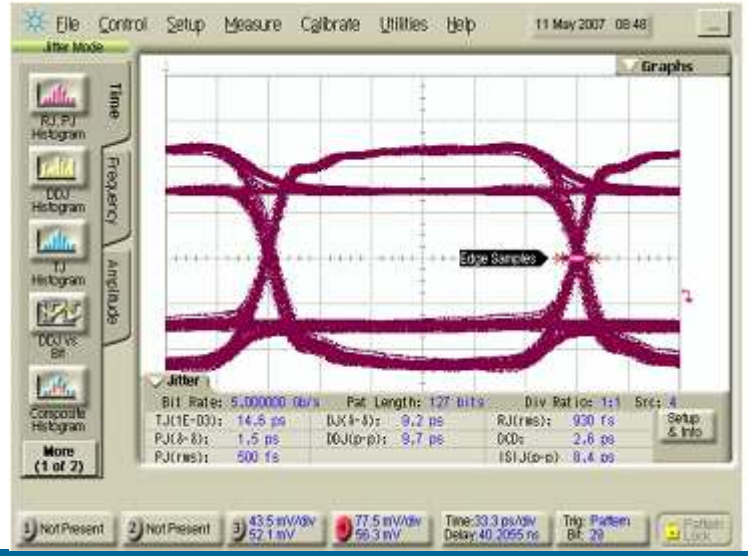
in

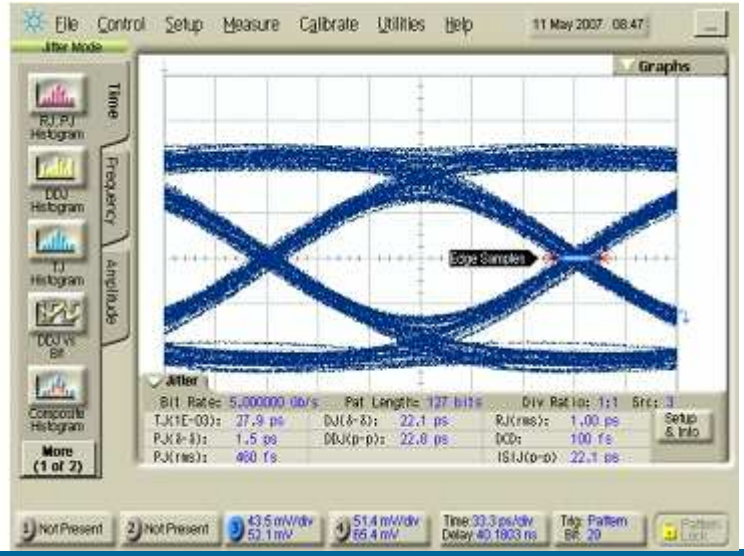
out





no de-emphasis



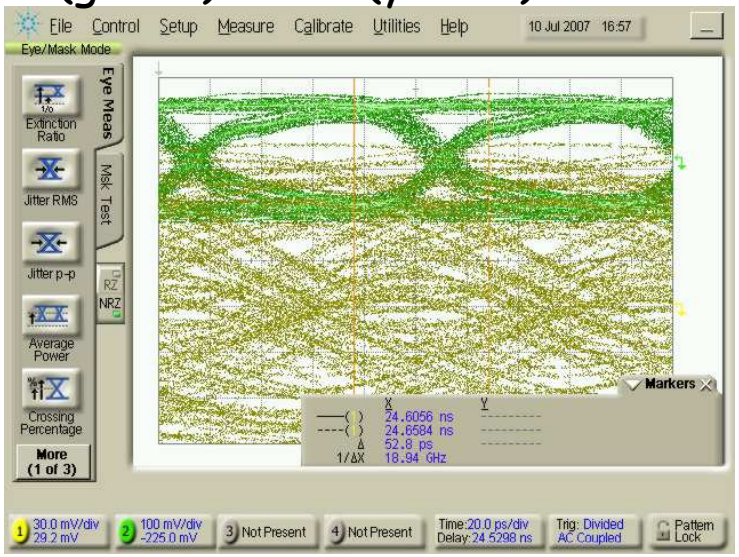


optimized de-emphasis With N4916A

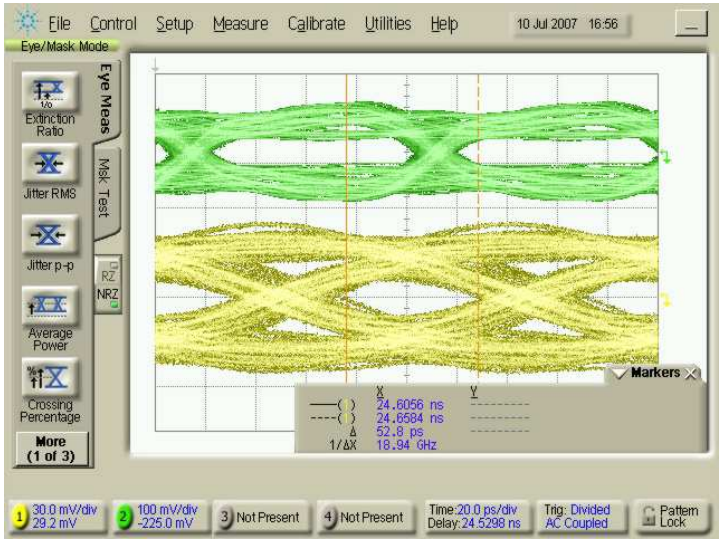
Example Motherboard @ 10 Gb/s

in (green) & out (yellow)

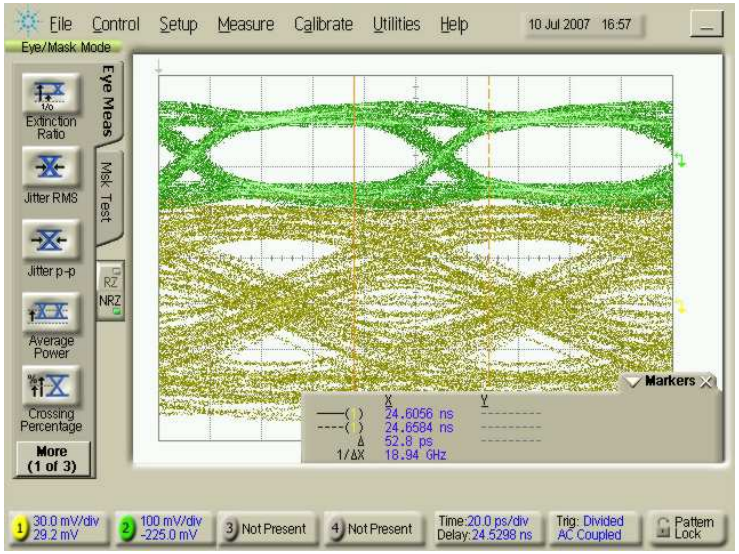
no de-emphasis



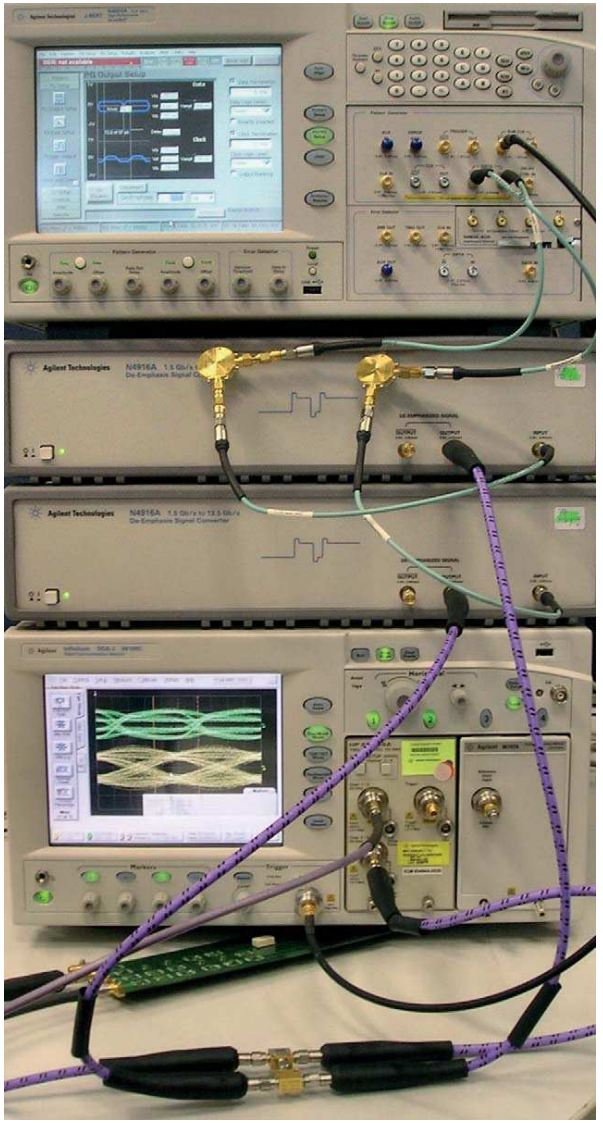
optimized de-emphasis (three taps)



maximum de-emphasis (two taps)



3 taps Emphasis with N4916A J-bert

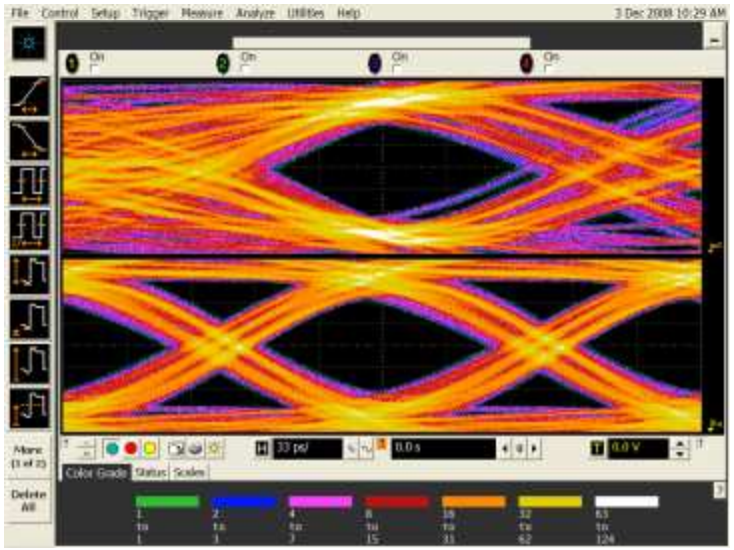


Agenda

1. Introduction
2. Eye Masks & TDR with an Network Analyzer
3. Pre-Emphasis
4. *Equalization*
5. Virtual probing / De-Embedding
6. Probing Hardware
7. Practical examples (see next page)
8. Summary

Equalization:

Serial Data Equalization N5461A



The Serial Data Equalization software is innovative software for the 90000 Series that allows for real time equalization of partially or completely closed eyes.

Serial Data Equalization provides the following:

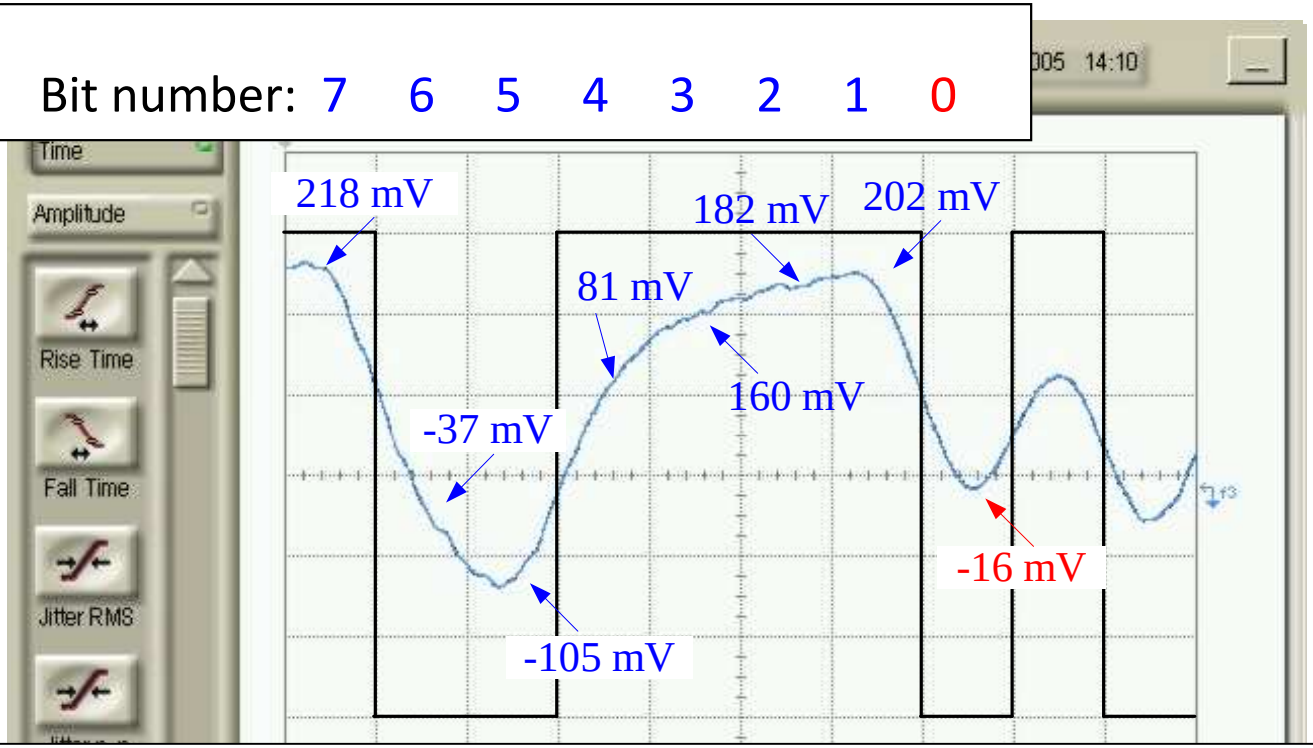
- Modeling of both DFE and FFE
- Automated tap value creation
- Basic de-embedding capability
- Full integration with the 90000 Series software
- Real time updating
- Equalization wizard
- Full cursor control to measure eye height

The idea behind equalization is to use the voltage levels of the other bits to correct the voltage level of the current bit.

FFE Concept – an Example

"Tap" the "pre-cursors" to "equalize" the bit

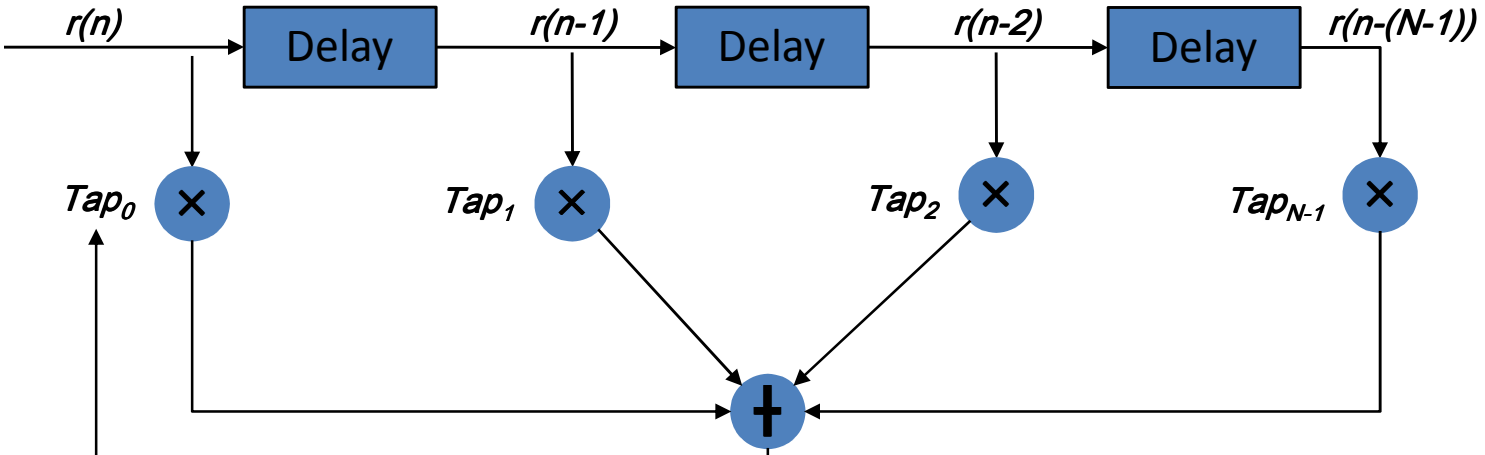
Bit number: 7 6 5 4 3 2 1 0



Equalized signal, $e(0) = -16k_0 + 202k_1 + 182k_2 + 160k_3 + 81k_4 - 105k_5 - 37k_6 + 218k_7$

- k_i are correction constants called "Taps"
- The bits before the bit of interest are called "pre-cursors"
- The bits after the bit of interest are called "post-cursors"

Feed-Forward Equalization (FFE)

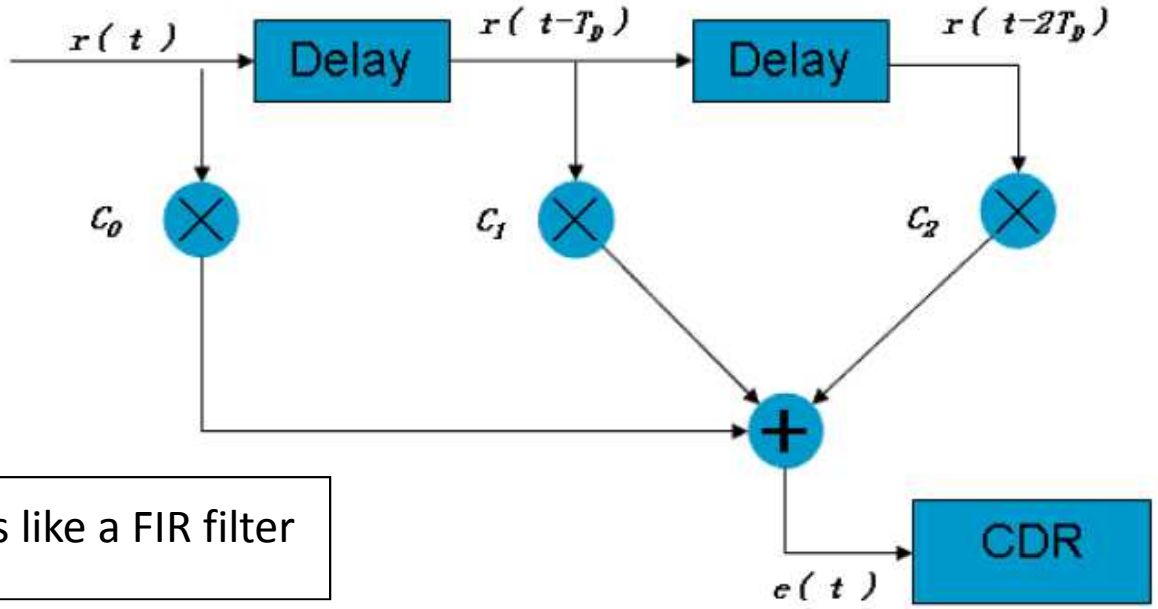


Tap values are dimensionless; they are a ratio of the voltage the receiver should have seen to what it does see. Tap_0 is applied to the current bit.

$f(k) = Taps(k) \otimes$ LP(bw) where LP is a 4th order Bessel.

gives $e(n) = \sum_{k=0}^{N-1} (Tap_k) r(n-k)$ **or** $e(n) = \sum_{k=0}^{N-1} f(k) r(n-k)$

3 tap FFE example from N5461A manual



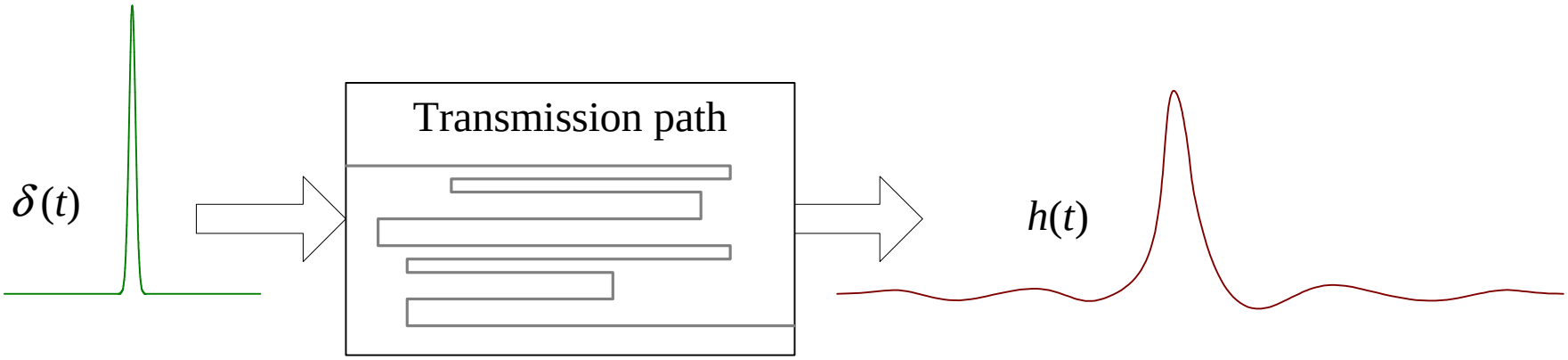
Note Gustaaf: FFE is like a FIR filter

where:

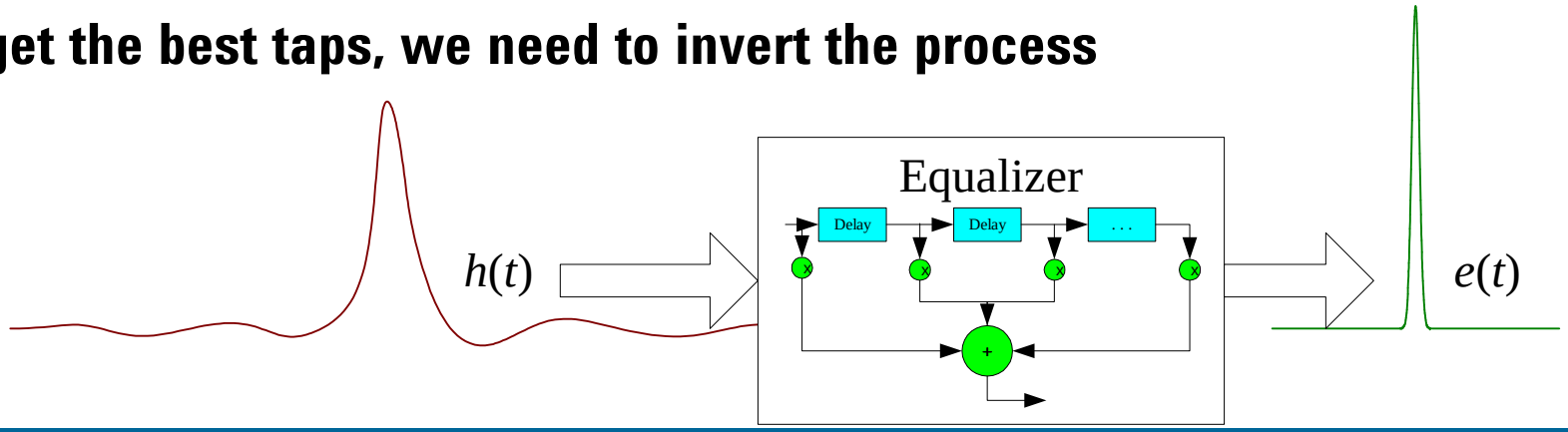
- $r(t\text{-}nT_D)$ is the input waveform n tap delays before the present time
- C_n is the n^{th} coefficient (tap)
- T_D is the tap delay
- $e(t)$ is the equalized waveform at time t
- CDR is Clock/Data Recovery

Basic Theory – Why Equalization Works

The Impulse Response $h(t)$ has all the information contained in a circuit element.



To get the best taps, we need to invert the process



Basic Theory – Why Equalization Works

ISI ⇔ Transfer Function ⇔ Ideal Taps

The impulse response is related to the transfer function through a Laplace transform $\mathcal{L}[h(t)] = G(s)$ where s is the Laplace parameter, $s = j\omega + \alpha$

The Transfer Function, $G(s)$, describes how a signal is affected by a network element

$$G(s)S(s) = R(s)$$

S = transmitted signal, R = received signal

- **ISI is contained in $G(s)$.**
- **The ideal equalizer comes from the inverse of the transfer function, $G(s)^{-1}$.**
- **Get the signal back as it was transmitted:**

$$G(s)^{-1}G(s)S(s) = G(s)^{-1}R(s) = S(s)$$

(except for random noise . . .)

Basic Theory – Why Equalization Works

ISI ⇔ Transfer Function ⇔ Ideal Taps

- **To get to the time domain take the inverse Laplace transform**

$$\mathcal{L}^{-1}[G(s)^{-1}R(s)] = g_I(t) * r(t) = s(t)$$

- **$g_I(t) * r(t)$ is the *convolution* given by**

$$g_I(t) * r(t) = \int g_I(u) * r(t-u)du$$

- **Or, for a discrete system, by**

$$g_I(n) * r(n) = \sum_{k=1}^{N} g_I(k) r(n-k)$$

... which is an LFE $e(n) = \sum_{k=0}^{N-1} f(k) r(n-k)$ **with N taps, $f(n) \sim g_I(n)$**

(note: $\mathcal{L}^{-1}[G(t)] = h(t)$ and $\mathcal{L}^{-1}[G(t)^{-1}] = g_I(t)$, but $g_I(t) \neq h(t)^{-1}$)

Basic Theory – Why Equalization Works
Ideal vs actual LFE – MFB

The step from continuous, $g_I(t)$, to discrete, $f(n)$, makes a big difference

- **The number of taps went from infinity to about 5 (which is << ∞)**

The Matched Filter Bound (MFB) is the maximum possible signal to noise ratio when an equalizer exactly cancels ISI

Let $h(i)$ be the impulse response of the channel, then

$$e(n) = \sum_{k=0}^{N-1} \sum_{i=0}^{\infty} f(k)h(i)s(n-k-i) + \sum_{k=0}^{N-1} f(k)w(n-k)$$

Imperfect ISI correction – finite $f(k)$ vs infinite $g_I(i)$

Impulse response*transmitted signal = received signal without noise

Noise term can be amplified by the equalizer

The Decision Feedback Equalizer (DFE)
Start with an LFE and . . . fix it!

A *perfect equalizer* would remove all ISI,
leaving just the signal and the filtered noise

$$e(n) = s(n) + \sum_{k=0}^{N-1} f(k)w(n-k)$$

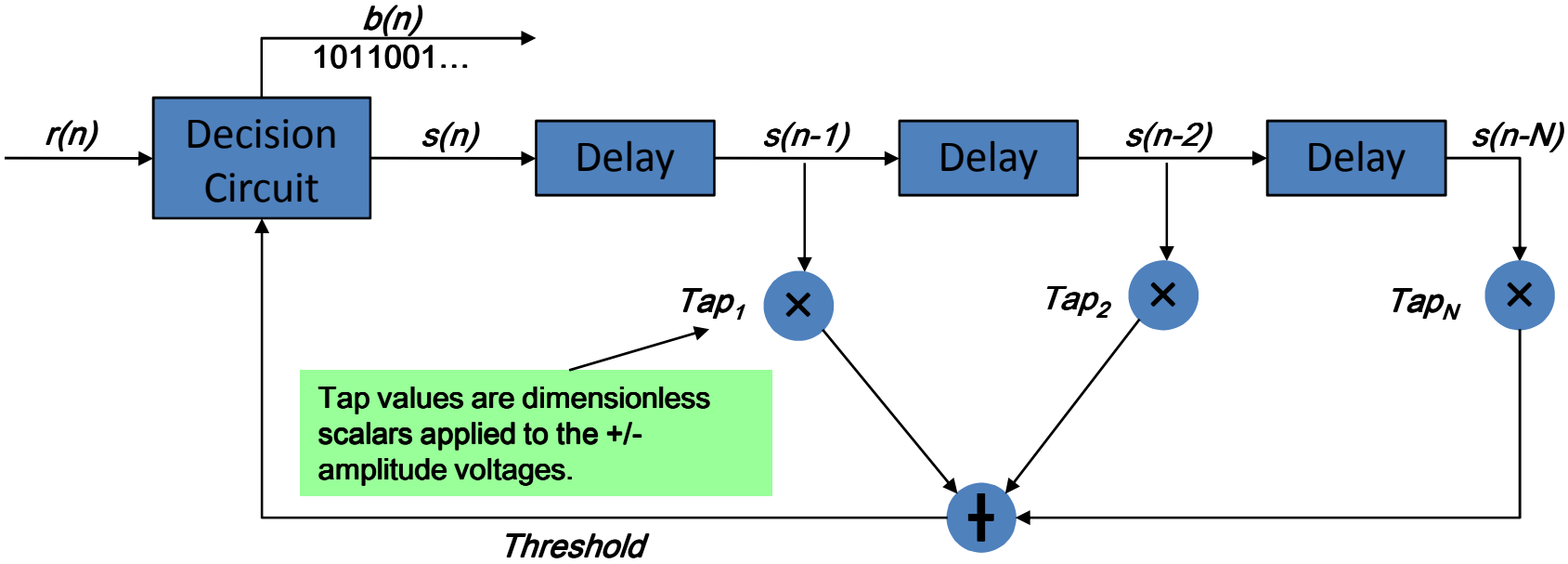
But an LFE:

1. **Is discrete – usually one tap per bit, ISI is continuous.**
2. **Is finite – not long enough to completely correct the impulse response.**
3. **Only uses information from the current and previous bits.**

→ **Introduce another correction based on the best guess of the current and previous bits – a feedback term – to cancel the rest of the ISI**

i.e., use the logic Decision to Feedback to the LFE output for better Equalization

Decision Feedback Equalization (DFE) Hardware Receiver



$$s(n) = r(n) > Threshold_{DC} \ ? \ Amplitude \ : (-Amplitude)$$

gives

$$b(n) = r(n) - \sum_{k=1}^{N} (Tap_k) s(n-k)$$

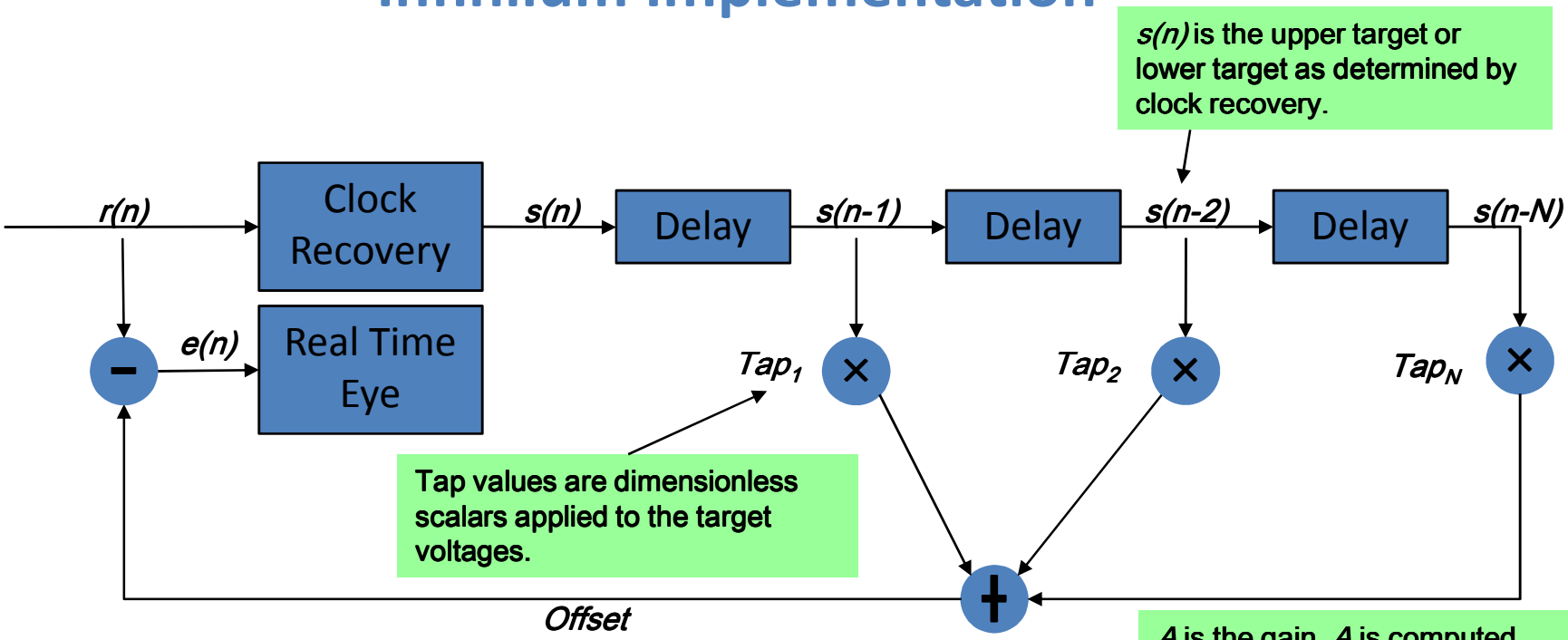
- r(n) is the signal at the receiver.
- s(n) is the +/- amplitude as determined by comparing the incoming signal is the given Threshold.
- b(n) is the bit sequence coming out of the receiver.

Decision Feedback Equalization (DFE) Principle

DFE calculates a correction value that is added to the logical decision threshold.
This is the threshold above which the waveform is considered a logical high and below which the waveform is considered a logical low.

Therefore, DFE results in the threshold shifting up or down so new logical decisions can be made on the waveform based upon this new equalized threshold level.

Decision Feedback Equalization (DFE)
Infiniium Implementation



$$s(n) = r(n) > Threshold_m \ ? \ UpperTarget \ : (-LowerTarget)$$

A is the gain. A is computed when Normalize DC Gain is selected.

gives $e(n) = r(n) - \sum_{k=1}^{N} (Tap_k) s(n-k)$ **or** $e(n) = A\left[r(n) - \sum_{k=1}^{N} (Tap_k) s(n-k) \right]$

FFE vs DFE

- FFE implemented in hardware via analog filtering.
- All devices perform the same filtering. Fixed in hardware.
- DFE is adaptive and is performed digitally.
- FFE shapes the waveform. DFE computes a new decision threshold for every bit.
- DFE can be used in addition to LFE.

Difference Between FFE and DFE

DFE=Decision Feedback Equalization

FFE= Feed Forward Equalization

Key feature	DFE	FFE
Flexibility	DFE is adaptive and is performed digitally. The DFE system learns the tap values (tap values are dimensionless correction factors).	FFE implemented in hardware via analog filtering. All devices perform the same filtering in FFE
Cost to Implement	Expensive	Inexpensive
Possible Tap Values	**Unlimited**	**1**

The application of FFE may noise gain.

This makes the oscilloscope industry's lowest noise floor on the 90000A so important with equalization and de-embedding.

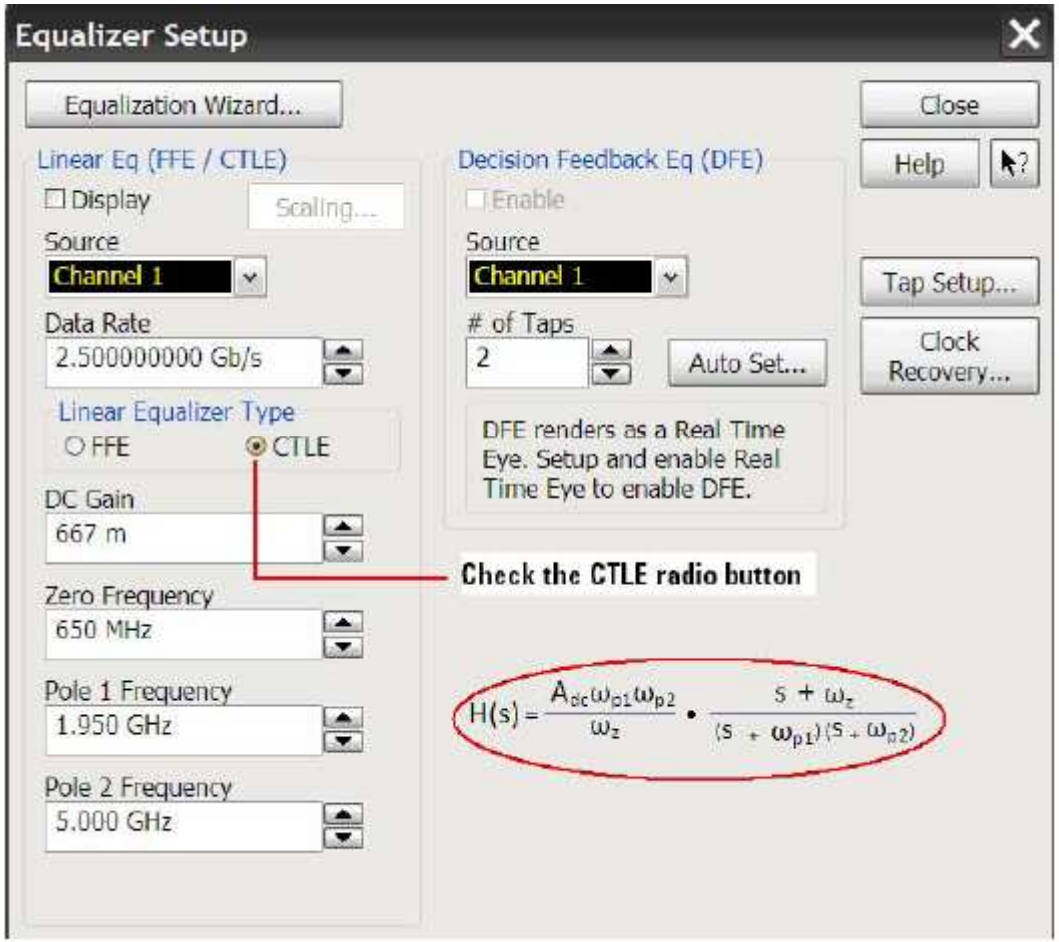
CTLE example from N5461A manual

Continuous Time Linear equalization (CTLE) is another linear equalization method.

Many of today's standards require CTLE as part of compliance testing.
When performing equalization on your Infiniium oscilloscope, you choose whether you want to use FFE or CTLE (or neither) for your linear equalization method.

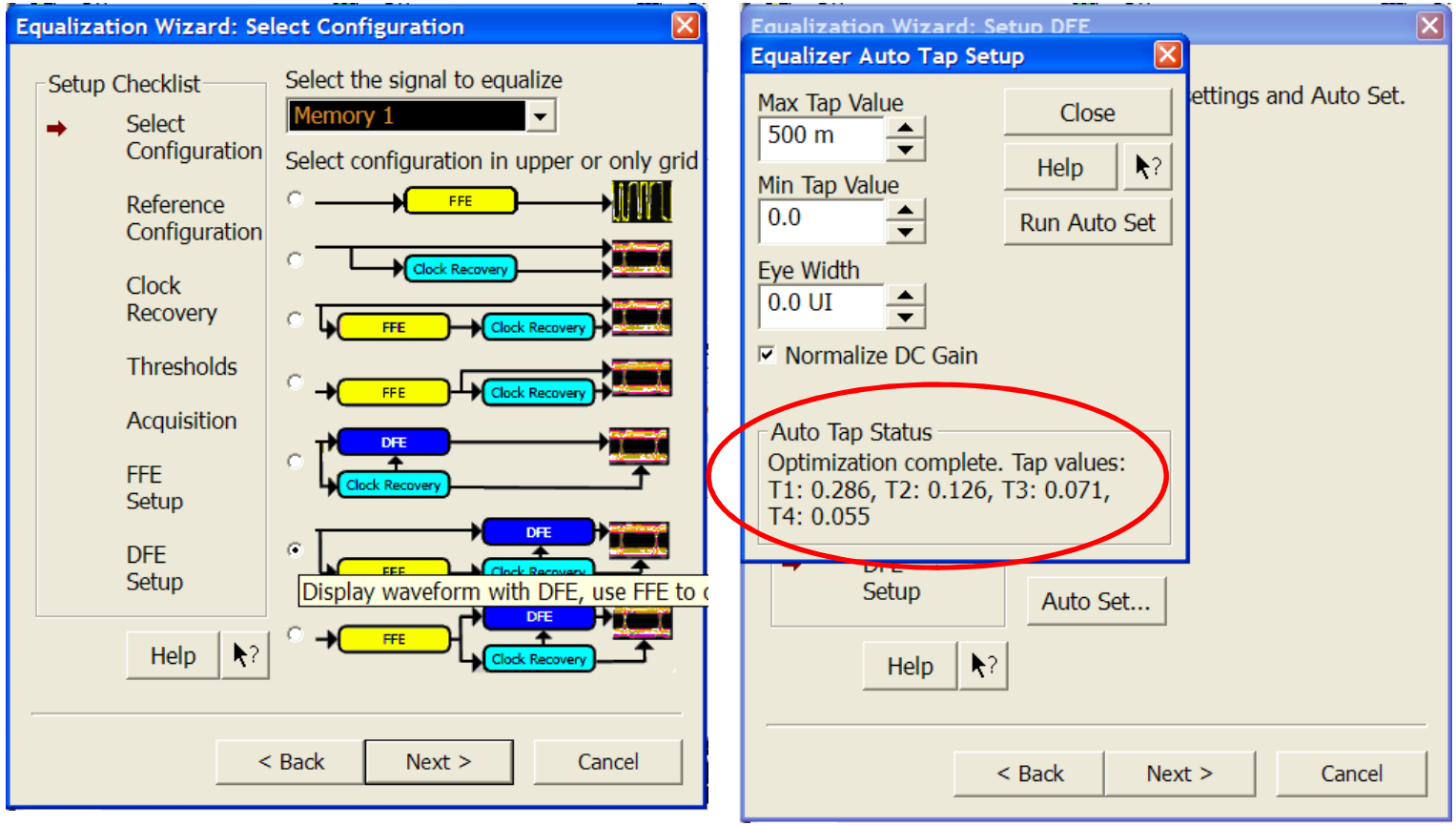
The filter applied to your signal via CTLE is described by:

$$H(s) = \frac{A_{dc}\omega_{p1}\omega_{p2}}{\omega_z} \bullet \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$



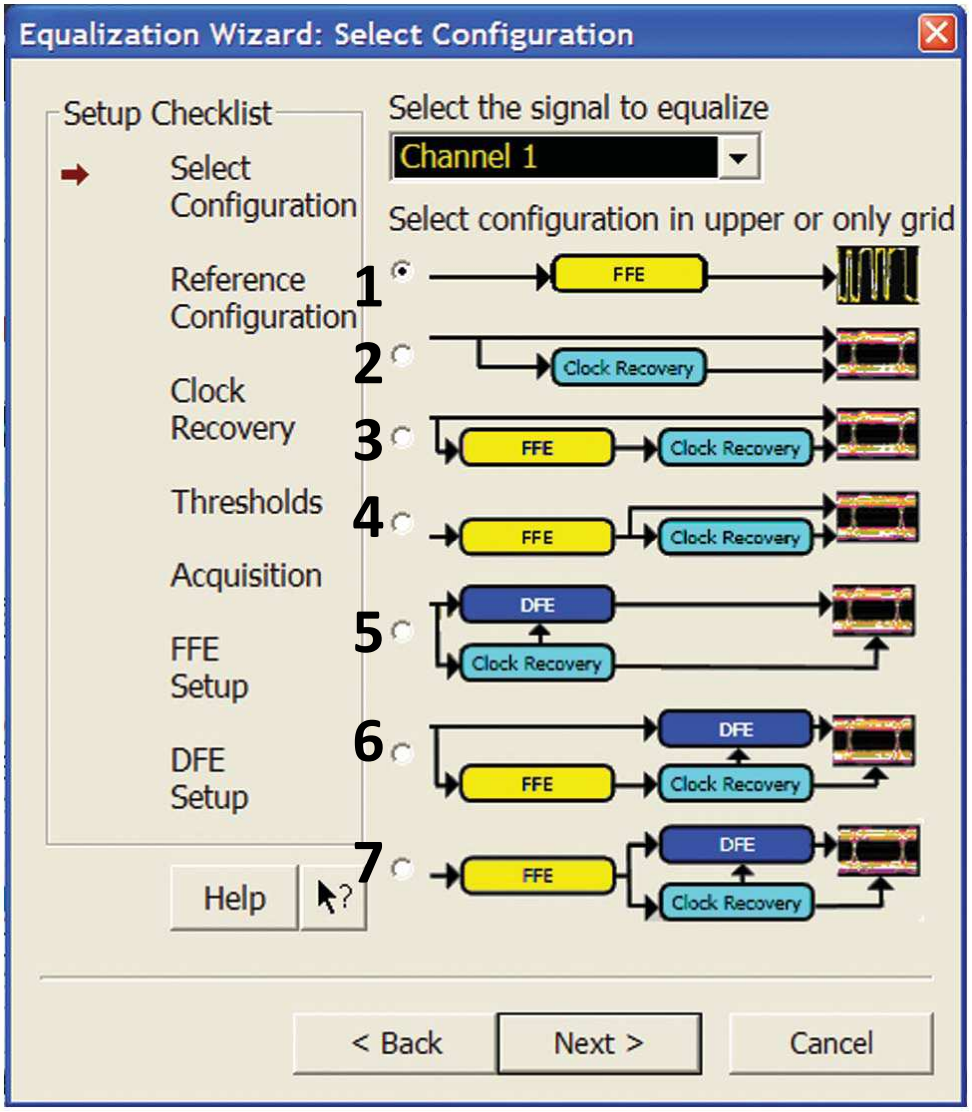
DC Gain (Adc), Zero Frequency (Wz), Pole 1 (Wp1), Pole 2 (Wp2)

Serial Data Equalization Provides a Complete Equalization Wizard and Automated Tap Values



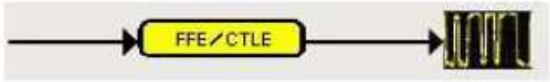
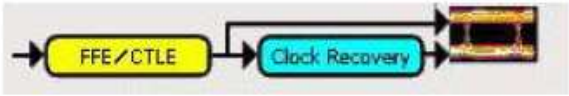
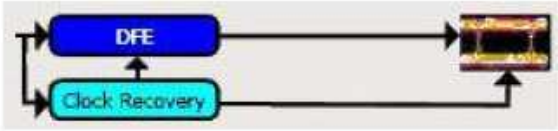
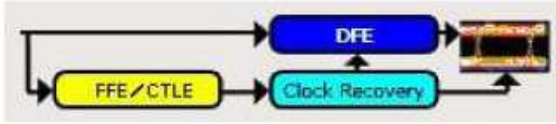
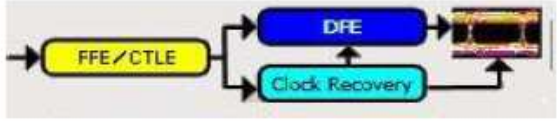
1. Wizard allows for seven real time eye options (including DFE and FFE on a closed eye)
2. Wizard provides full step by step process for clock recovery
3. Wizard provides tap value automation via the FFE and DFE setup menus
4. Wizard makes setting up equalization fast and easy

N5461A Equalization Wizard options



1. FFE is applied, but the real time eye is not displayed. You will see only the waveform.
2. No equalization applied. This is to compare an equalized signal versus a non-equalized signal.
3. FFE is applied only to recover the clock, but the referenced eye is unequalized. This is useful forfinding the recovered clock from a closed eye.
4. Standard FFE equalization.
5. Standard DFE equalization for a non closed eye.
6. Standard DFE equalization for a closed eye. Note the FFE is used to recover the clock, but is notdisplayed in the real time eye.
7. FFE is applied and then DFE is applied to the real time eye. Both are displayed in the resulting realtime eye.

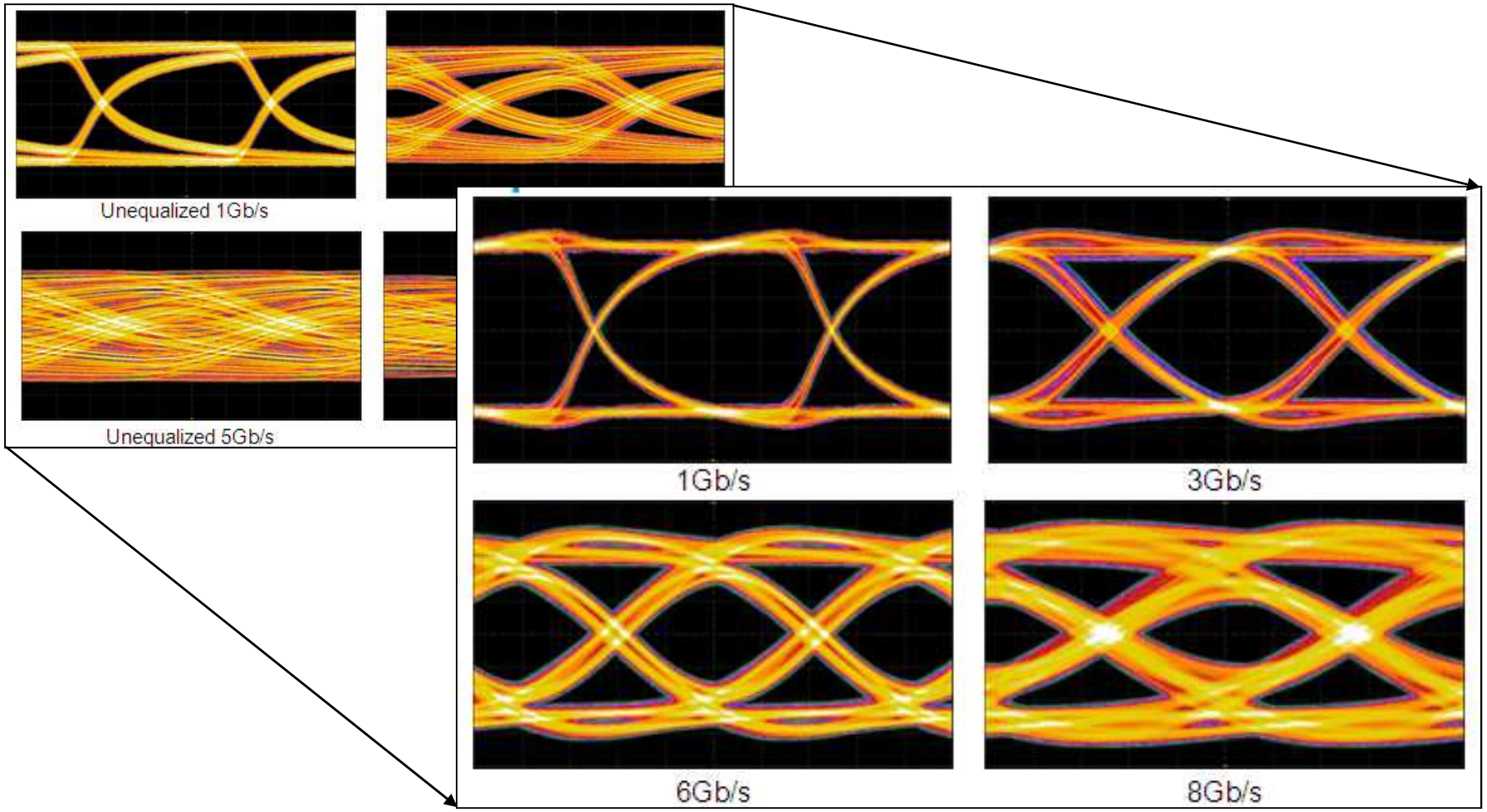
N5461A Equalization Wizard options

Image from Dialog Box	Description
	• FFE/CTLE is applied, but the real-time eye is not shown. Instead, the waveform resulting from applying FFE/CTLE is displayed.
	• No equalization is implemented and the unequalized real-time eye is displayed. This is useful if you want to have a reference to compare to. For instance, you can put the unequalized eye in the top grid and the equalized eye in the bottom grid so you can compare them on the same screen.
	• FFE/CTLE is only used to recover the clock, but the actual displayed real-time eye is unequalized. This is useful if you want to have a reference to compare to, but your unequalized eye is completely closed. You cannot recover a clock on a closed eye, so FFE/CTLE is applied to open the eye so the clock can be recovered. In other words, this options serves the same purpose as the selection immediately above it, but is used with closed eyes.
	• A FFE/CTLE eye is displayed on the oscilloscope. This is a standard FFE/CTLE implementation and can be used on partially or completely closed eyes.
	• A Decision Feedback Equalized eye is displayed on the oscilloscope. This structure cannot be used on completely closed eyes as the clock cannot be recovered with this method. If the eye is closed and you want to implement DFE, use the option immediately below this.
	• FFE/CTLE is used to recover the clock (but is not implemented in the real-time eye display) and a Decision Feedback Equalized eye is displayed on the oscilloscope. This allows you to perform DFE on completely closed eyes.
	• FFE/CTLE is applied and then DFE is applied to the real-time eye. Additionally, since FFE/CTLE is also used to recover the clock, this structure can be used on completely or partially closed eyes.

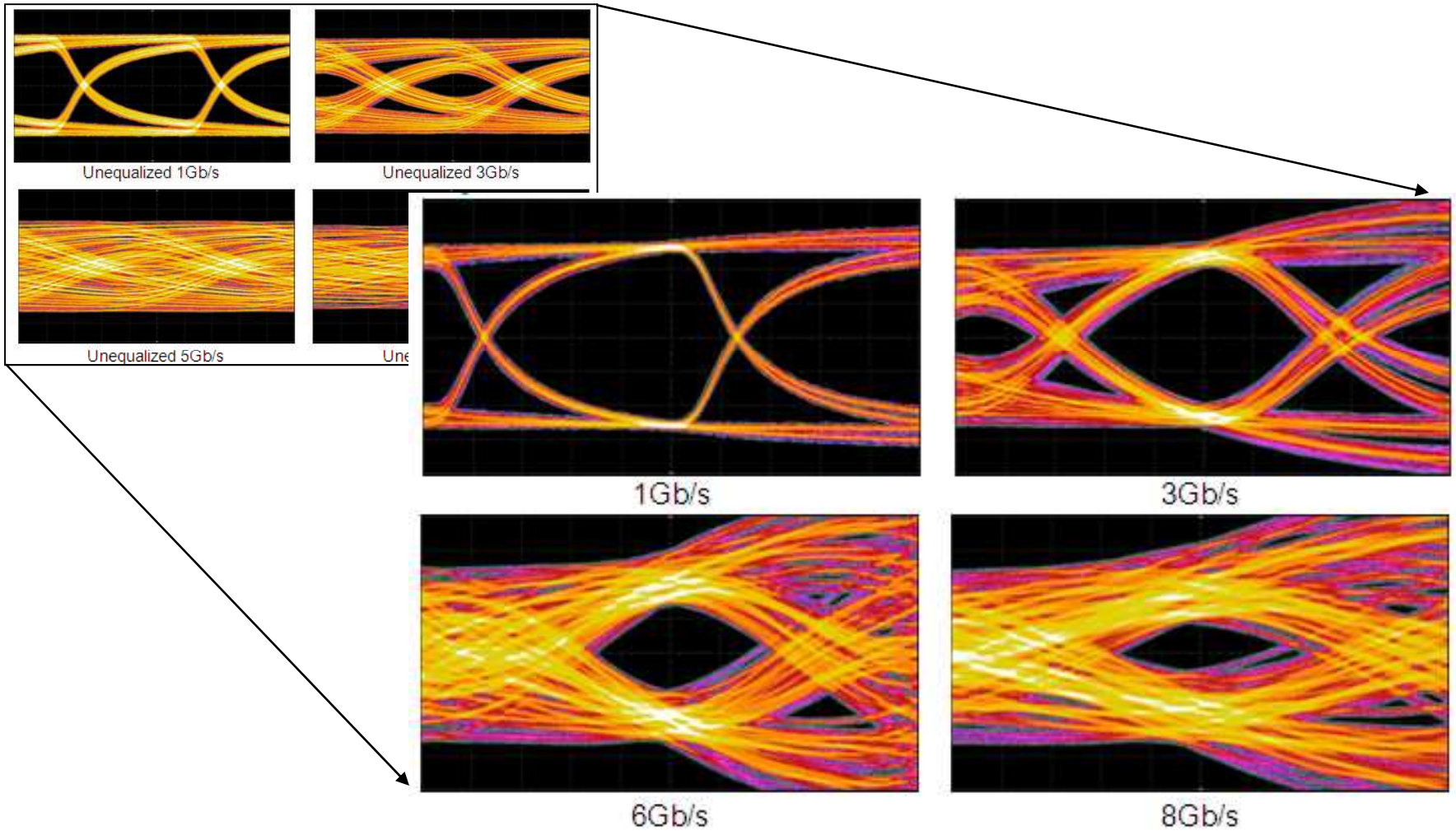
Equalizer demonstration

- 81134A as ideal source
- "Bad cable" as medium
- 90.000 scope as receiver with N5461A equalizer

FFE Results taken from the Serial Data Equalization SW



DFE Results taken from the Serial Data Equalization SW



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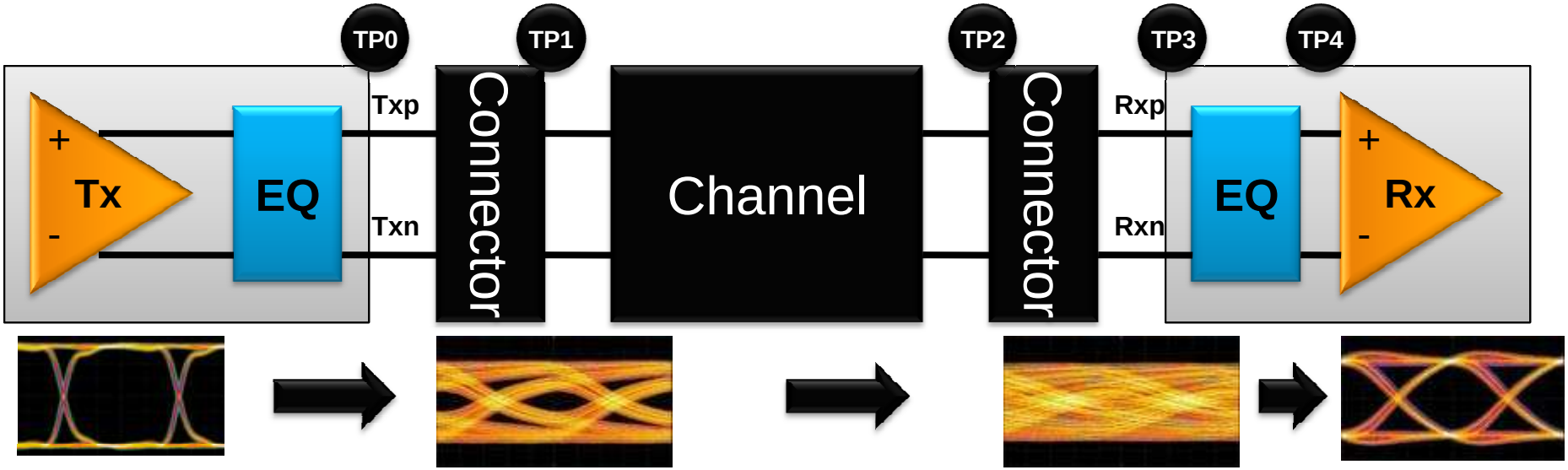
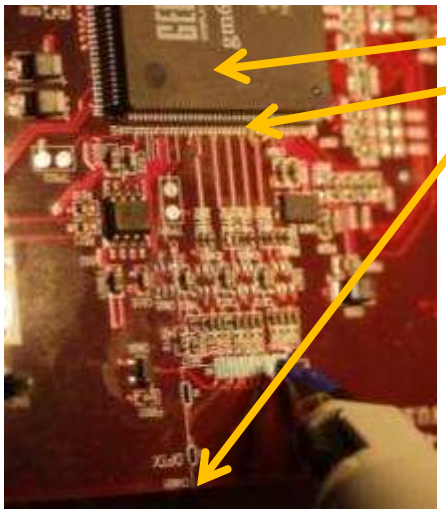
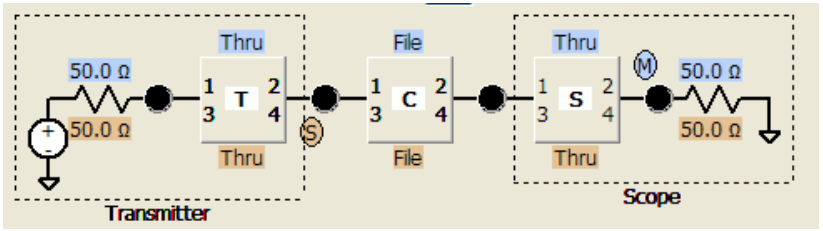
De-embedding Fixtures or PCB Traces





Signal generated here
Exits IC here
Exits board here

Combine measurements and transmission line models to view simulated scope measurements at any location in your design



Intuitive GUI speeds setup

What is Virtual probing / De-Embedding ?

De-Embedding:
‘There is something between my measurement point and where I want to measure that I have to remove.’

Embedding:
‘I want to add a cable to see what happens to the eye’

Virtual Probing:
‘I want to look anywhere in the circuit!’

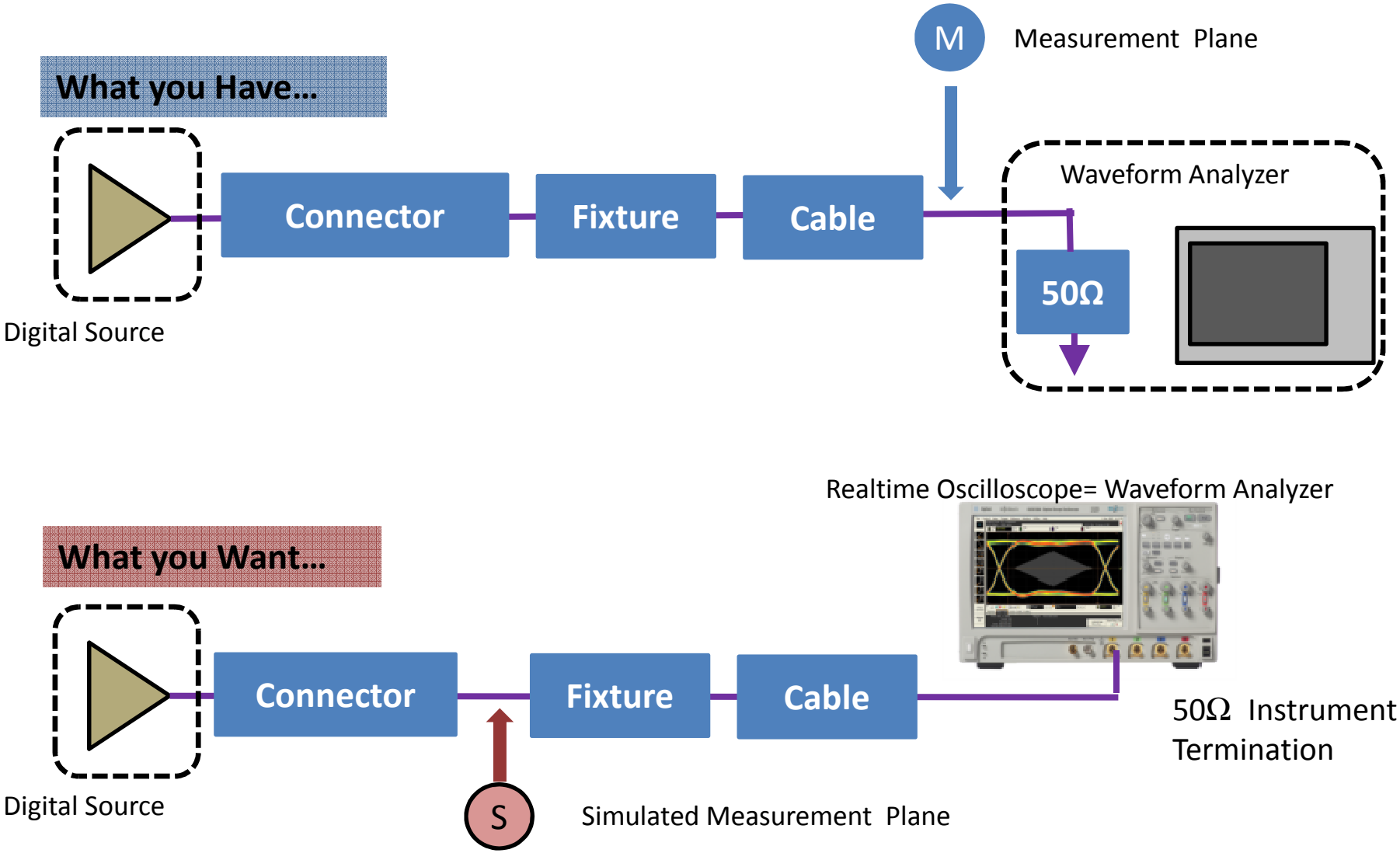
Probe Loading:
‘I want to remove any loading effects of the probe’

Accuracy:
‘I want the lowest uncertainties.’

Why Virtual probing on Infiniium Scopes?

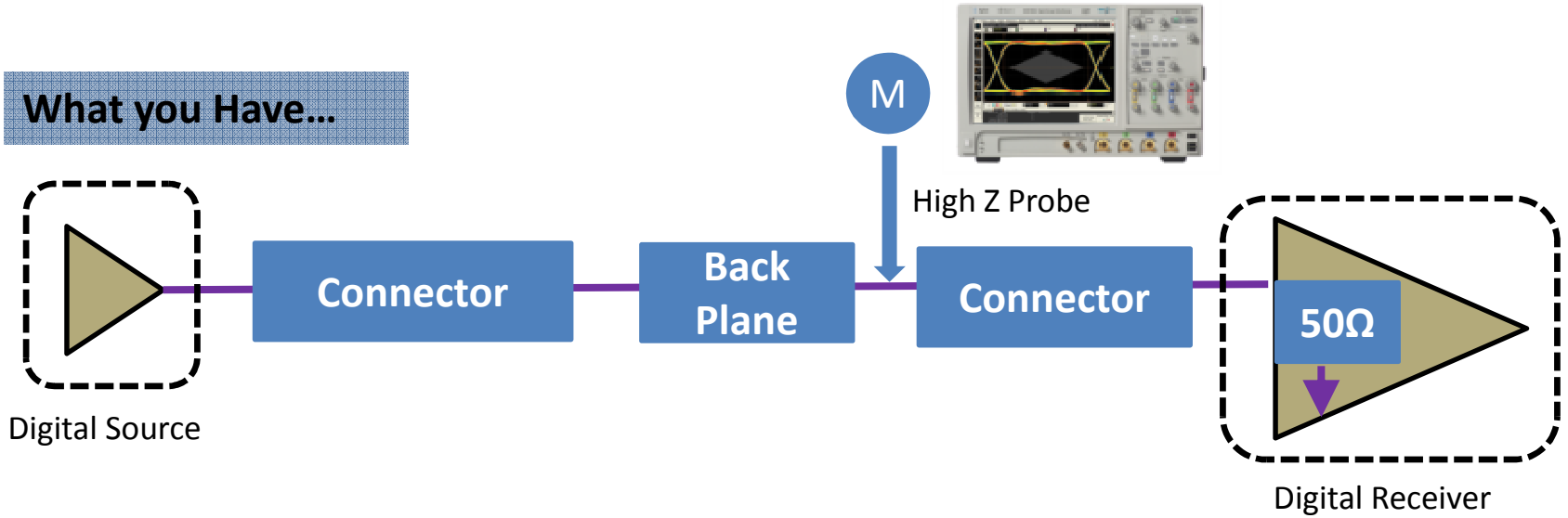
Agilent Technologies

Virtual Probing = Measurement Plane Relocation

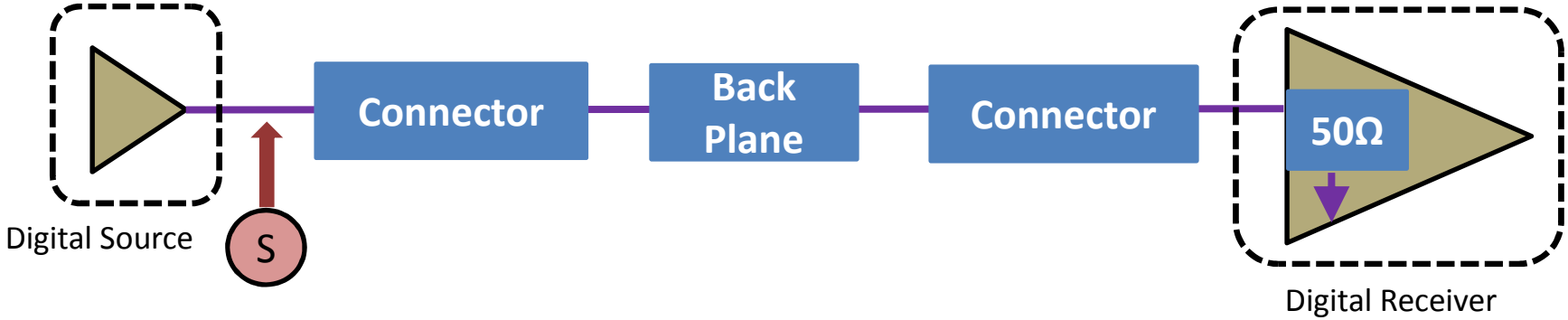


Virtual Probing (or Measurement Plane Relocation)

What you Have…



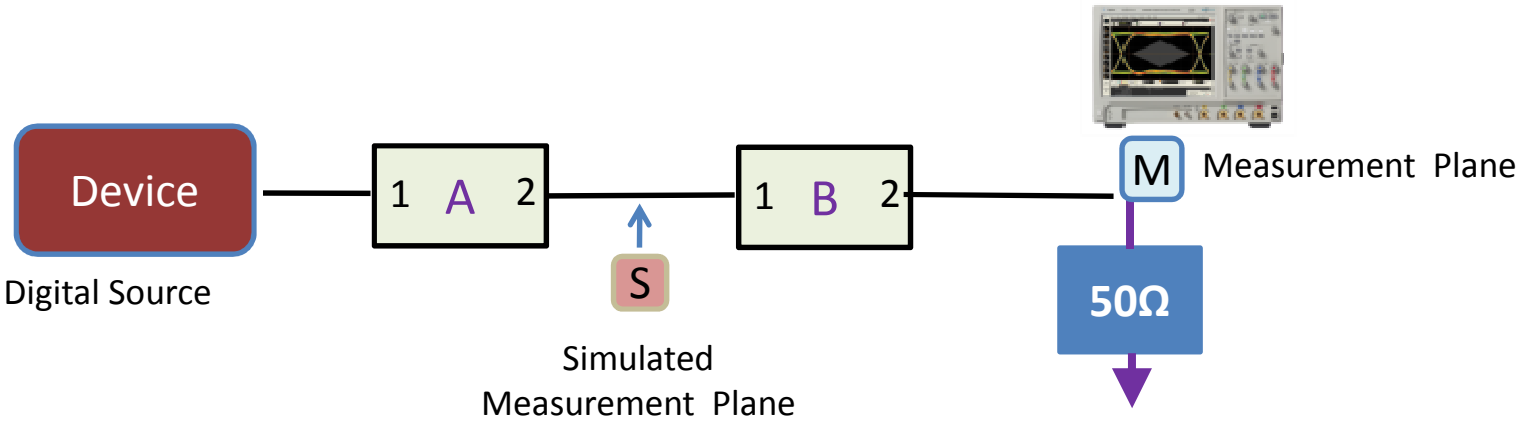
What you Want…



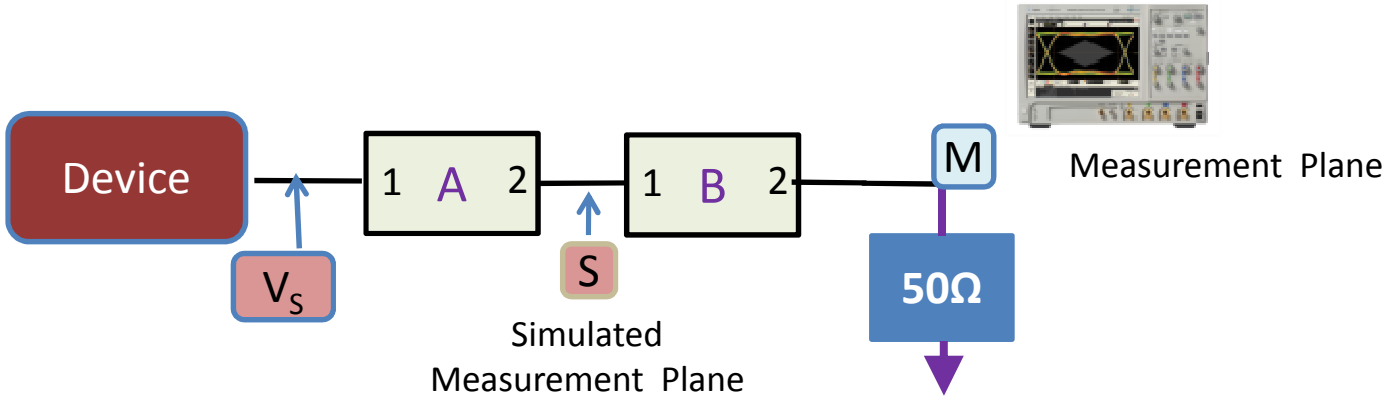
Transfer Functions

If you want to see signal at S but can only measure at M, what do you do?

- A Transfer Function describes the ratio of a voltage wave entering/exiting one port to a voltage wave exiting/entering another port.
- An S-Parameter or combination of S-Parameters can be used as a Transfer Function.
- Transfer Functions are commonly described in the frequency domain H(s), where s=jw



Transfer Functions, continued



M * H (s) = S

$$M(k) * H(n-k) = S(n)$$

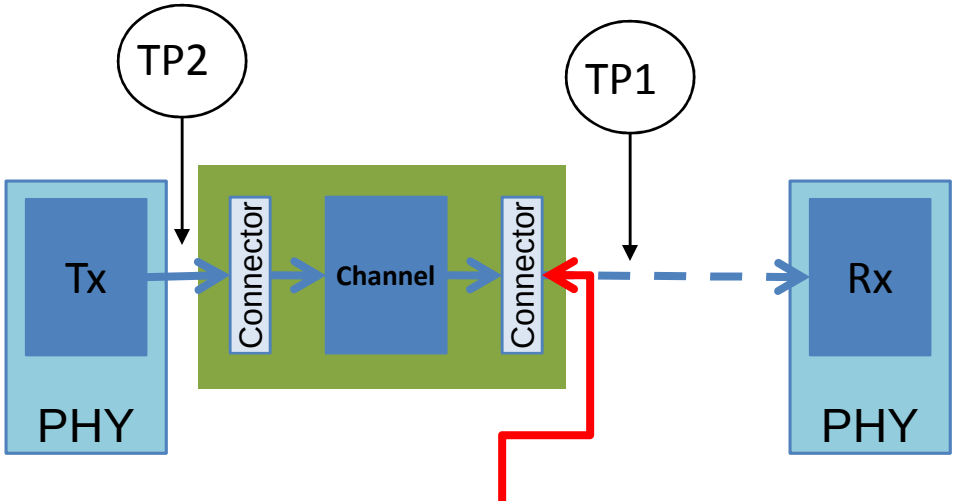
Acquisition Data

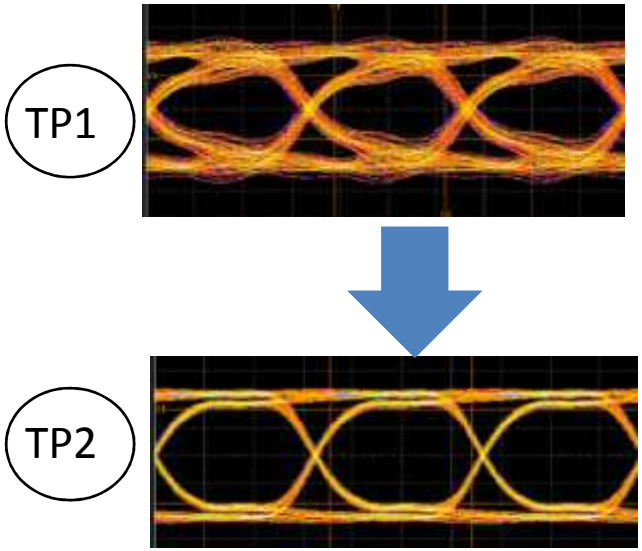
Simulated Measurement

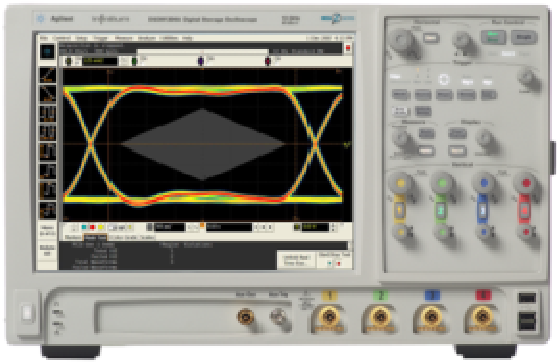
Discrete Time Representation
of Transfer Function

Removing a Channel Element – De-Embedding

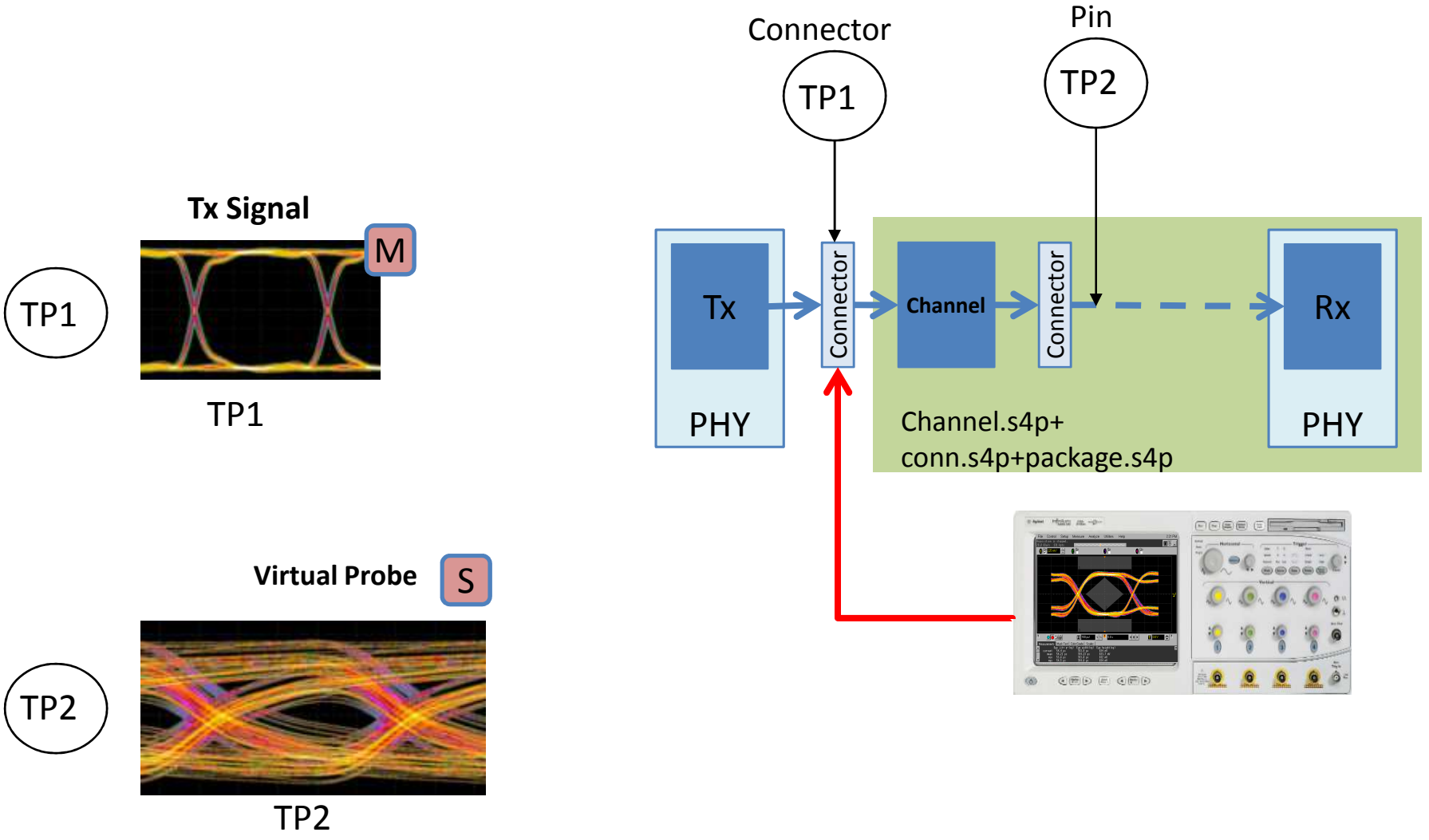
- Compensate for Probing and Fixture Loss – Add Margin to Transmitter Characterization
- PCI Express 2, SATA, and Custom
- Compliance Requirement for Gen 2





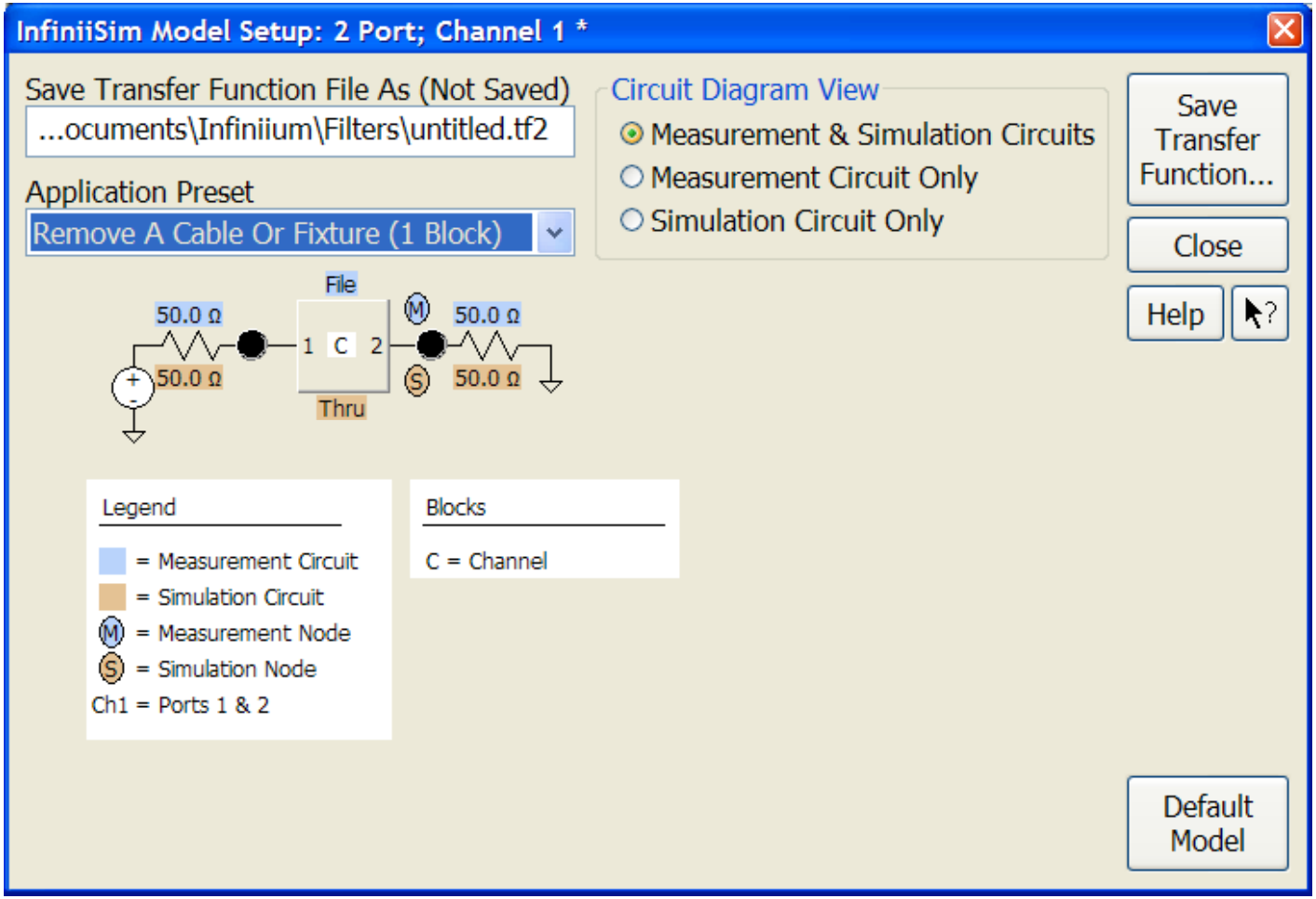


Inserting a Channel Element - Embedding



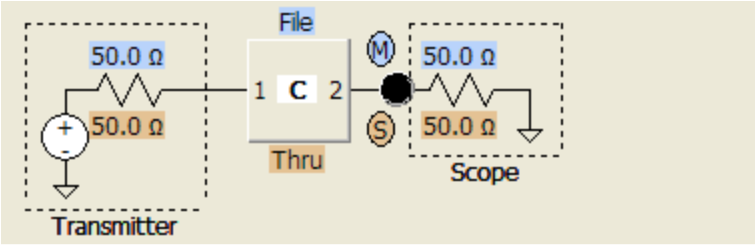
Agilent De-Embedding Representation: InfiniiSim

Example Remove Insertion Loss of 1 Channel Element

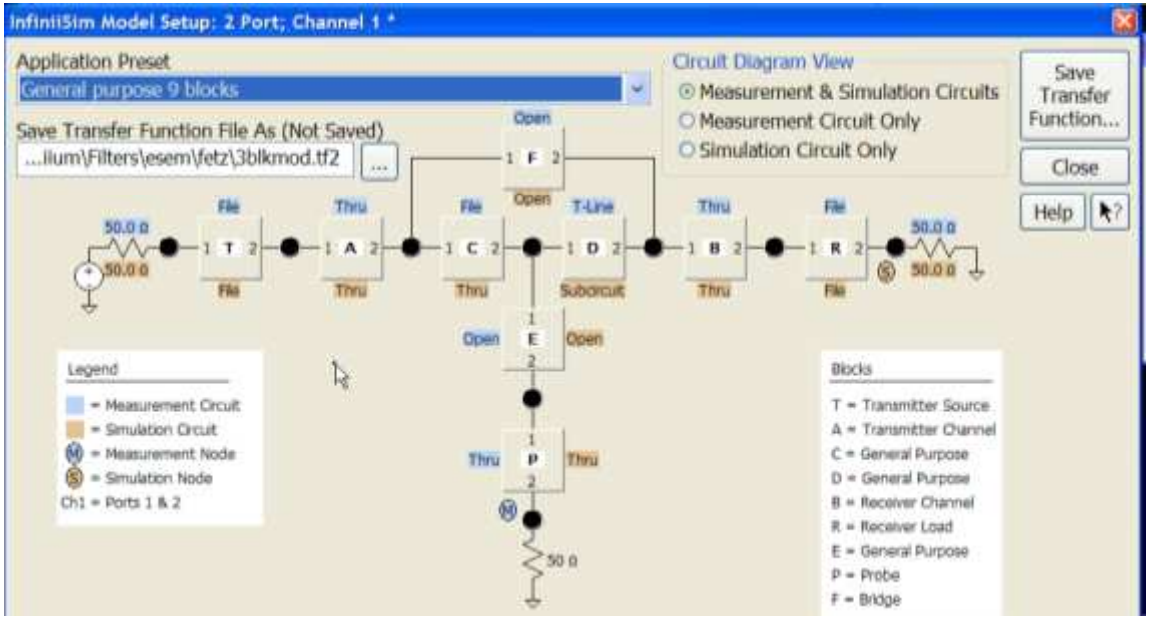


InfiniiSim: Go as Detailed as you need

From 1 block



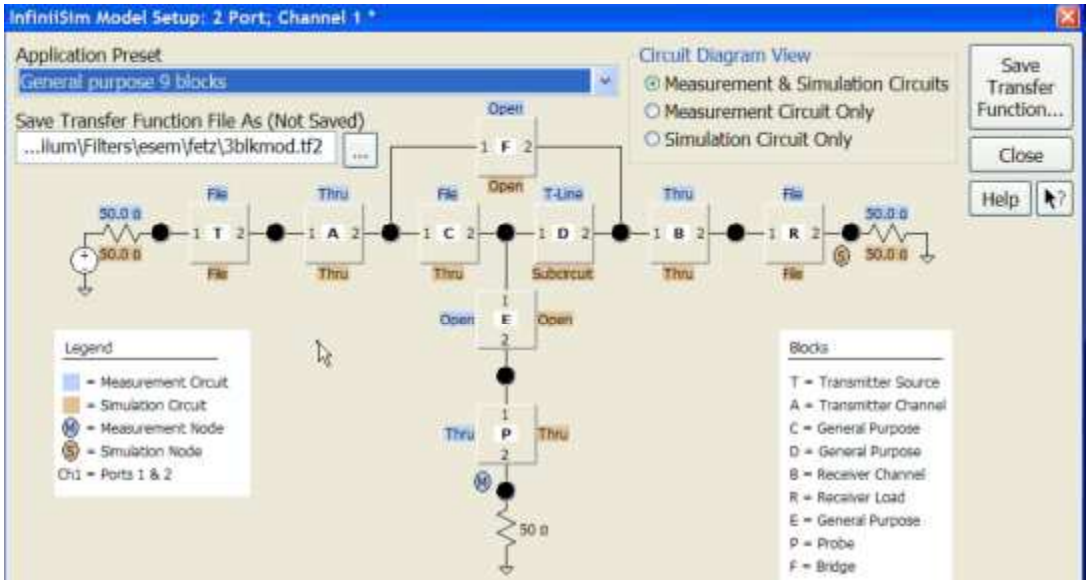
To 9 blocks

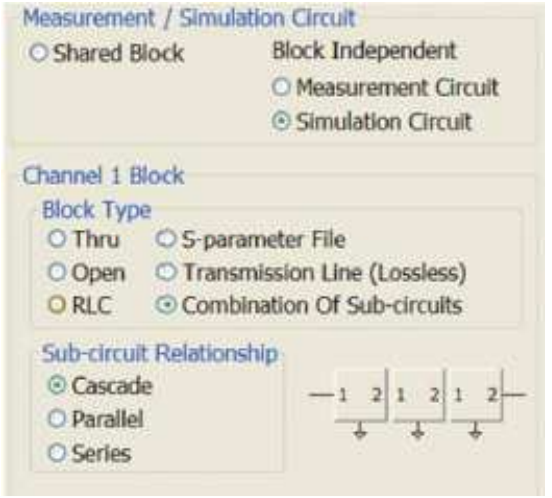


T= Tx, R = Rx, M = scope, S= Virtual probing point

InfiniiSim: Go as Detailed as you need

Each block can be a combination of 3 Sub-circuits



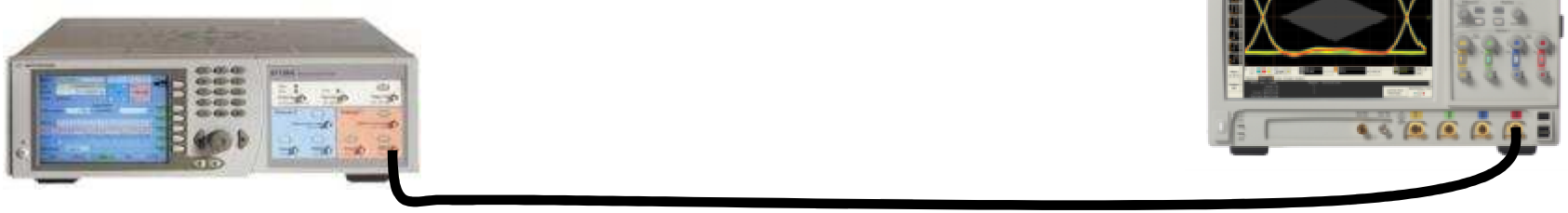


9 blocks
T= Tx, R = Rx, M = scope, S= Virtual probing point

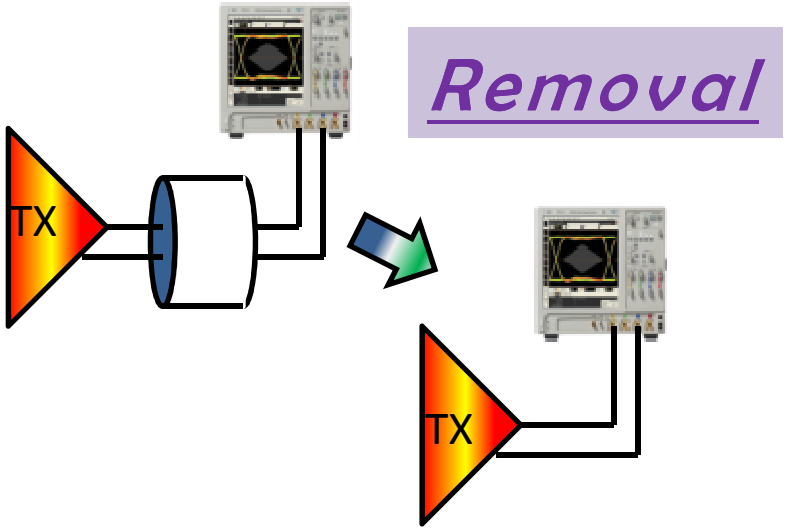
Each block can be a combination of 3 sub-circuits. Total 27 S-parameter files.

InfiniiSim Example: De-embedding of cable effect

- Generate 3Gb/s PRBS7 signal

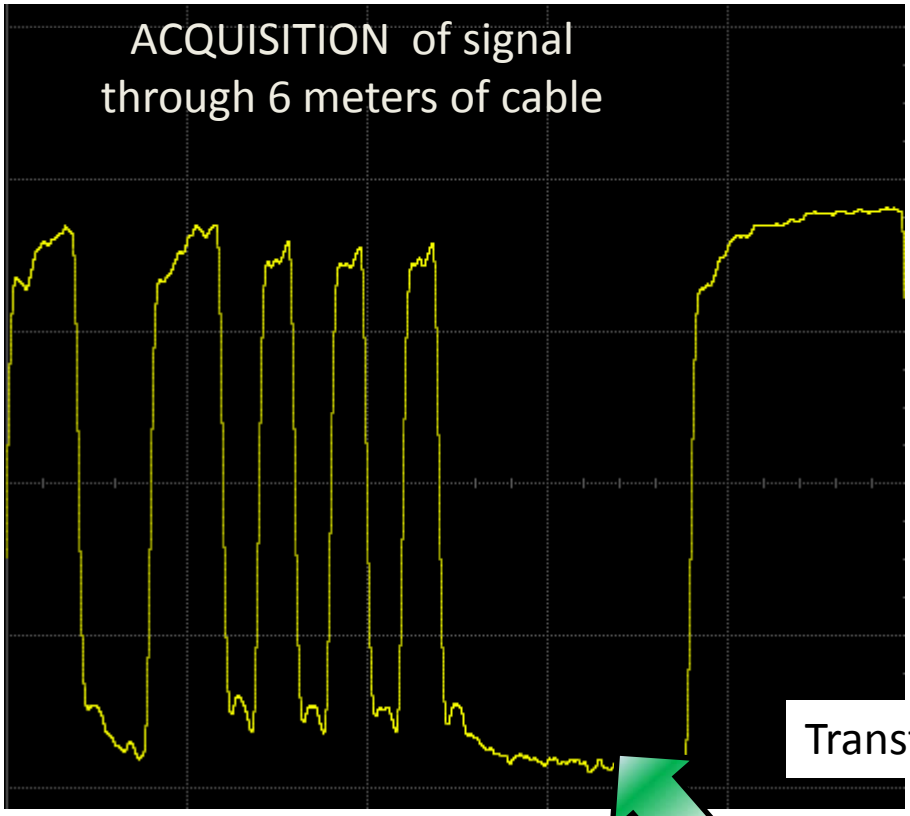


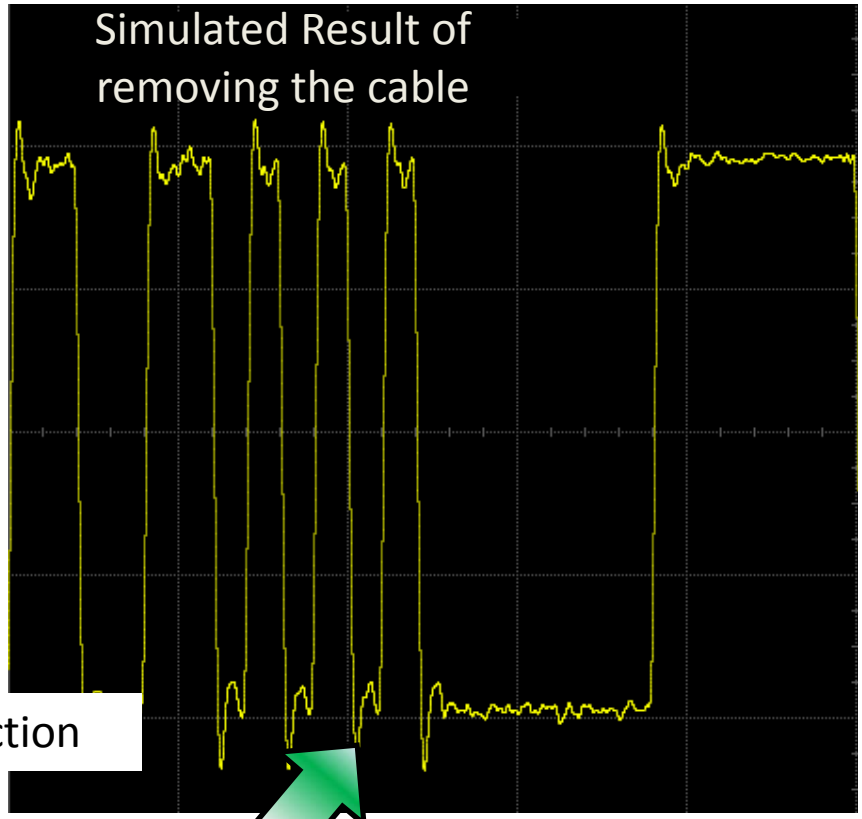
- Go through 6 meters of cable



InfiniiSim Example: De-Embedding of 6 meter Cable

We are going to perform a Transformation of a Waveform

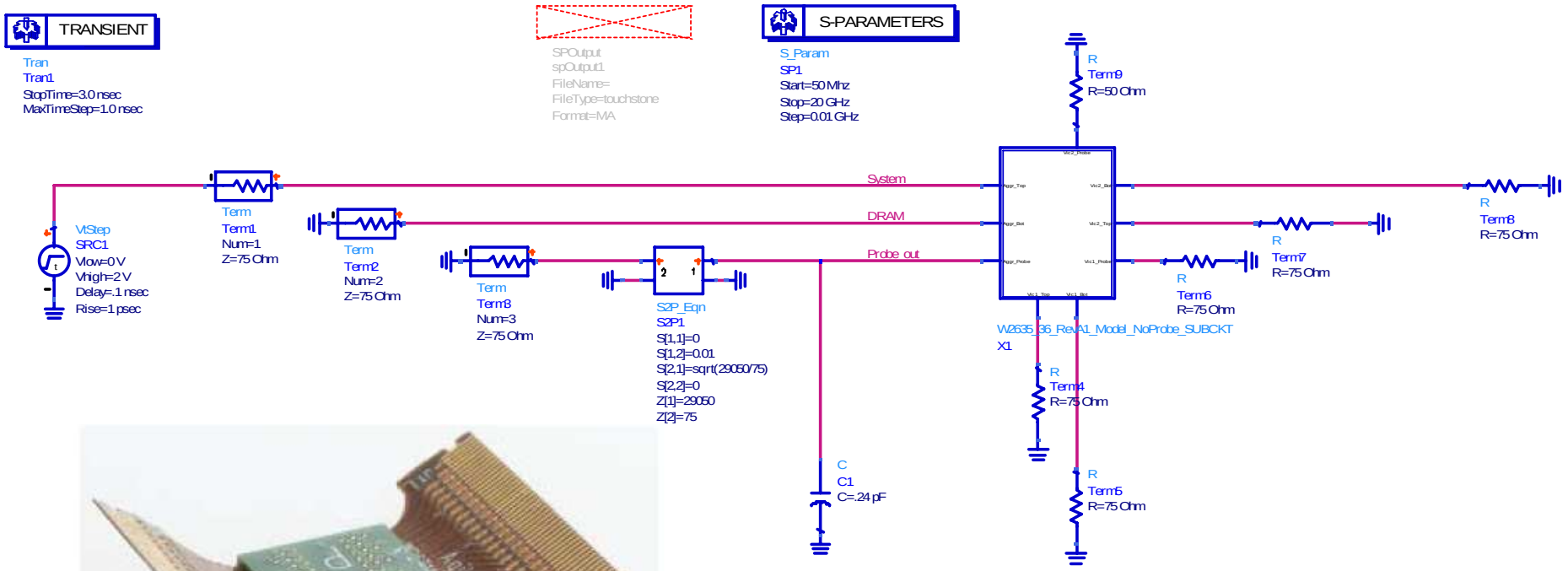


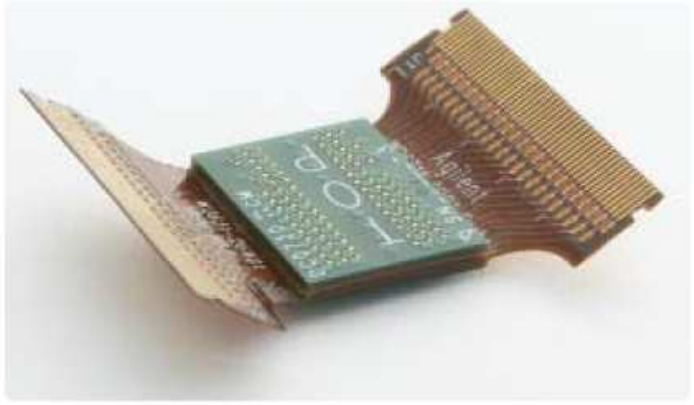


Transfer Function

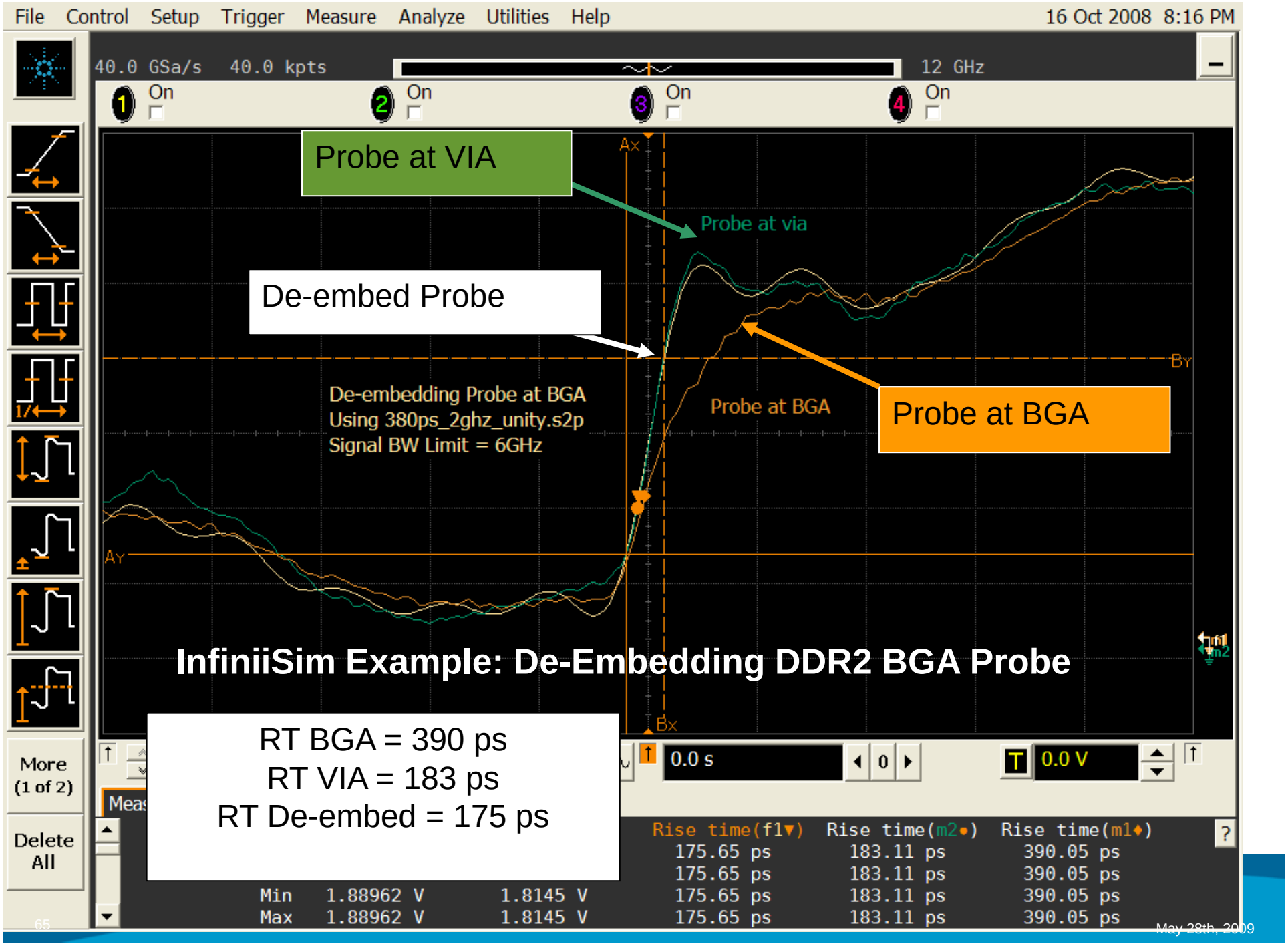
$$R(t) * H(t) = S(t)$$

InfiniiSim Example: De-Embedding DDR2 BGA Probe

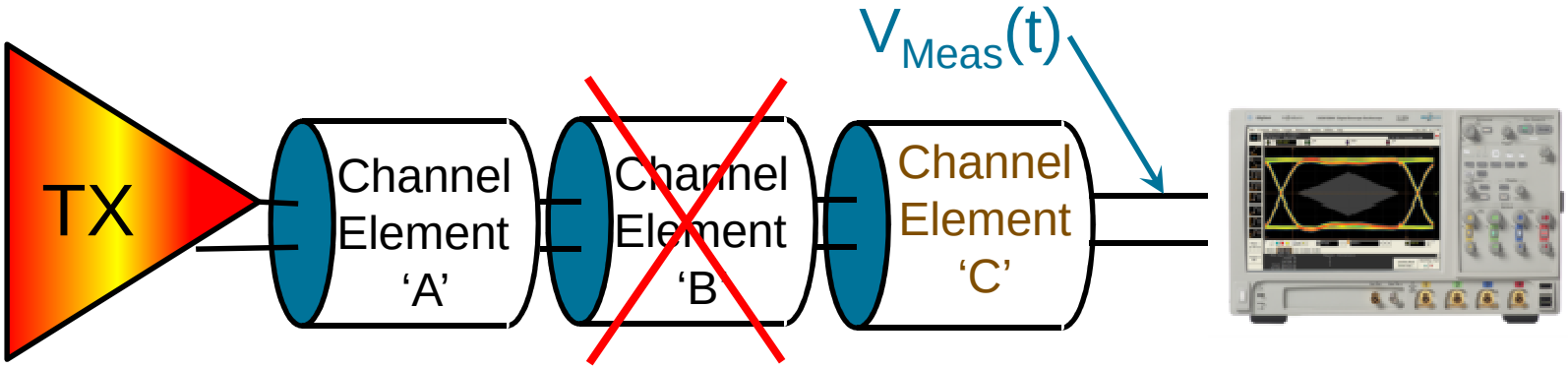




DDR2 BGA probe adapter for oscilloscopes and logic analyzers

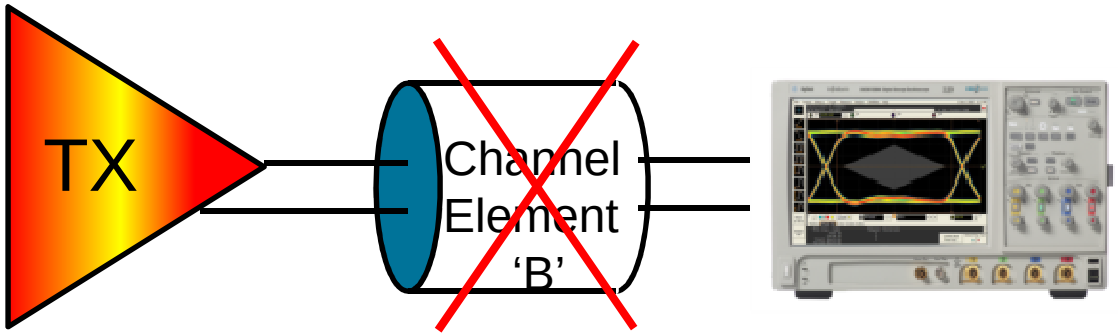

File Control Setup Trigger Measure Analyze Utilities Help
16 Oct 2008 8:16 PM
40.0 GSa/s 40.0 kpts
12 GHz
1 On
2 On
3 On
4 On
Probe at VIA
Probe at via
De-embed Probe
Probe at BGA
De-embedding Probe at BGA
Using 380ps_2ghz_unity.s2p
Signal BW Limit = 6GHz
InfiniiSim Example: De-Embedding DDR2 BGA Probe
RT BGA = 390 ps
RT VIA = 183 ps
RT De-embed = 175 ps
More (1 of 2)
Delete All
0.0 s
0.0 V
Rise time(f1▼) Rise time(m2•) Rise time(m1♦)
175.65 ps 183.11 ps 390.05 ps
Min 1.88962 V 1.8145 V
Max 1.88962 V 1.8145 V

Full De-Embedding versus *Insertion Loss Removal*



Full De-Embedding

VS.



Insertion Loss Removal

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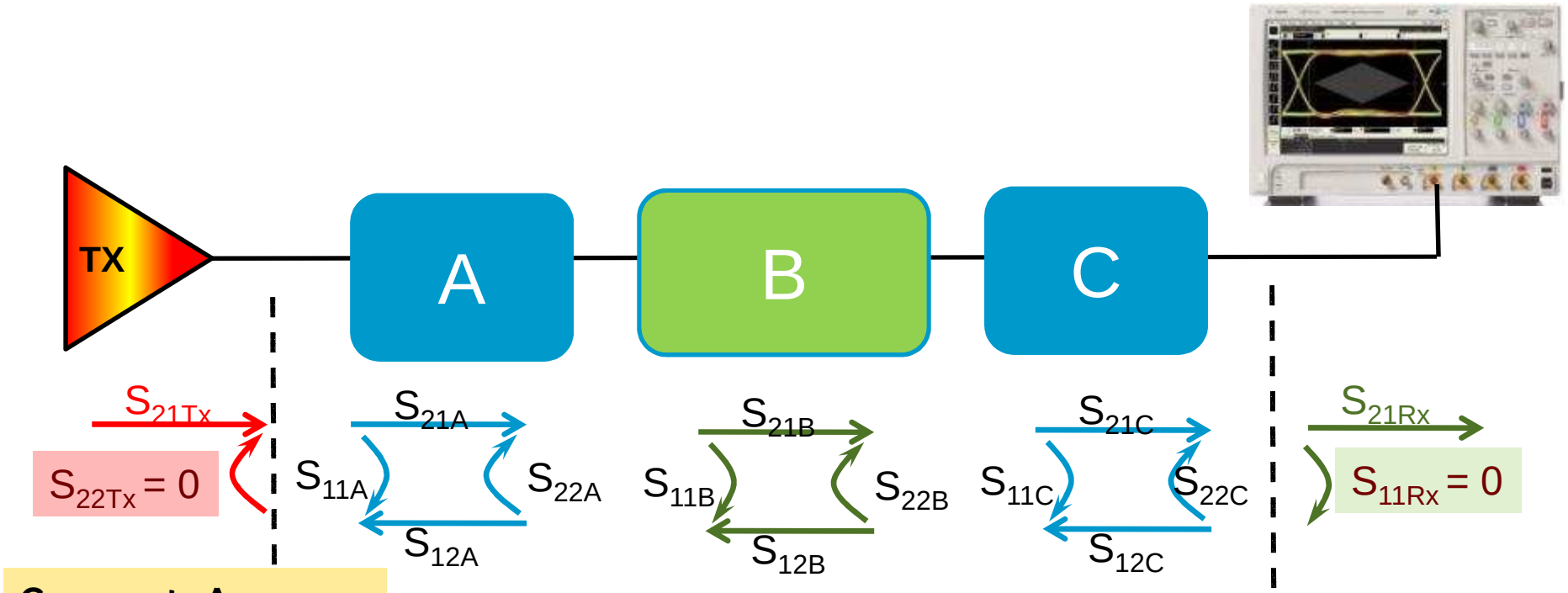
System Model



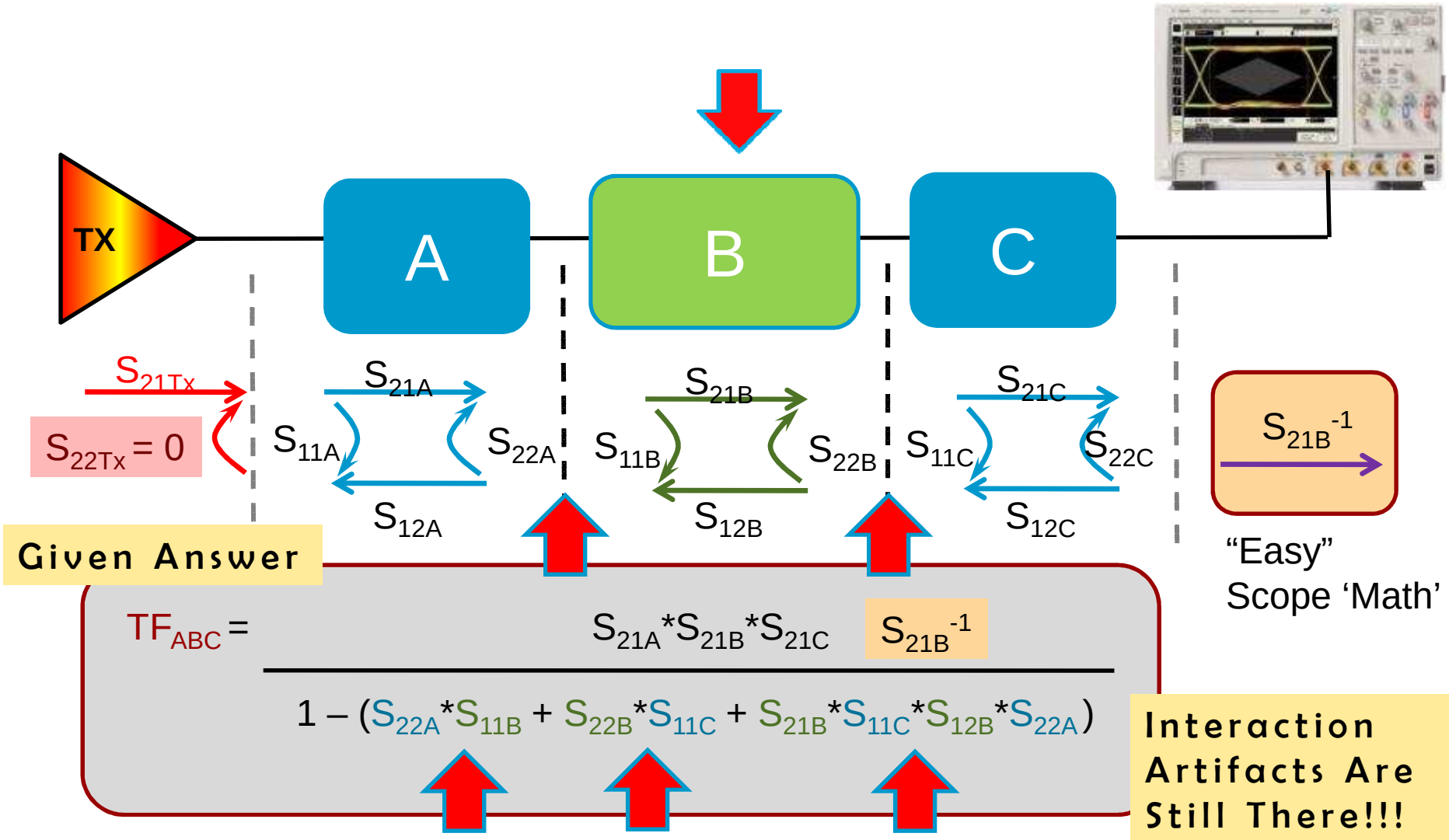
Correct Answer

$$TF_{ABC} = \frac{S_{21A} * S_{21B} * S_{21C}}{1 - (S_{22A} * S_{11B} + S_{22B} * S_{11C} + S_{21B} * S_{11C} * S_{12B} * S_{22A})}$$

Agilent Technologies

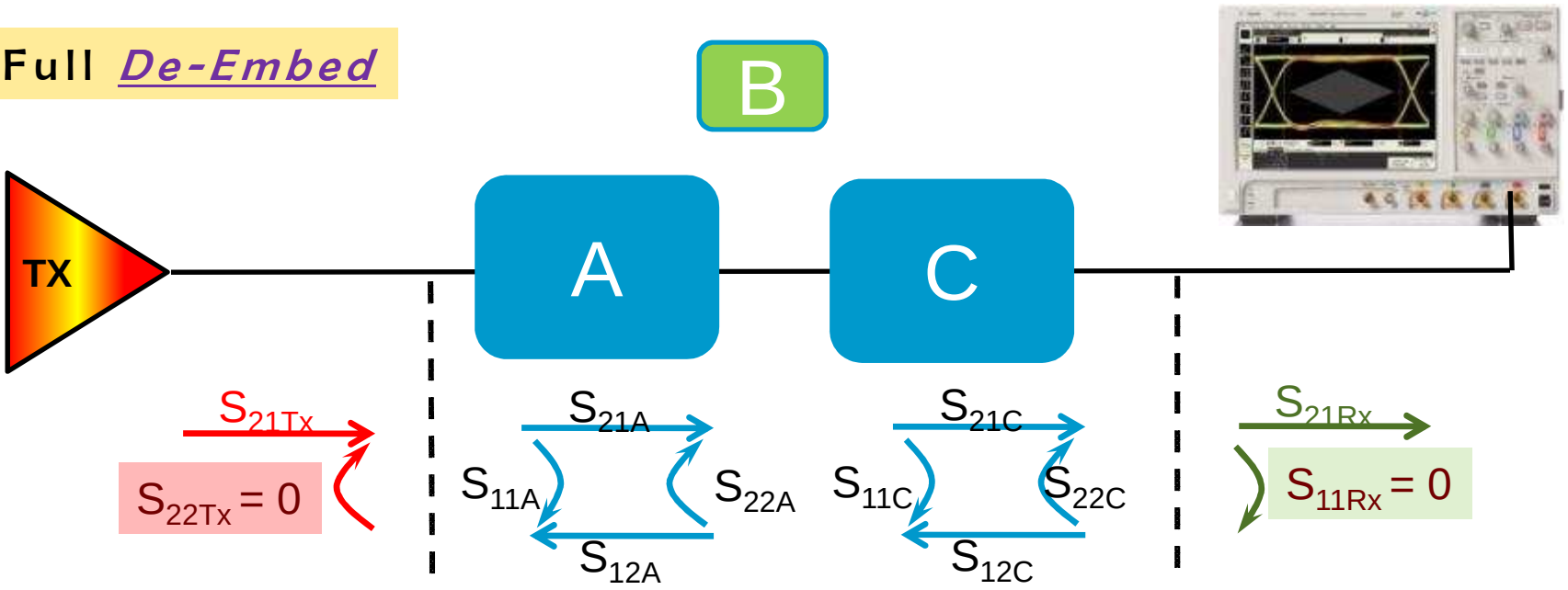
Comparing the two: Insertion Loss Removal

Insertion Loss Removal Uses "easy scope math": S_{21B}^{-1}



Comparing the two: true removal of block ‘B’

Full *De-Embed*



Correct Answer

$$TF_{AC} = \frac{S_{21A} * S_{21C}}{1 - (S_{22A} * S_{11C})}$$

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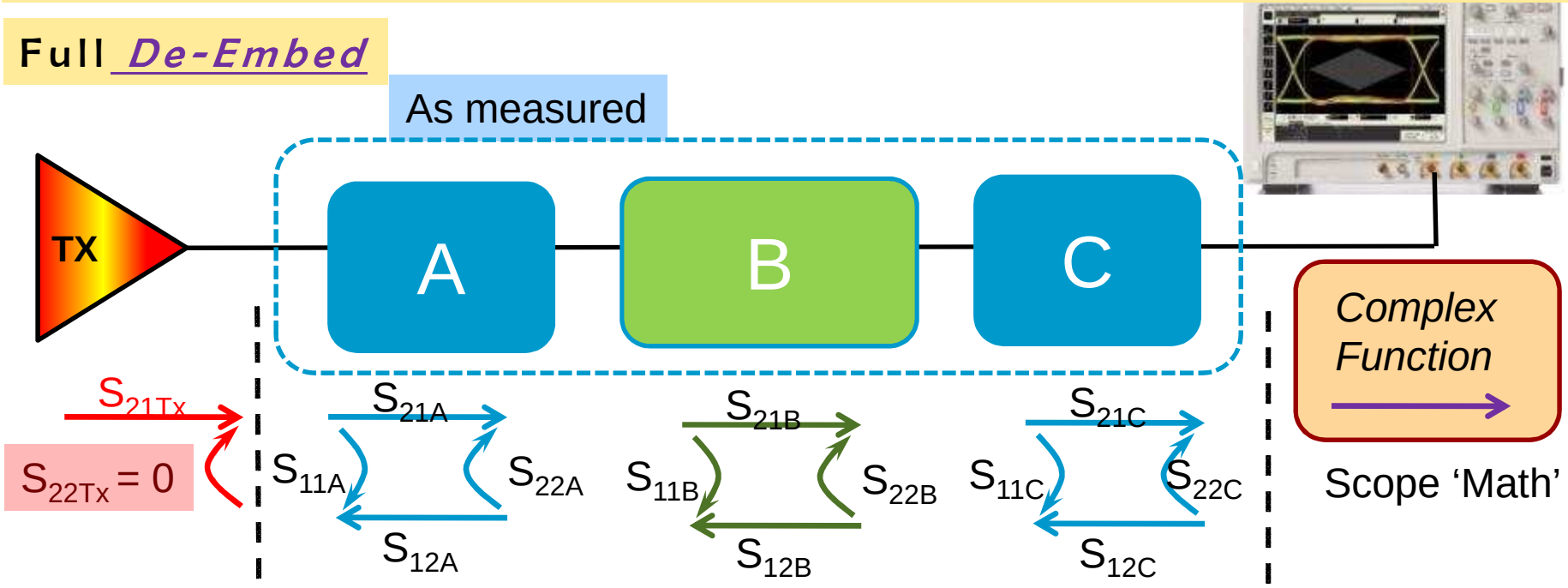
Comparing the two: Full De-embed

Full De-Embed uses "complex scope math" that removes also interaction artifacts (in this casebetween A-B and B-C and A-B-C) :

Full *De-Embed*



$$TF_{AC} = \frac{S_{21A}*S_{21B}*S_{21C}\,[1 - (S_{22A}*S_{11B} + S_{22B}*S_{11C} + S_{21B}*S_{11C}*S_{12B}*S_{22A})]\,S_{21B}^{-1}}{[1 - (S_{22A}*S_{11B} + S_{22B}*S_{11C} + S_{21B}*S_{11C}*S_{12B}*S_{22A})]\,[1 - (S_{22A}*S_{11C})]}$$

Interaction Artifacts Are Removed!!!

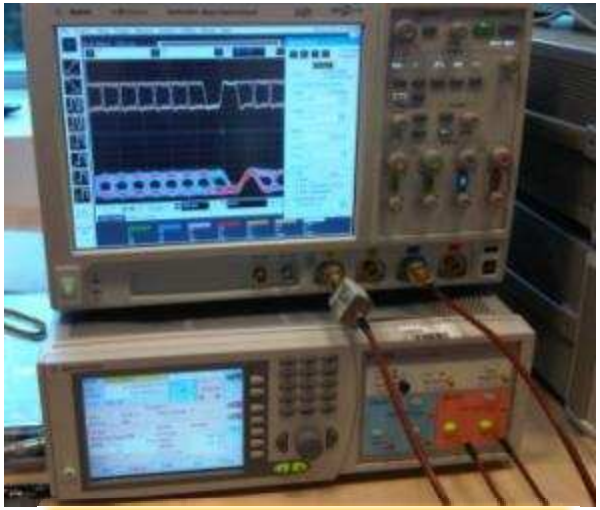
Agilent Technologies

DEMO InfiniiSim Virtual Probing

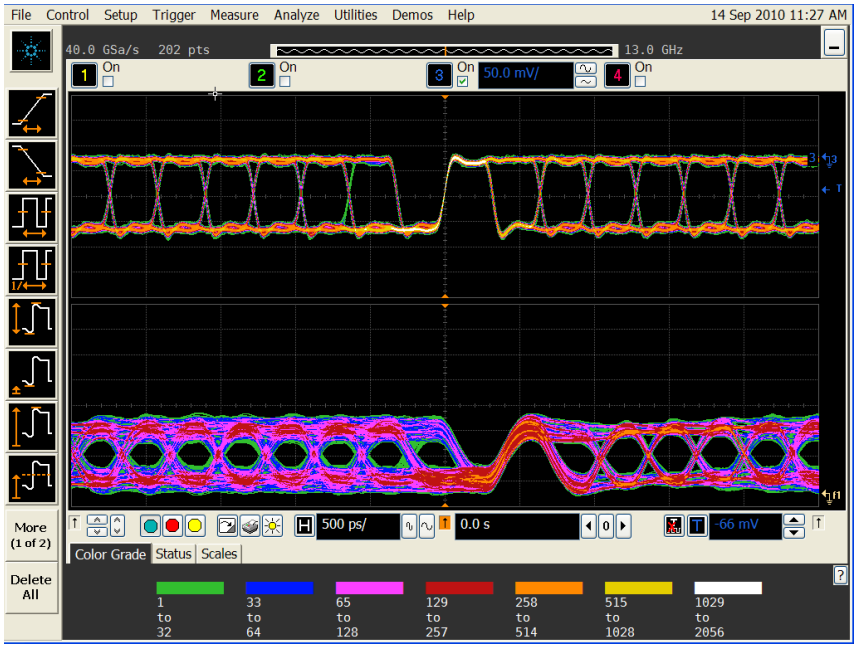
Test –Fixture to De-Embed

Agilent Technologies

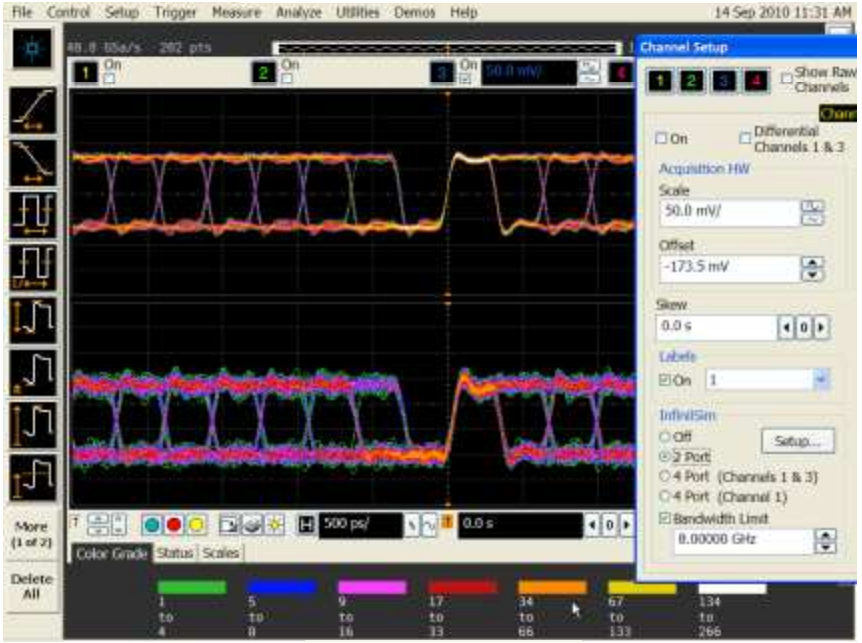
DEMO JIM
&
INFINIISIM



81134A/90.000 Setup at Amstelveen Office



Infiniisim OFF



Infiniisim ON

Agilent Technologies

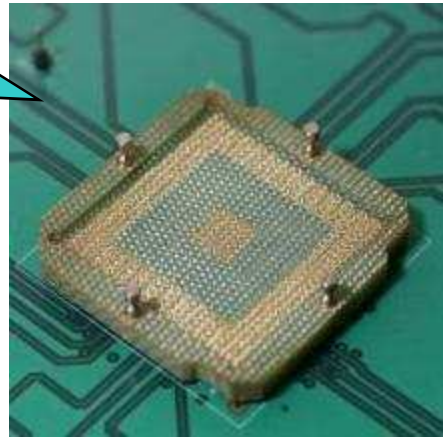
Agenda

1. Introduction
2. Eye Masks & TDR with an Network Analyzer
3. Pre-Emphasis
4. Equalization
5. Virtual probing / De-Embedding
6. ***Probing Hardware***
7. Practical examples
8. Summary

Agilent Technologies

How to inject data from PG in embedded design?

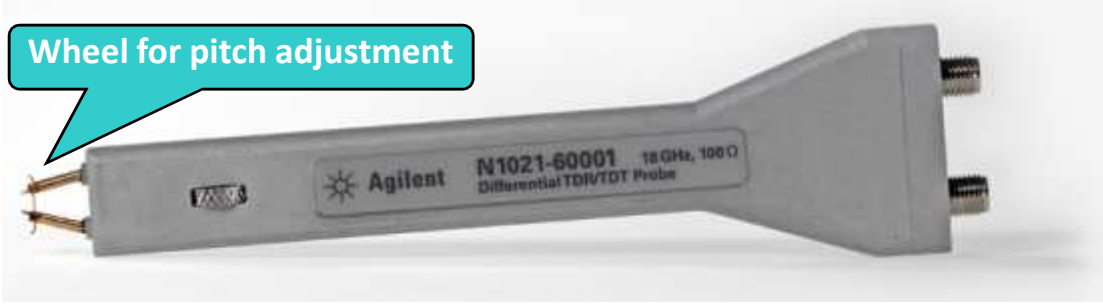
Differential traces



Agilent TDR Probe N1021B (100Ohm, 18GHz) mounted in 3D Probe Positioner N2787A could be used for pattern injection up to 18GHz.

EZ-Probe Positioner from Cascade Microtech, here shown with 6GHz passive TDR probe N1020A and Calibration Substrate N1020A-K05. For more information, see product overview 5968-4811EN.

Wheel for pitch adjustment



Differential Connectivity Kit

E2669A Differential Connectivity Kit

Differential Browser

- 6 GHz Bandwidth
- Input R: 50KΩ
- Input C: .33 pF
- Variable tip spacing, replaceable tips
- Dual tip Z-axis compliance

Ergonomic browser sleeve comes standard!

Differential Socketed

- 7 GHz Bandwidth
- Input R: 50KΩ
- Input C: 0.38 pF
- 100 mil socket spacing, accepts standard 20-mil round resistor leads

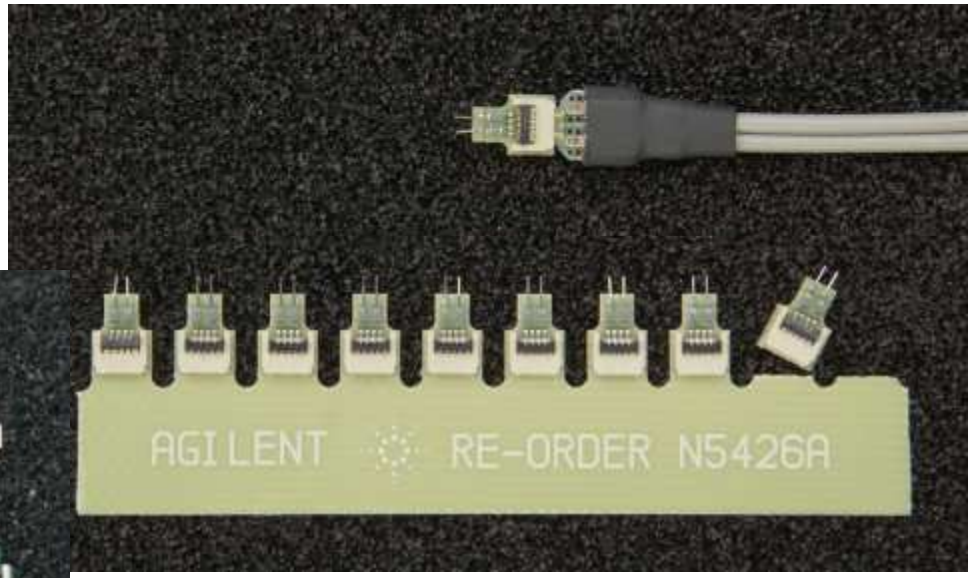
Differential Solder-In

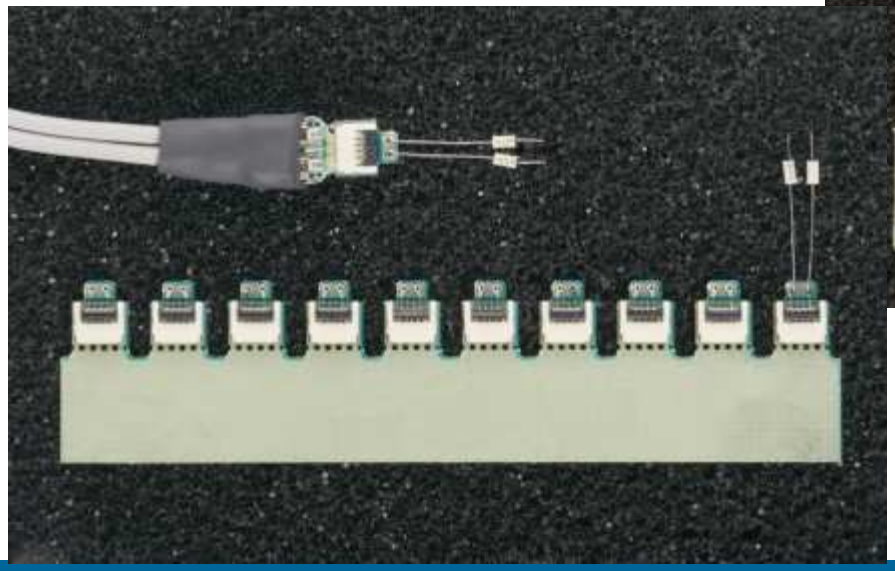
- 7 GHz Bandwidth
- Input R: 50KΩ
- Input C: 0.30 pF
- 8 mil tip leads are flexible

ZIF Probe Heads

Economical replaceable solder-in tips

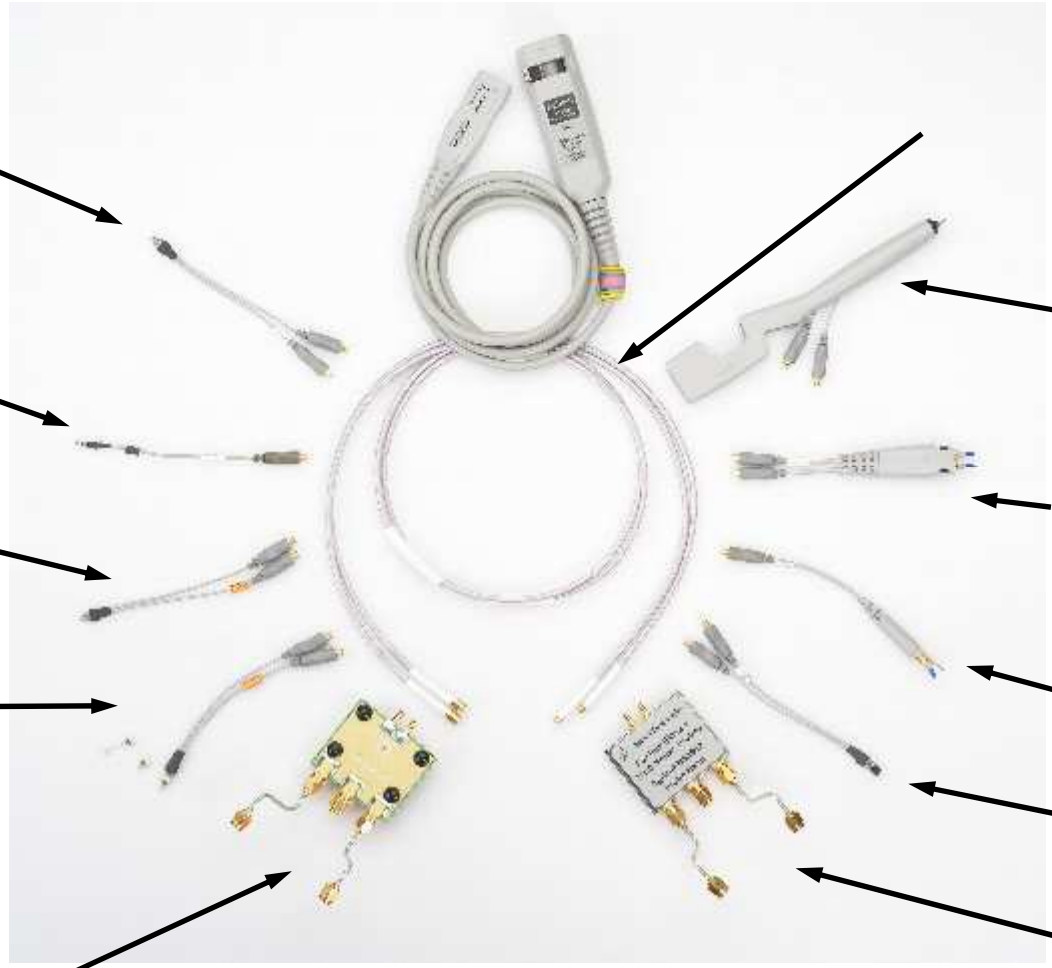
- ❑ N5451A Long-wire ZIF – extra span
  - ▪ >10 GHz (with 7mm wire) at zero deg span
  - ▪ > 5GHz (with 11mm wire) at zero deg span
- ❑ N5425A ZIF head + N5426A ZIF tips (qty 10)
  - • Full bandwidth (13 GHz)





Key applications: DDR memory system, server and storage, embedded applications

Probing Solutions for High Speed Realtime Scopes



12GHz differential solder-in probe head

6GHz single end solder-in probe head

12-13GHz differential solder-in probe head

12-13GHz differential ZIF solder-in probe head & ZIF Tip & Long Wire ZIF Tip (4~9GHz)

8GHz SMA probe head

InfiniiMax extreme temp extension cable (-55 ~ 150 C)

12-13GHz differential browser probe head

6GHz differential browser probe head

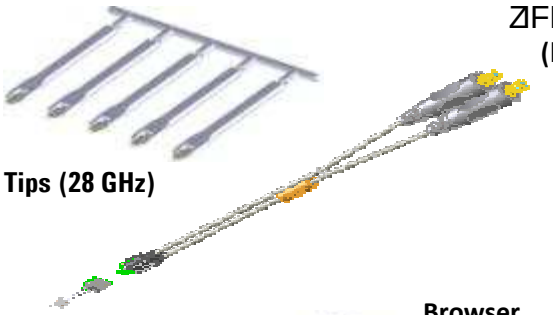
5GHz single end browser probe head

12GHz Socket probe head

12-13GHz SMA probe head

True Analog Bandwidth that Delivers…
Full 30 GHz Probing System

NEW



ZIF Probe Head
(N5439A)
28 GHz

ZIF Tips (28 GHz)

Probe Pod & Amplifier
Full Bandwidth

Browser
(N5445A) 30
GHz

2.92/3.5 mm Probe Head
(N5444A) – 28 GHz

Solder-in (N5441A)
Probe 16 GHz

Sampling Scope Adaptor
(N5477A)
Full Bandwidth

igh Impedance
(N5449A)
daptor 500MHz

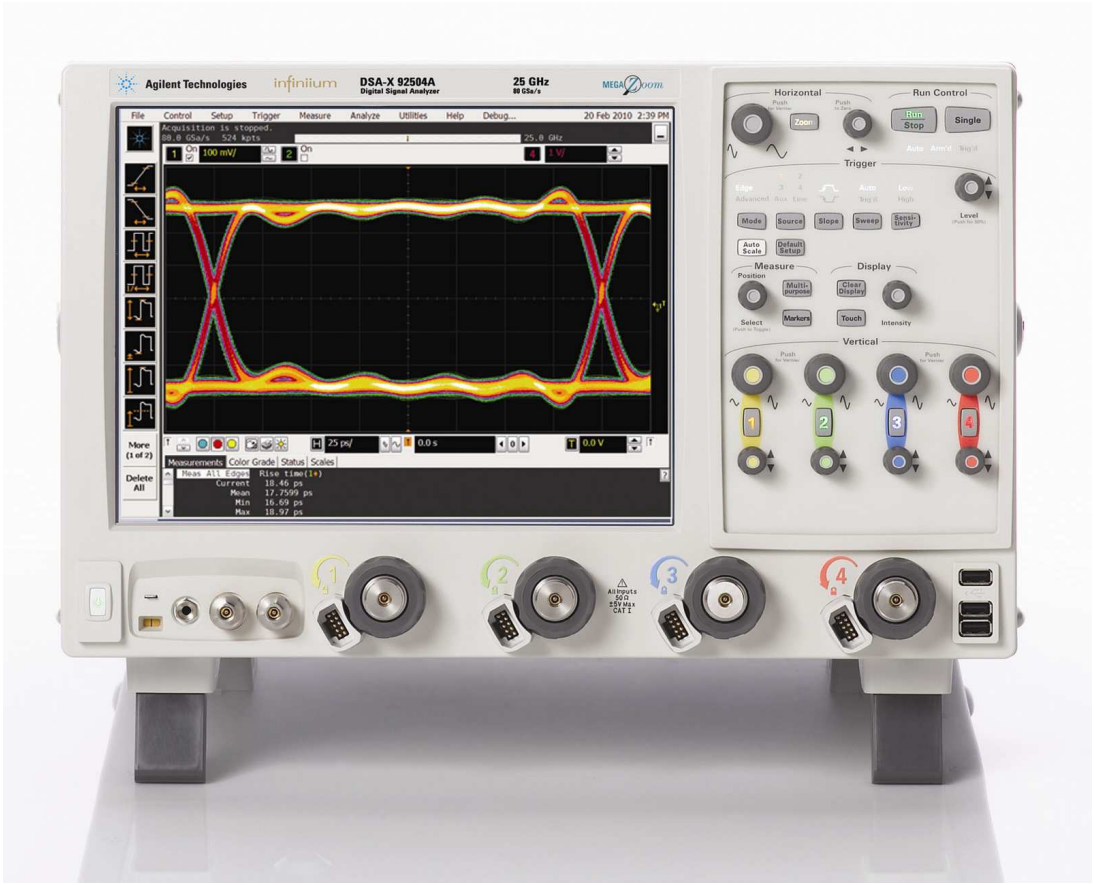
PV/Deskew Fixture
(N5443A)

IniniiMax I and II
Adaptor (N5442A)

- ✓ Integrated de-embedding with customized s-parameter loaded in the amp
- ✓ Fully upgradeable hardware

Introducing the Infiniium 90000 X-Series Oscilloscopes

Engineered for 32 GHz true analog bandwidth that delivers

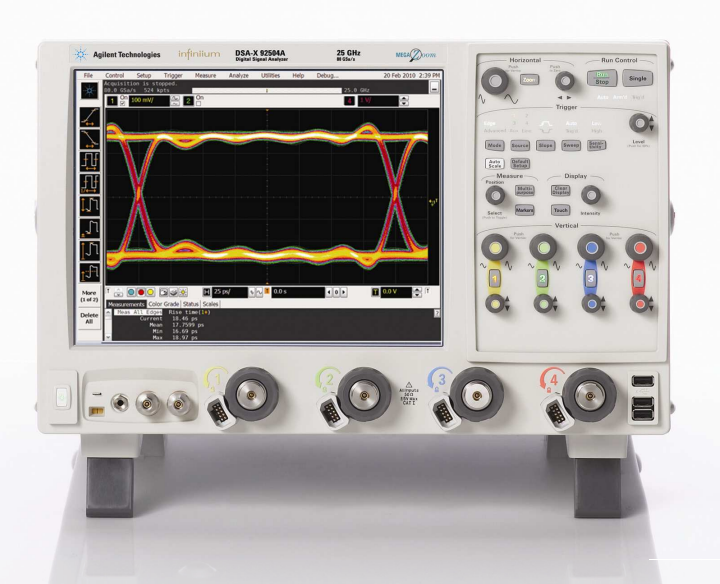


The industry's highest measurement accuracy

Full 30 GHz probing system

The most comprehensive software specific application software

Infiniium 90000 X-Series Oscilloscopes



Engineered for true analog bandwidth that delivers

- ✓ The highest real-time scope measurement accuracy
- ✓ Complete 30 GHz oscilloscope probing system
- ✓ The industry's most comprehensive application-specific measurement software

Bandwidth upgradeable for investment protection

6 New Scope Models	DSO/DSA91604A	DSO/DSA92004A	DSO/DSA92504A	DSO/DSA92804A	DSO/DSA93204A
Analog Bandwidth (2 ch)	16 GHz	20 GHz	25 GHz	28 GHz	32 GHz
Max Sample Rate (2 ch/4 ch)	80/40 GSA/s	80/40 GSA/s	80/40 GSA/s	80/40 GSA/s	80/40 GSA/s
Std Memory	10M	10M	10M	10M	10M
Max Memory	2 Gpts	2 Gpts	2 Gpts	2 Gpts	2 Gpts
Noise @ 50mV/div	1.34 mV	1.53 mV	1.77 mV	1.89 mV	2.08 mV
Jitter Measurement Floor	150 fs rms	150 fs rms	150 fs rms	150 fs rms	150 fs rms

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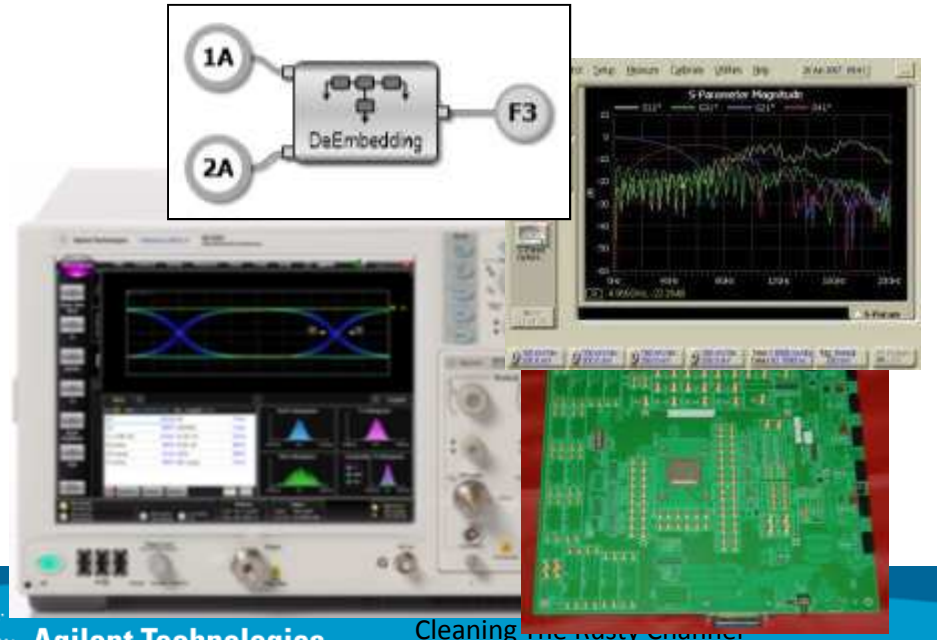
7. Practical Examples

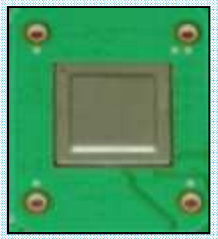
1. ***High-Speed Characterization (effect of 4.5 GHz Notch in test fixture)***
2. **BGA probe setup in infiniisim Virtual Probe**
3. **Tuned, measurement enhanced, IBIS parameters for DDR**
4. **Creating S2P (touchstone) files from Gerber files**
5. **Basic Steps for Optimizing a Serial Link**
6. **Serial Data Analysis Solutions: 8b10b Trigger, Decode, Search and Listing Feature**
7. **Small peek inside the 90.000 X 32 GHz scope**

Practical example1
High-Speed IC Characterization

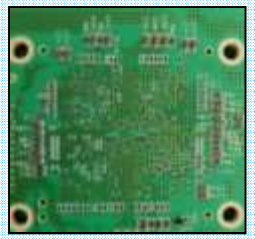
1. Fixture Characterization – obtain your model
2. Simulate waveform using the model
3. Verify model and waveform with an actual measurement
4. Apply the model and De-Embed Fixture
   - measure at connectors & simulate signal at balls of IC



Characterizing High-Speed Integrated Circuits (IC)



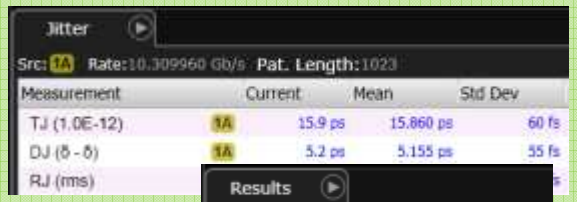
IC - Top

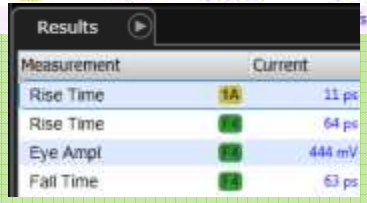


IC - Bottom

Device:

ASIC / FPGA / SERDES / Other High-Speed IC





Precision Characterization

What parameters get measured?
Full characterize includes measuring amplitude, rise/fall times, jitter (all types), etc. under various operating conditions.

Who? Where?
Performed by engineers and technicians in Performance Verification (PV) and Characterization labs

How are they measured?
Accuracy and precision is critical, so engineers often use a sampling scope due to:

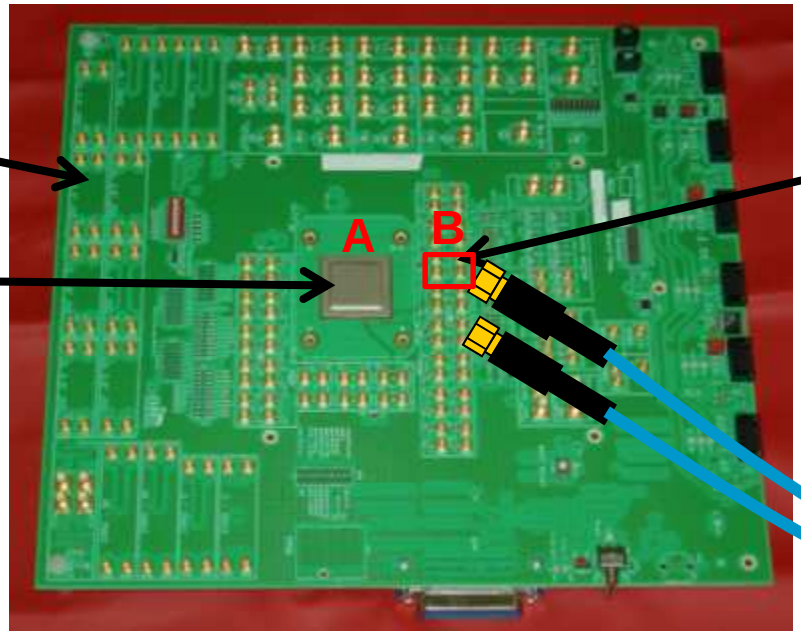
- High analog bandwidth (18GHz->90GHz)
- Low noise (<300uV)
- Ultra-low jitter (RJ<60fs)

Agilent Technologies

Custom Fixtures

Accurate characterization often requires custom fixtures.

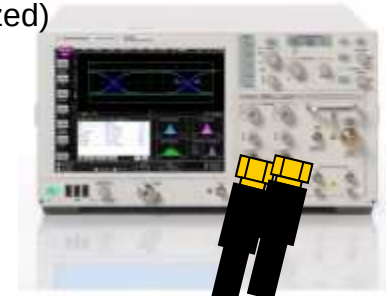
- Probing introduces measurement challenges
- Bring signals out to connectors
- Good fixture layout minimizes signal degradation



Test Fixture

DUT
TX Output at the pads/balls of the IC

Measure actual signal here using cables between fixture and scope (connectorized)



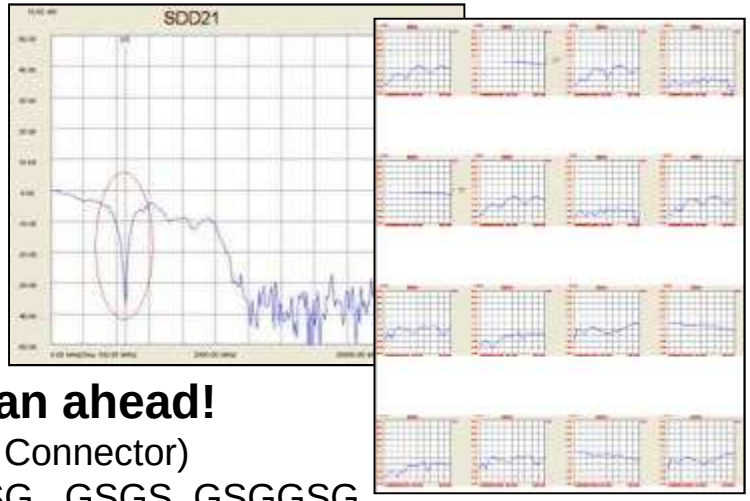
- **Problem:** **Fixture will degrade signal and may not represent end-user's implementation**

- **Solution:** **Remove fixture effects of the transmission line from pt A to pt B (commonly referred to as de-embedding). Allows us to predict the TX performance at the balls/pins of the IC, and/or predict performance using a different layout/material**

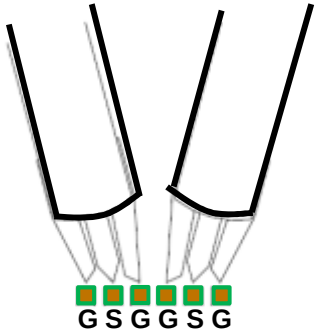
Agilent Technologies

Step 1: Fixture Characterization – obtain your model

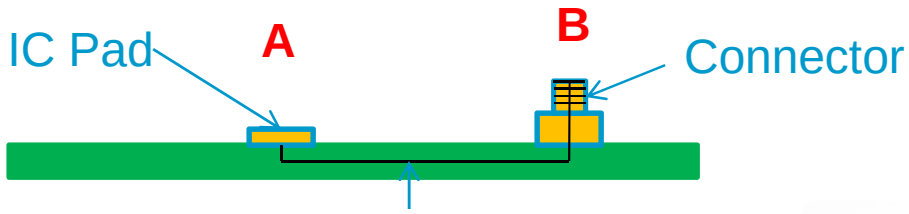
- **Generate an S-parameter model**
  - **a. Simulation**
    - o Use design software such as Agilent ADS, PLTS
  - **b. Measure**
    - o Use VNA (ENA/PNA) or TDR
    - o Do-It-Yourself or consult with an expert such as GigaTest Labs



- **Characterize raw (unpopulated) board – plan ahead!**
  - Add test coupons to fixture (e.g. Connector – pad, pad - Connector)
  - Layout pads with adjacent grounds for probing e.g. GSSG, GSGS, GSGGSG
  - Full S-Parameters - need differential probe that includes ground contacts



Differential Probe
- usually used with positioner
- select specific footprint, pitch, may be adjustable



Goal: Accurately characterize the signal path from pad to connector. Generate a .s2p or .s4p Touchstone file.

N1021B

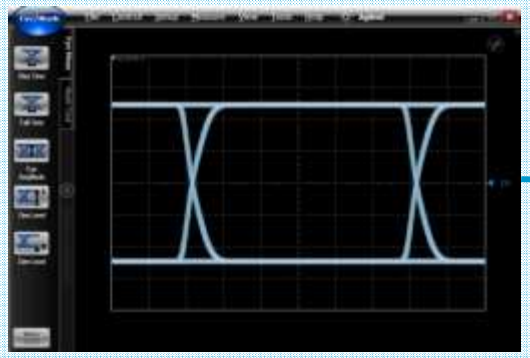
Handheld 18GHz Differential TDR Probe
- for fully balanced differential signals (no ground contact)

Agilent Technologies

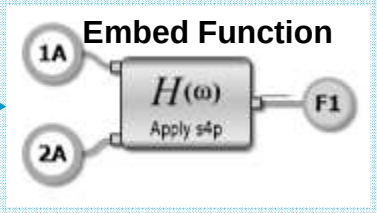
Step 2-3 Use your model to Simulate…then Verify

2. Simulate waveform using model (input –> apply S-parameter model -> output)

- simulate expected DUT TX signal (e.g. 10Gb/s, PRBS7, Rise/Fall Time = 25ps)

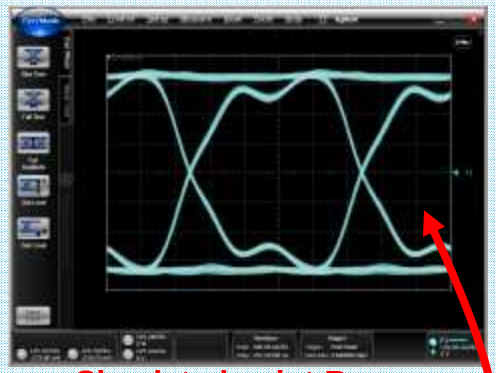


Simulated point A



SW Simulated Input Signal

SW Simulated Output Signal



Simulated point B

3. Verify model and waveform with an actual measurement
(inject signal from PG –> actual DUT -> measure O/P)

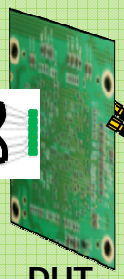
Good Correlation

- generate expected DUT TX signal using BERT, inject via probe, measure on scope

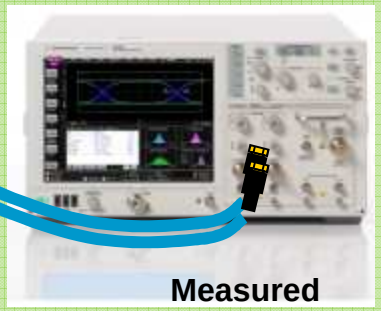
Input Signal from PG

Point A

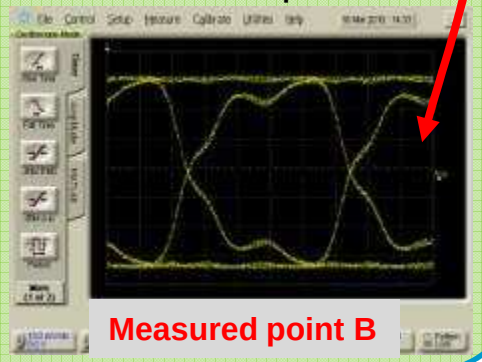
Probe



DUT (raw board)



Measured Output Signal

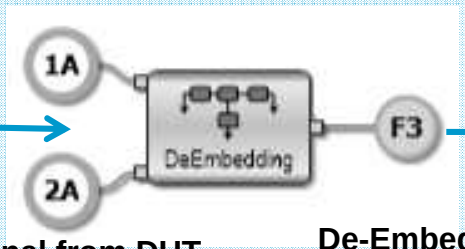


Measured point B

Agilent Technologies

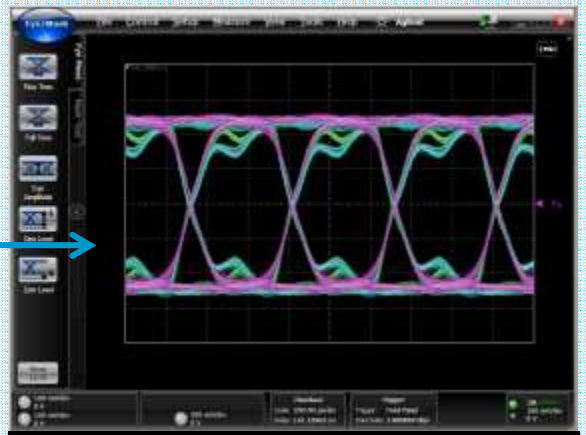
Step 4 - Fixture Removal (de-embedding)

4. De-Embed Fixture- measure at connectors (B), simulate signal at balls of IC (A)



Signal from DUT

De-Embedded Output Signal

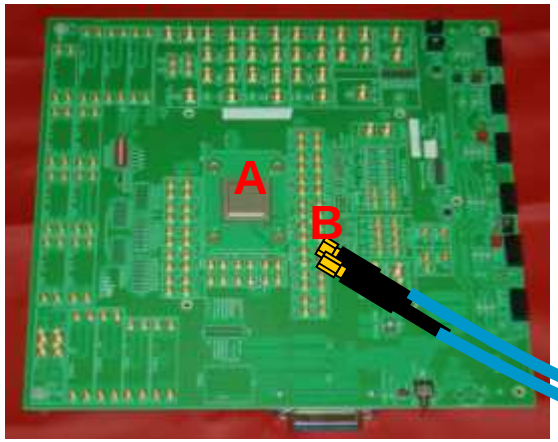


Yellow = measured signal (Actual DUT + Fixture + Cables)

Measure at Point B

Pink = de-embedded signal

Simulated Signal at Point A



Benefits:

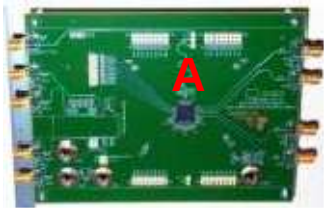
- Improved Margins
- More accurate representation of TX performance (at point 'A')
- Simulate signal using different fixture without building it (cascade functions)
- Gain valuable insight

Note – could also remove cable effects too

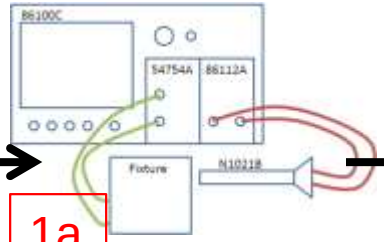
Agilent Technologies

Case Study – design your fixtures carefully!

Step 1



DUT - fixture
SMA-pads



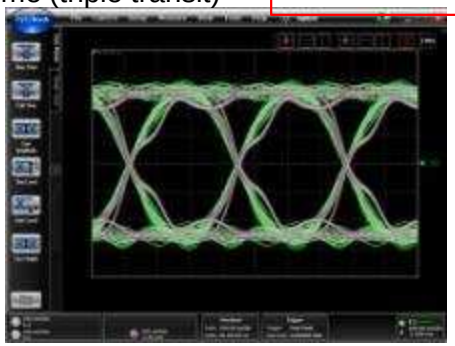
1a

Characterize fixture
with Agilent TDR and probe
-> Generate .s4p

S-Parameter has notch at 4.5GHz

TDR into open (Step Response) has a very long settling time (triple transit)

Steps 2, 3, 4a



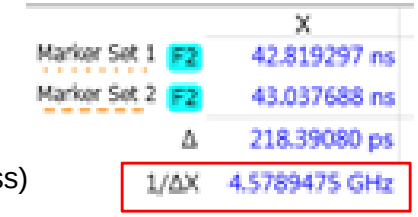
Eye Diagram
Purple – raw signal (reflection)
Green – de-embedded signal (noise)

5

Summary

- large notch in S-Parameter due to large reflection in the fixture (be wary of triple-transit !!)
- the 'inverse' function (de-embed) amplifies a lot of noise in the notch region => causes ringing
- must setup de-embed function to filter out notch at 4.5MHz.
- if left "as is", max data rate for fixture ~1Gb/s.
- analyzing S-parameters can help predict effectiveness of de-embedding (look for excessive loss)

Step 4b



SI design flaws cannot be hidden by De-emphasis, Equalization or de-embedding/virtual probing!!!!!

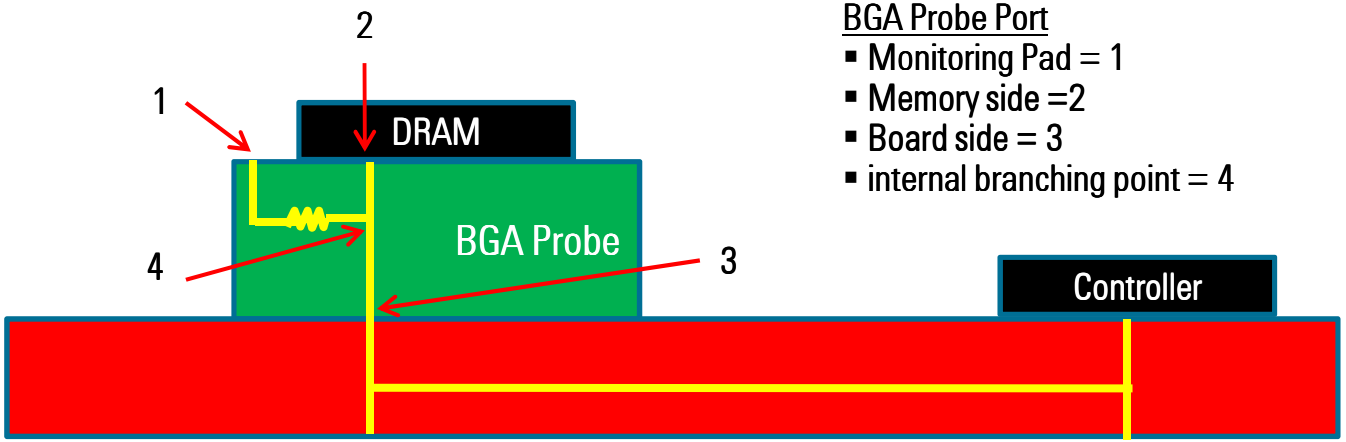
Agilent Technologies

Agenda

7. Practical Examples

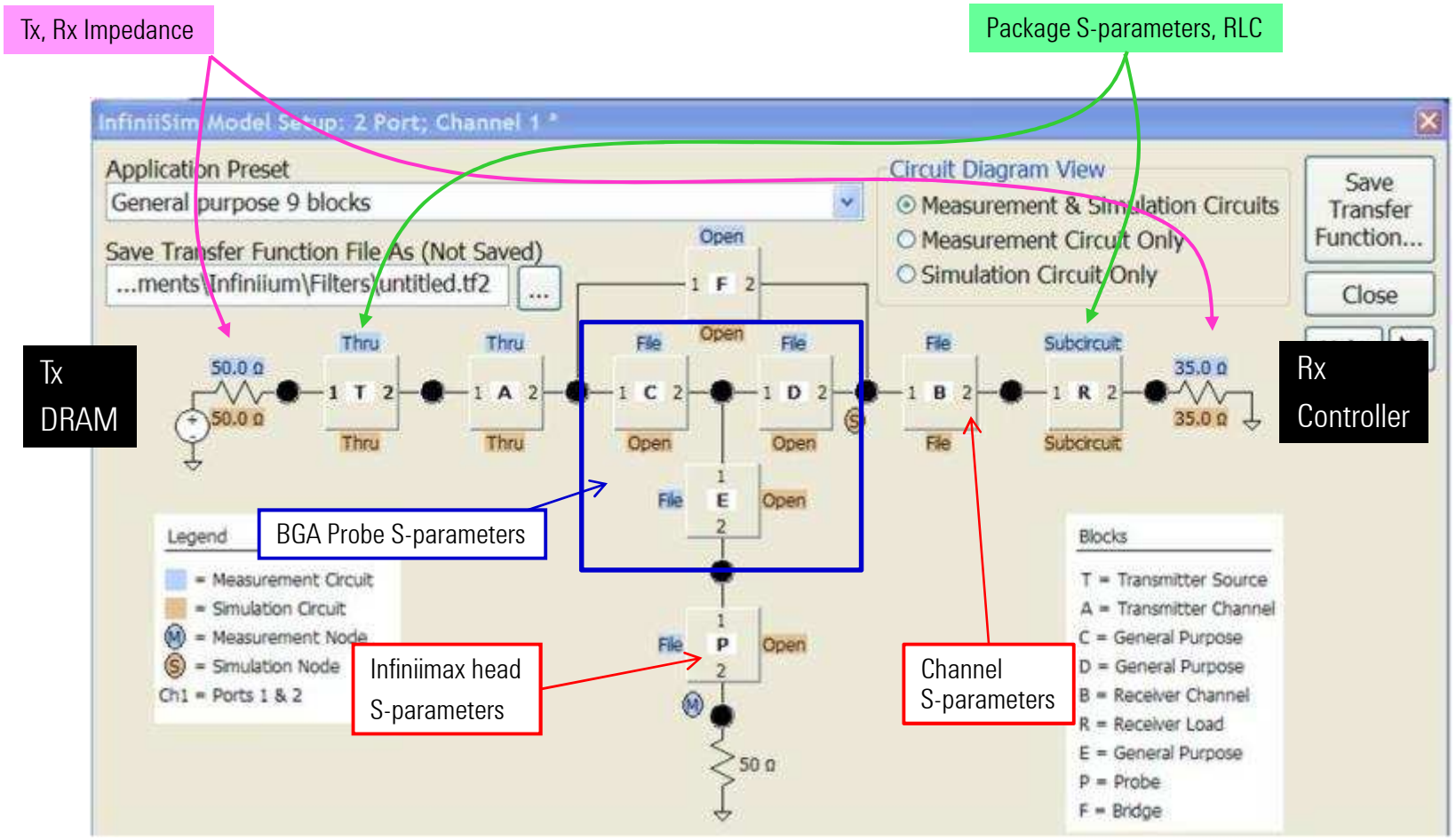
1. High-Speed Characterization (effect of 4.5 GHz Notch in test fixture)
2. *BGA probe setup in infiniisim Virtual Probe*
3. Tuned, measurement enhanced, IBIS parameters for DDR
4. Creating S2P (touchstone) files from Gerber files
5. Basic Steps for Optimizing a Serial Link
6. Serial Data Analysis Solutions: 8b10b Trigger, Decode, Search and Listing Feature
7. Small peek inside the 90.000 X 32 GHz scope

BGA Probe

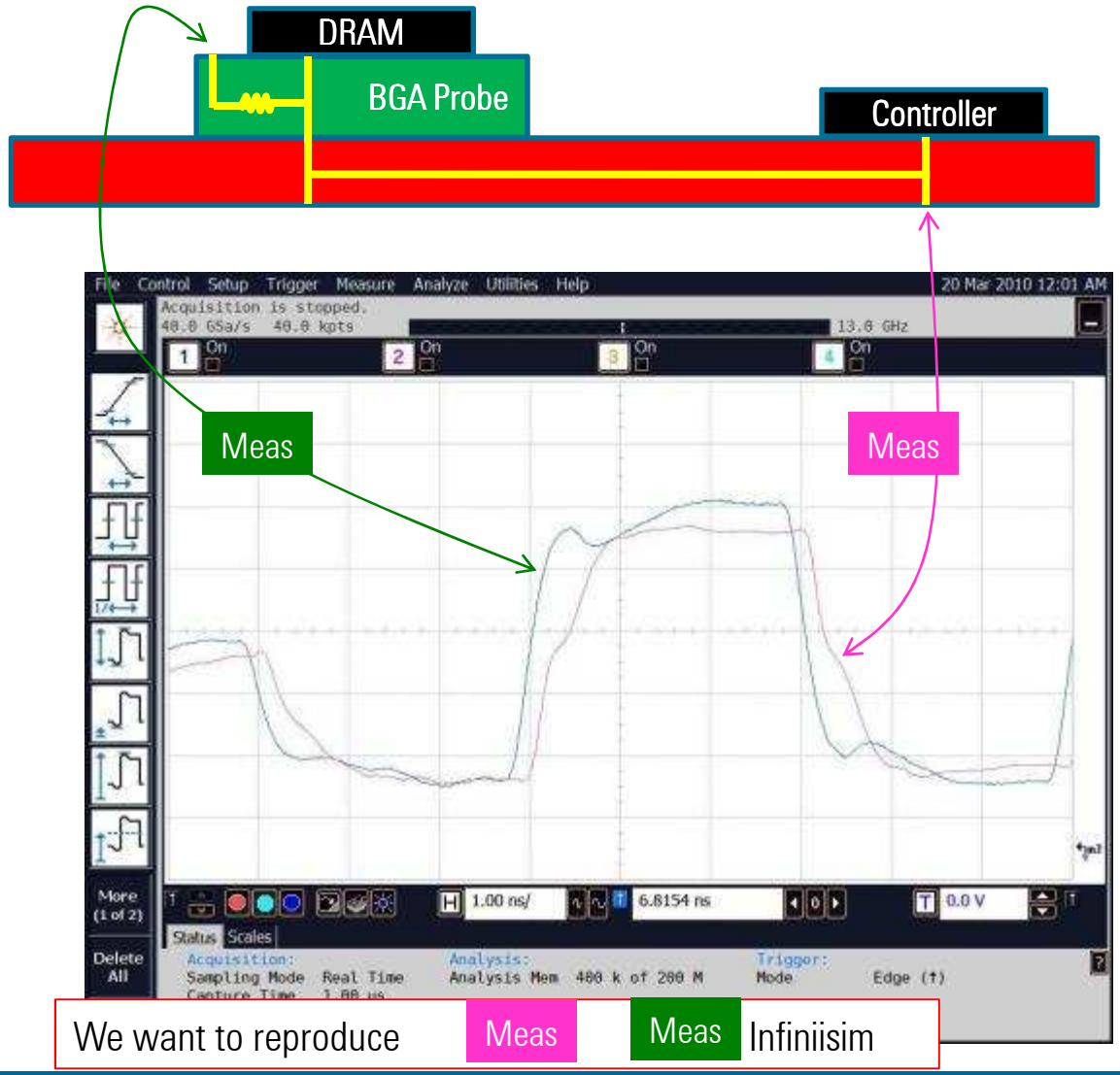


BGA Probe Port
- Monitoring Pad = 1
- Memory side =2
- Board side = 3
- internal branching point = 4

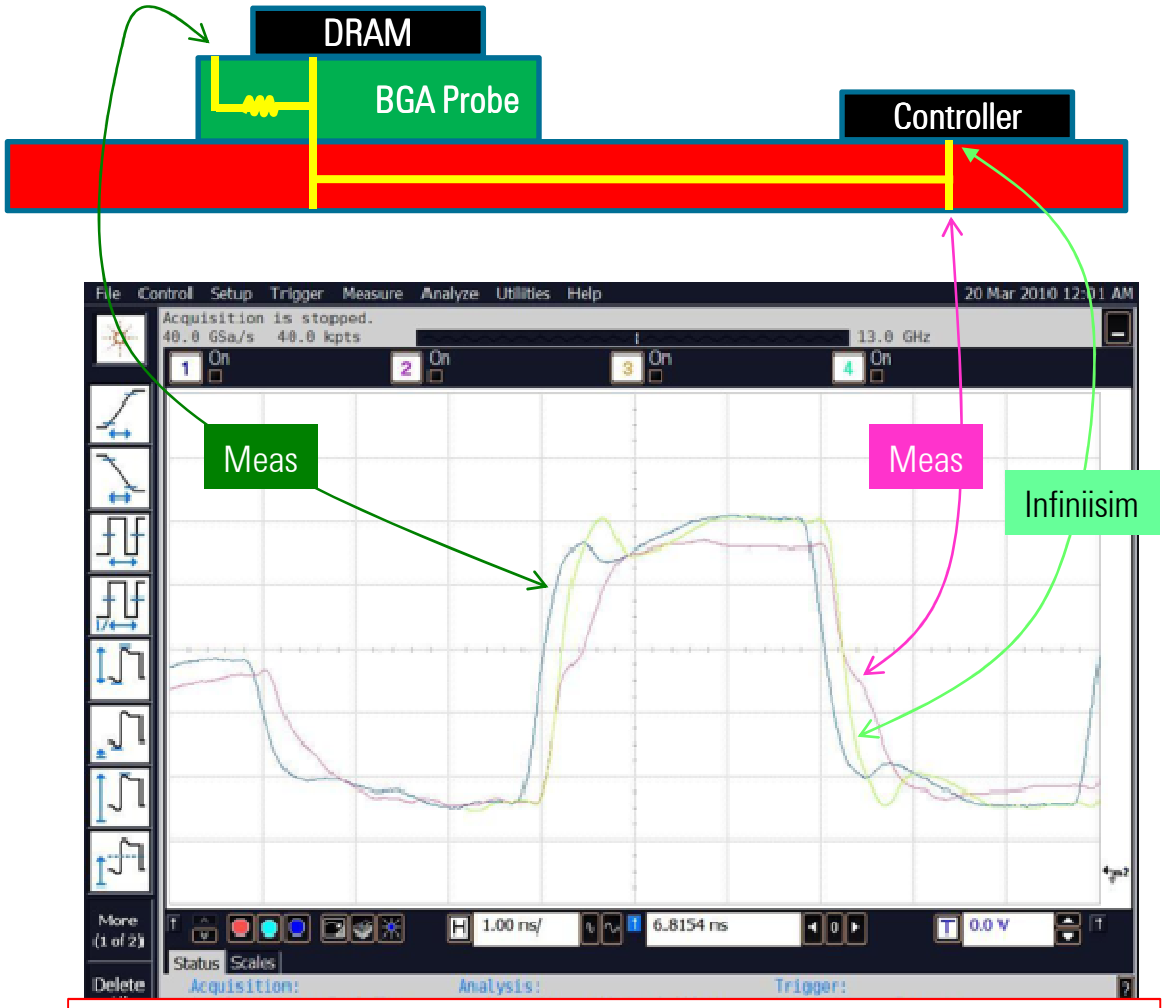
Infiniisim Settings

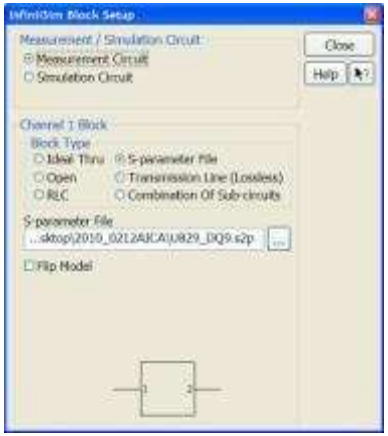


Observation point shift with Infiniisim



Observation point shift with Infiniisim

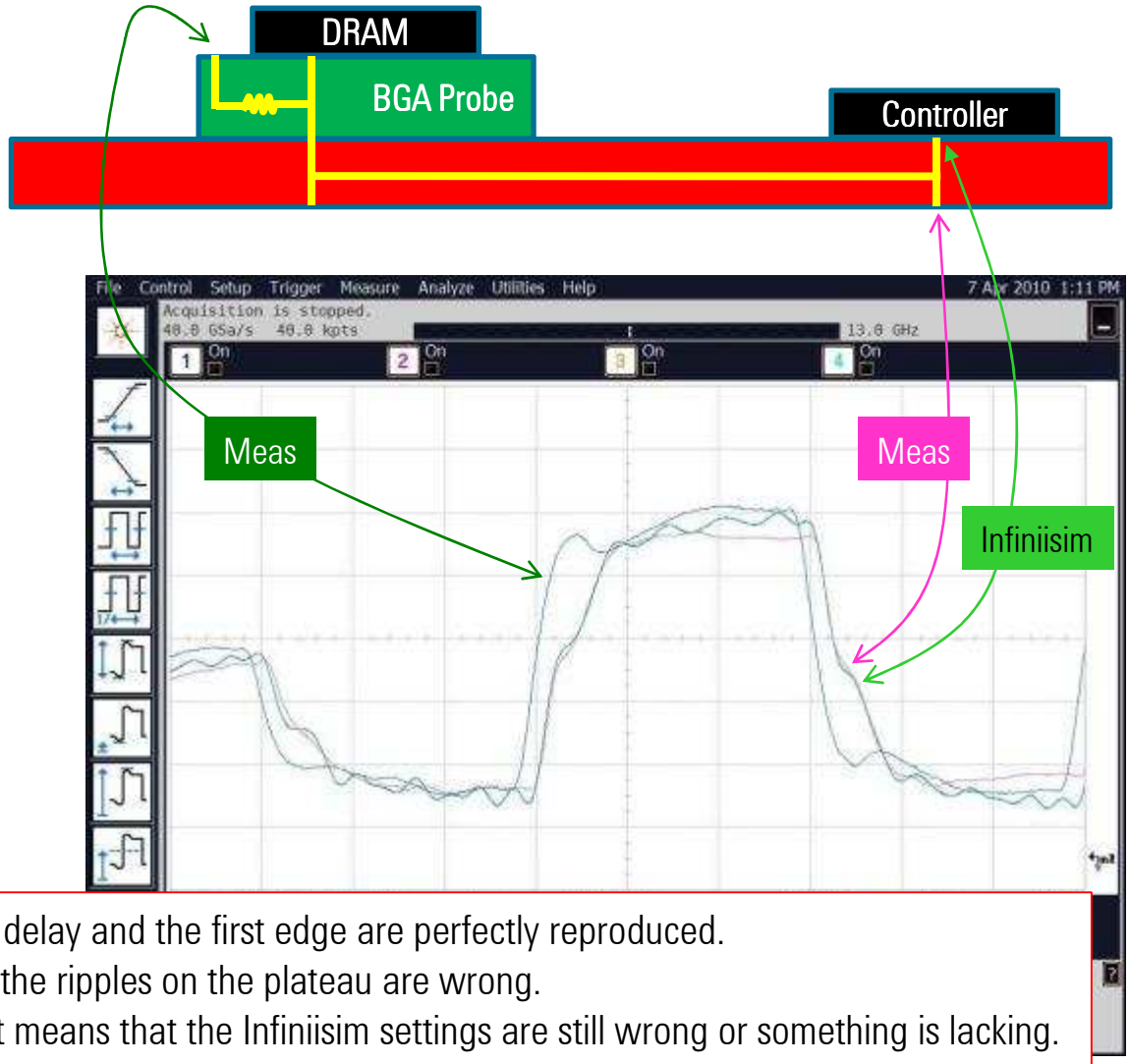


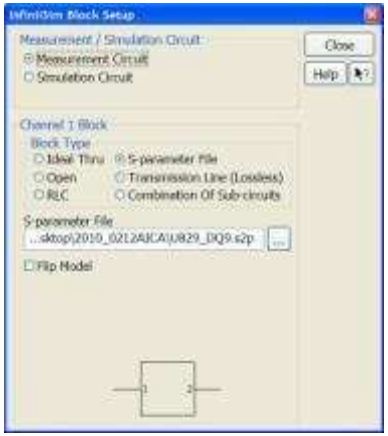


Channel S-parameters

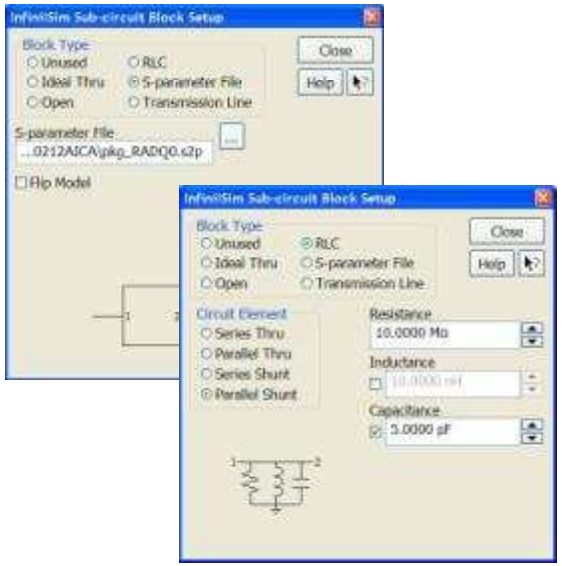
We have only applied the channel S-parameters.
The delay is good, but the reflection and amplitude aren't reproduced.
That means that it isn't enough with the channel S-parameters only.

Observation point shift with Infiniisim





Channel S-parameters



Package S-parameters
and Chip Die capacitance

The delay and the first edge are perfectly reproduced.
But the ripples on the plateau are wrong.
That means that the Infiniisim settings are still wrong or something is lacking.
That is you have to re-examine your simulation. => Let's go to Example 3

Agenda

7. Practical Examples

1. High-Speed Characterization (effect of 4.5 GHz Notch in test fixture)
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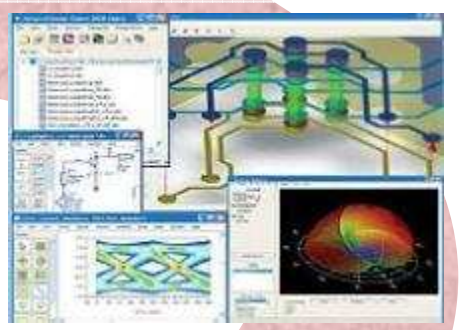
Practical example3

Simulation and Measurement Cooperation “connected solutions”

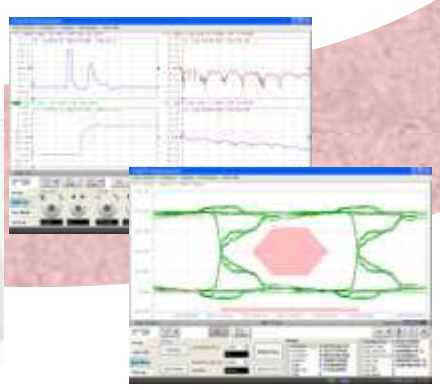
Simulation and Measurement Cooperation
“connected solutions”

Simulator (ADS)
Simulation using measured waveform
and S-parameters



Oscilloscope

New Function：Infiniisim
Simulation on the scope

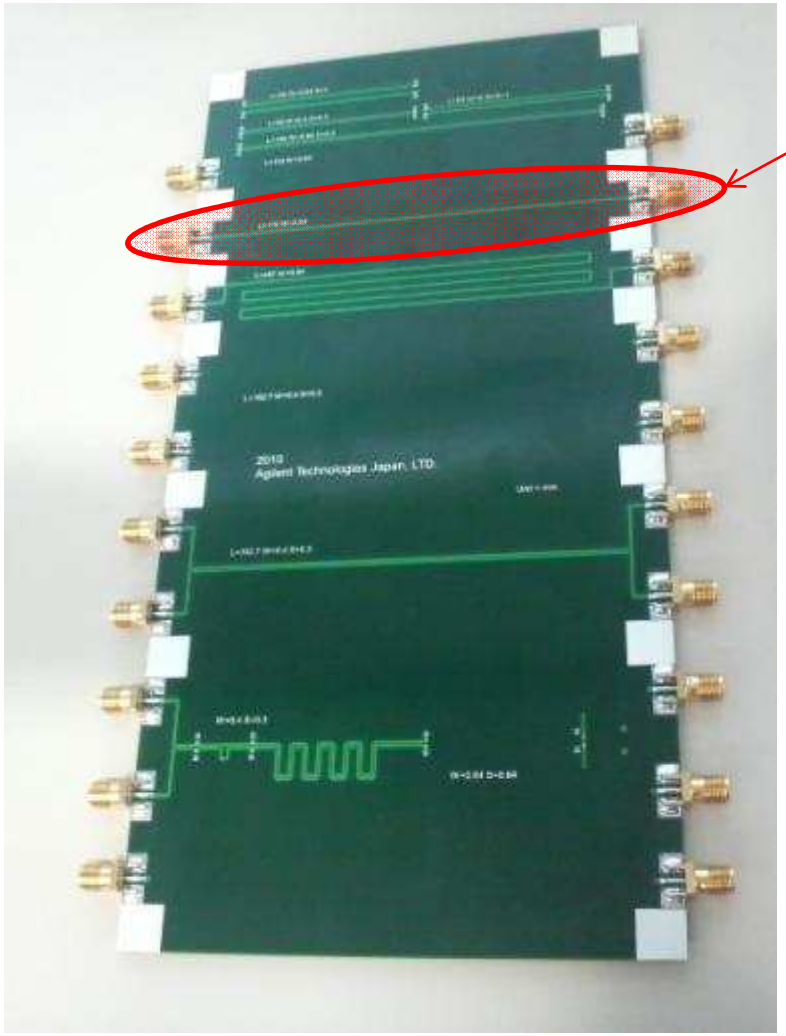


Network Analyzer

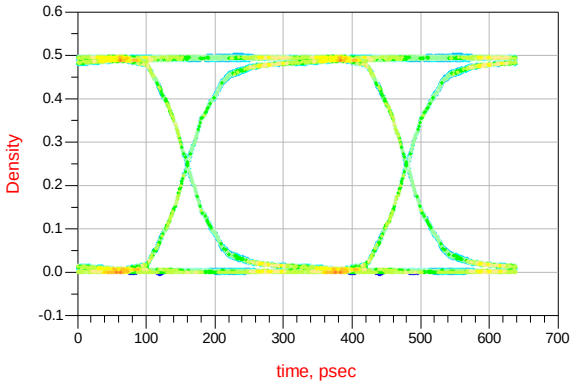
New function：ENA-TDR
Simulation on VNA

Agilent is the only one vendor delivering both simulation and measurement !

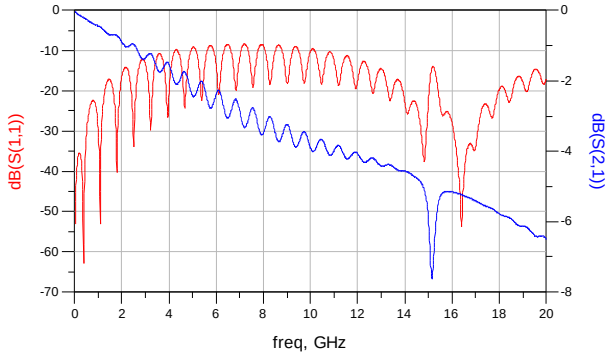
Simul and Meas, PCB board Straight Line



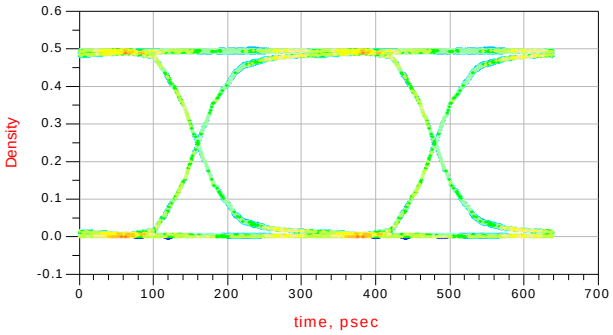
Straight line (test coupon).
We have designed it to be Z=50 Ohm.



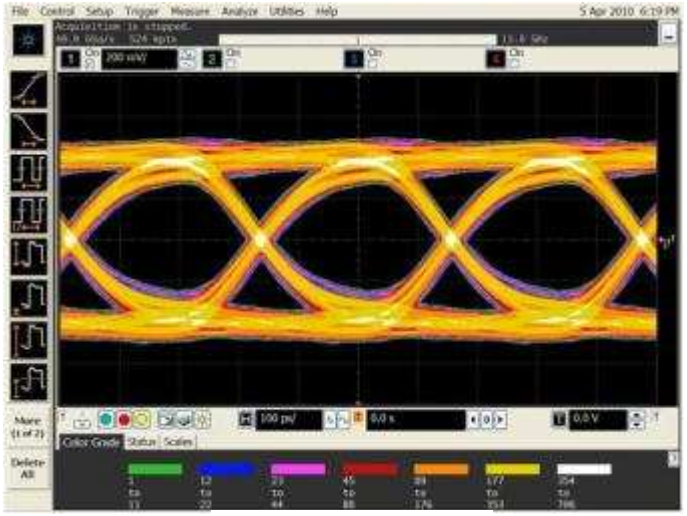
Simulated eye pattern and S-parameters at the design phase



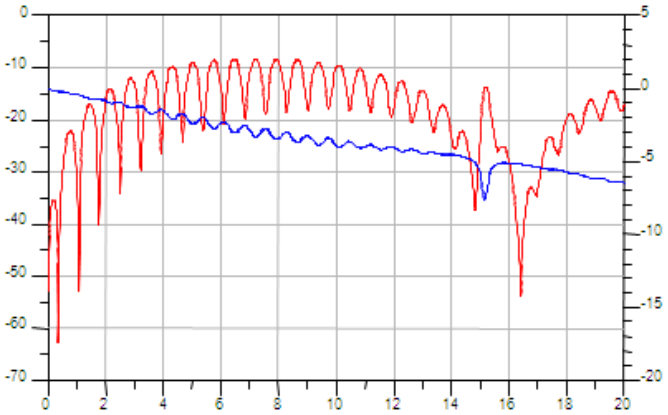
Sim and Meas, PCB board Straight Line



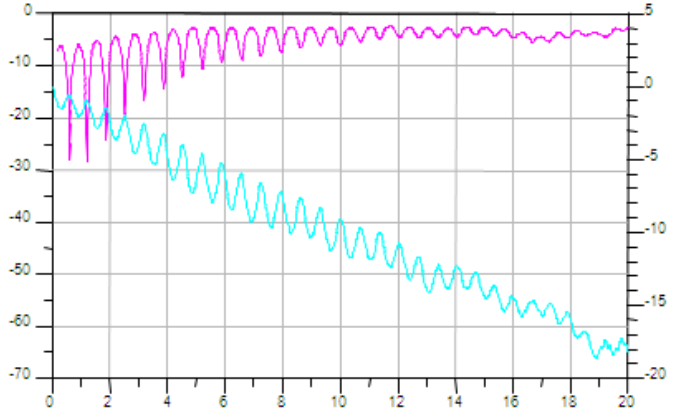
Simulated Eye at the design phase



Measured Eye

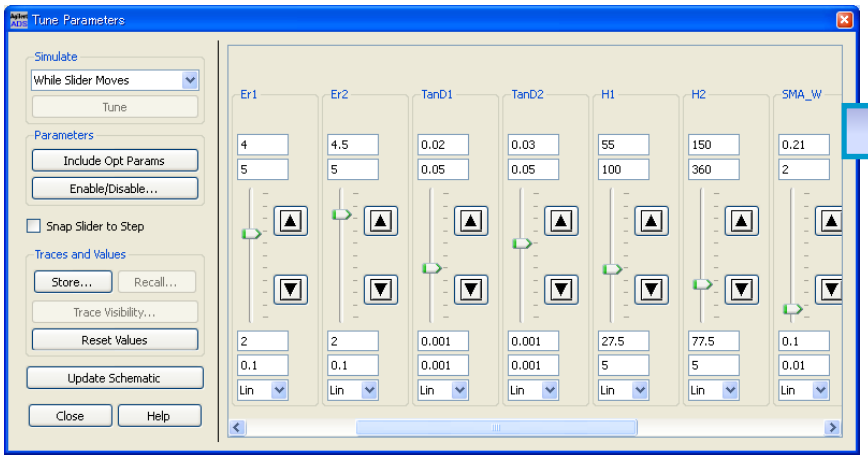


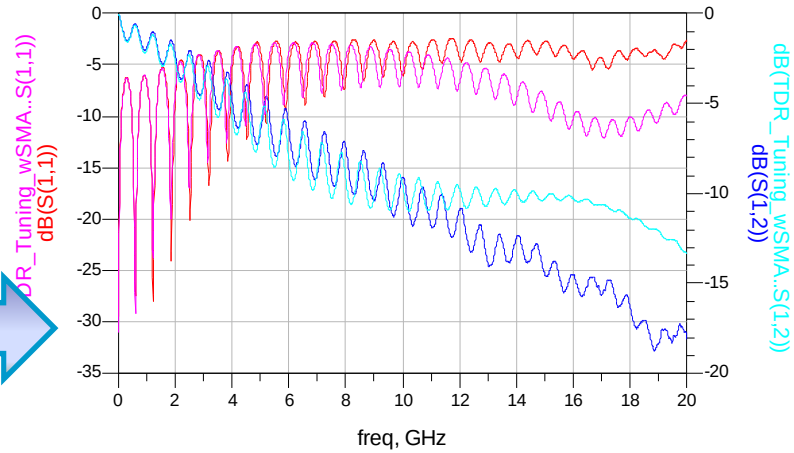
Simulated S-parameters at the design phase

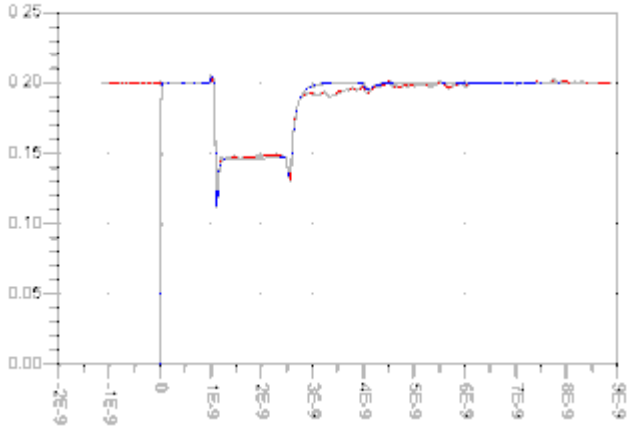


Measured S-parameters

Sim and Meas, PCB board Straight Line





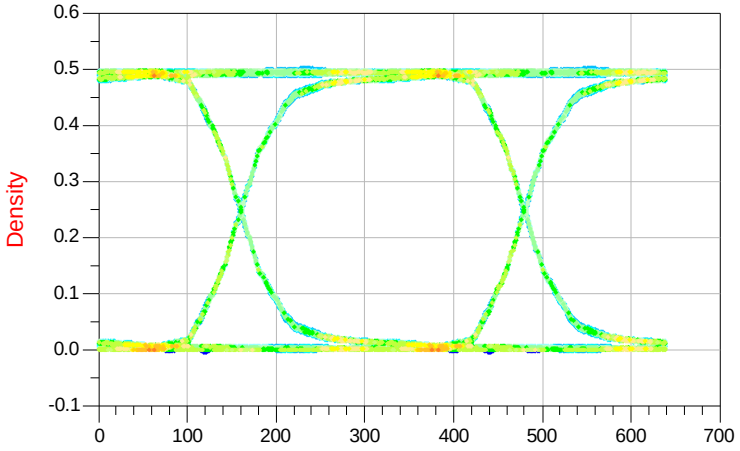


Tune PCB board parameters so that the simulated and measured S-parameters, TDR and TDT come very close.

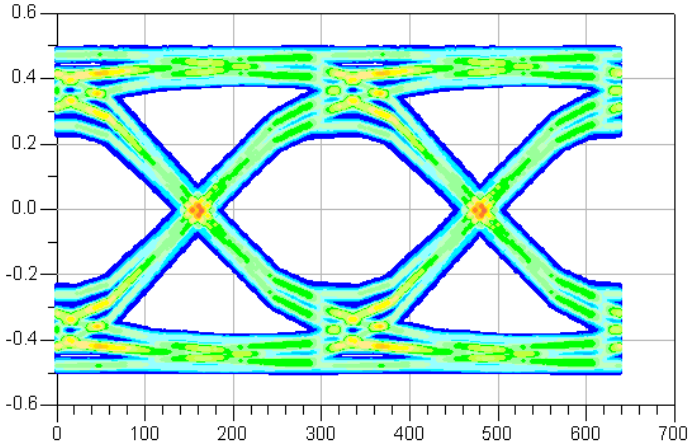
Tuning Result

er = 4.2	→	er = 4.5
h= 360um		h= 325um
tanδ = 0.015		tanδ = 0.023

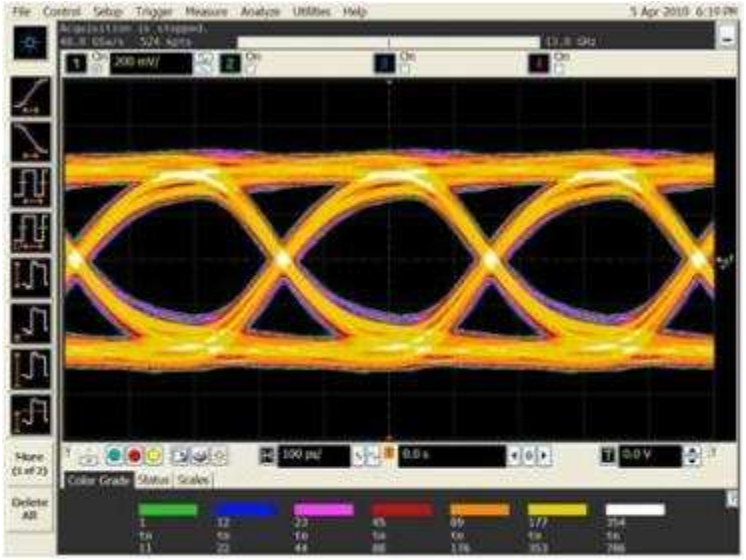
Sim and Meas, PCB board Straight Line



Simulation before tuning

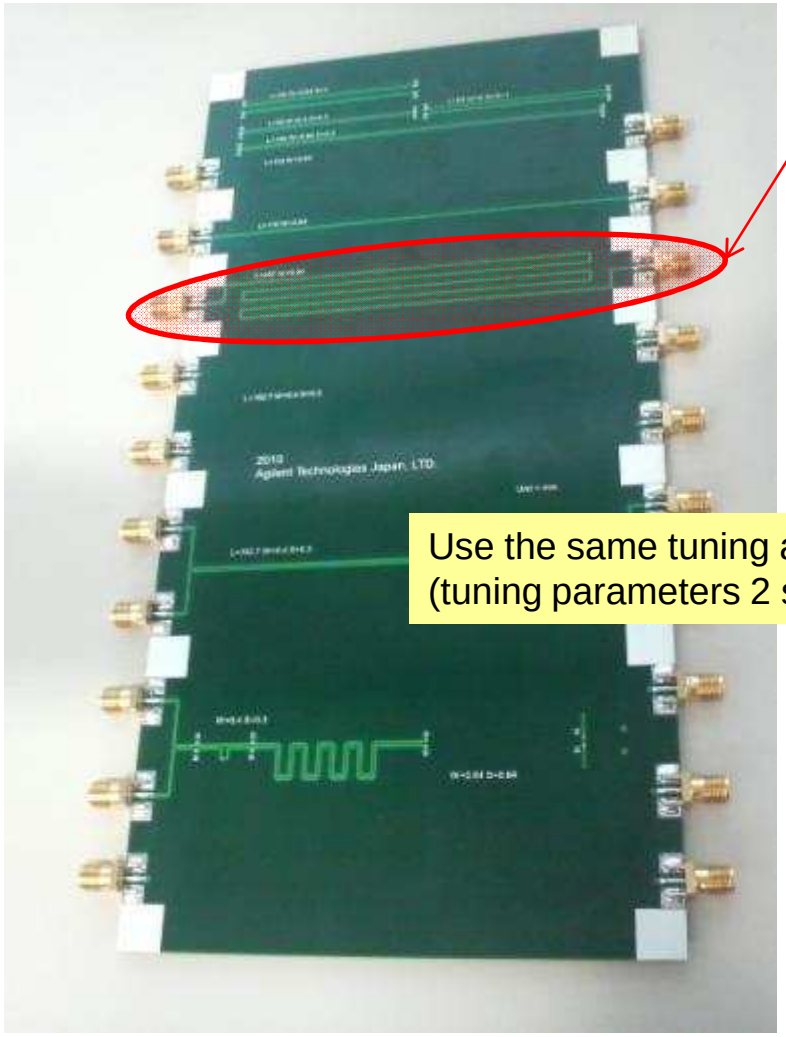


Simulation after tuning



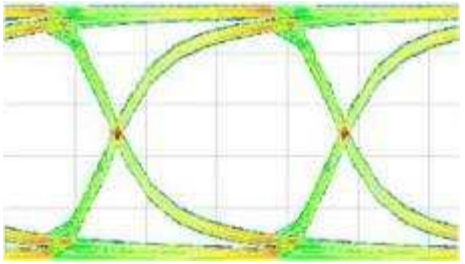
Measured Eye

Sim and Meas, PCB board Complex Channel

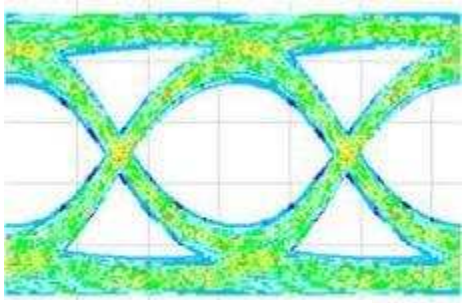


More complex channel

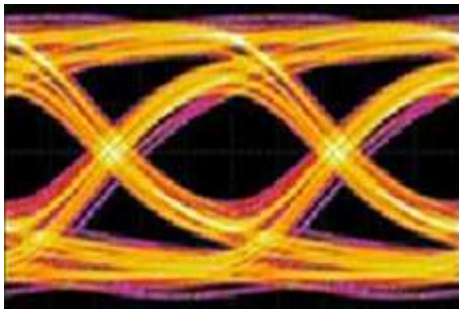
Use the same tuning as the test coupon (tuning parameters 2 slides back)



Simulation before tuning

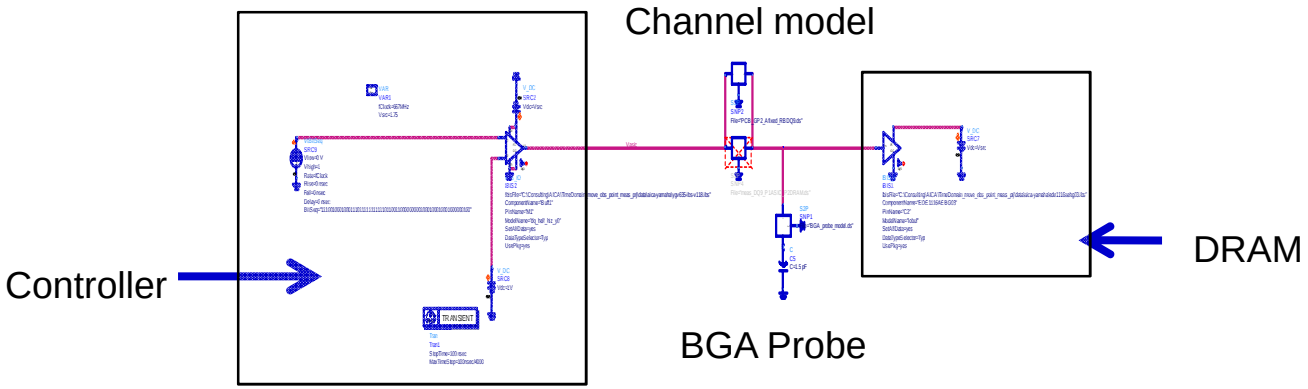


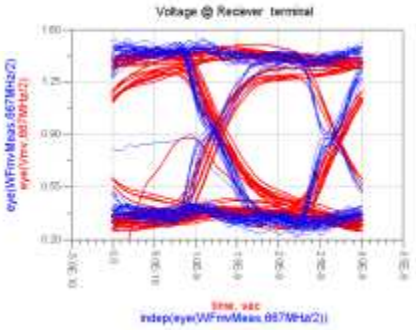
Simulation after tuning



Measured Eye

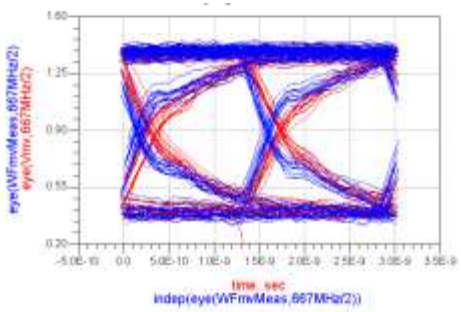
Sim and Meas, On Actual Device





Rx @Controller (READ)
- simulation
- measurement

Rx @DRAM (WRITE)
- simulation
- measurement

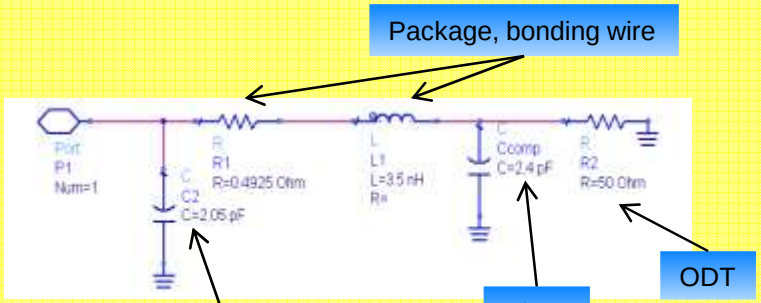


Is the channel model right ?

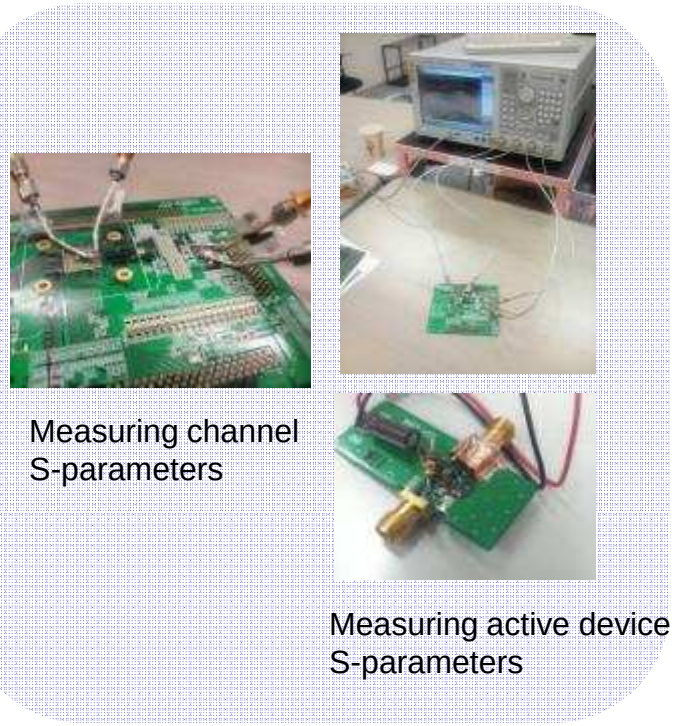
Are the devices IBIS model right ?
(Same thing for HSPICE model)

Sim and Meas, Device

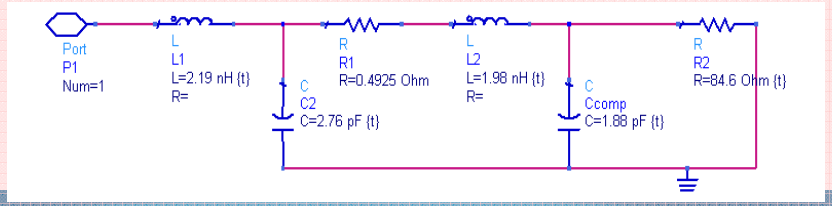
IBIS model from memory vendor



The package C seems to be 2.05pF from the sim model, but is it true ?

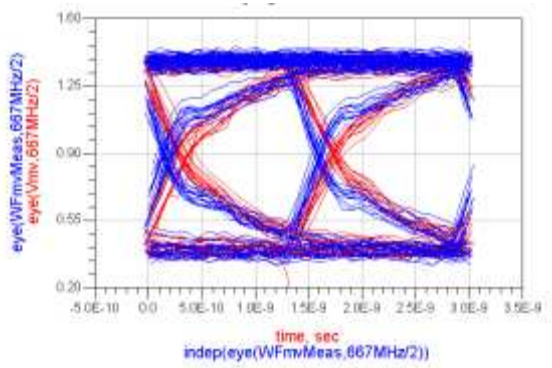


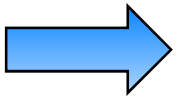
Tuned IBIS with measured result



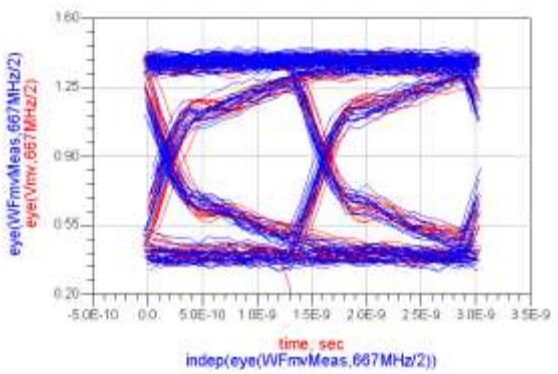
The package C should be 2.76pF to make consistent with the measured result.

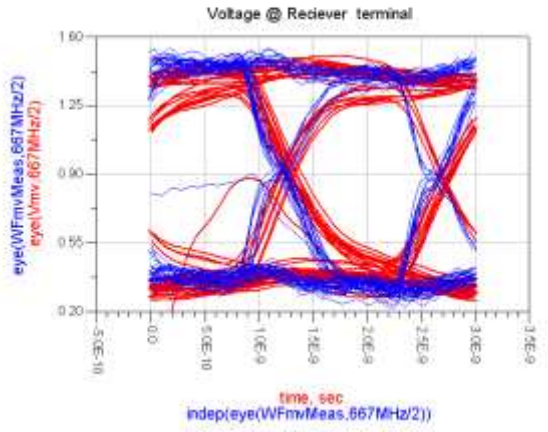
Sim and Meas, Device: now with tuned, measurement enhanced, IBIS parameter

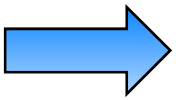




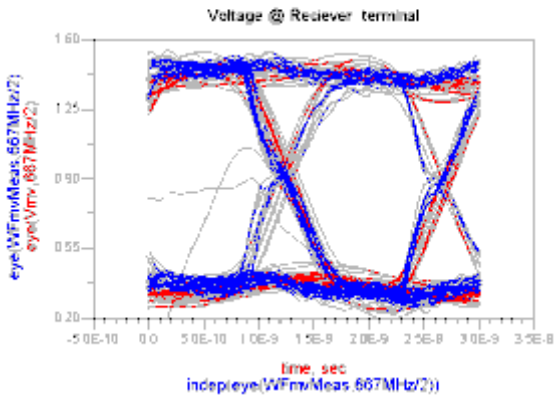
WRITE
- simulation
- measurement



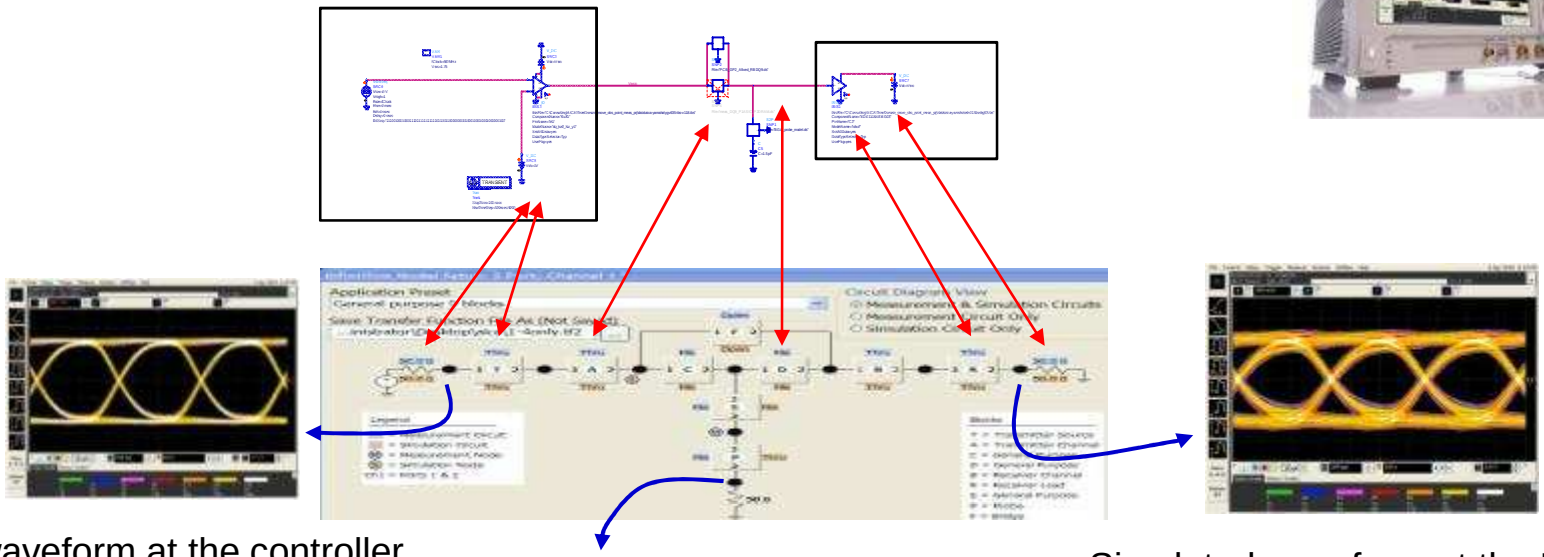




READ
- simulation
- measurement

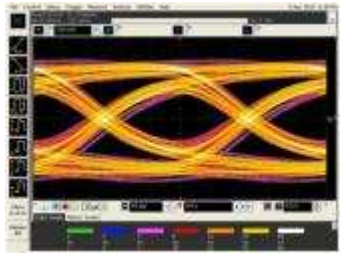


Simulation on scope



Simulated waveform at the controller

Simulated waveform at the DRAM



Measured waveform at the probing point

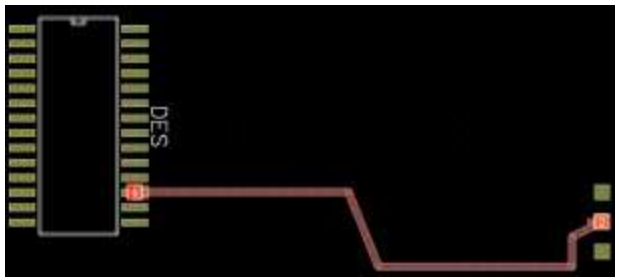
Agenda

7. Practical Examples

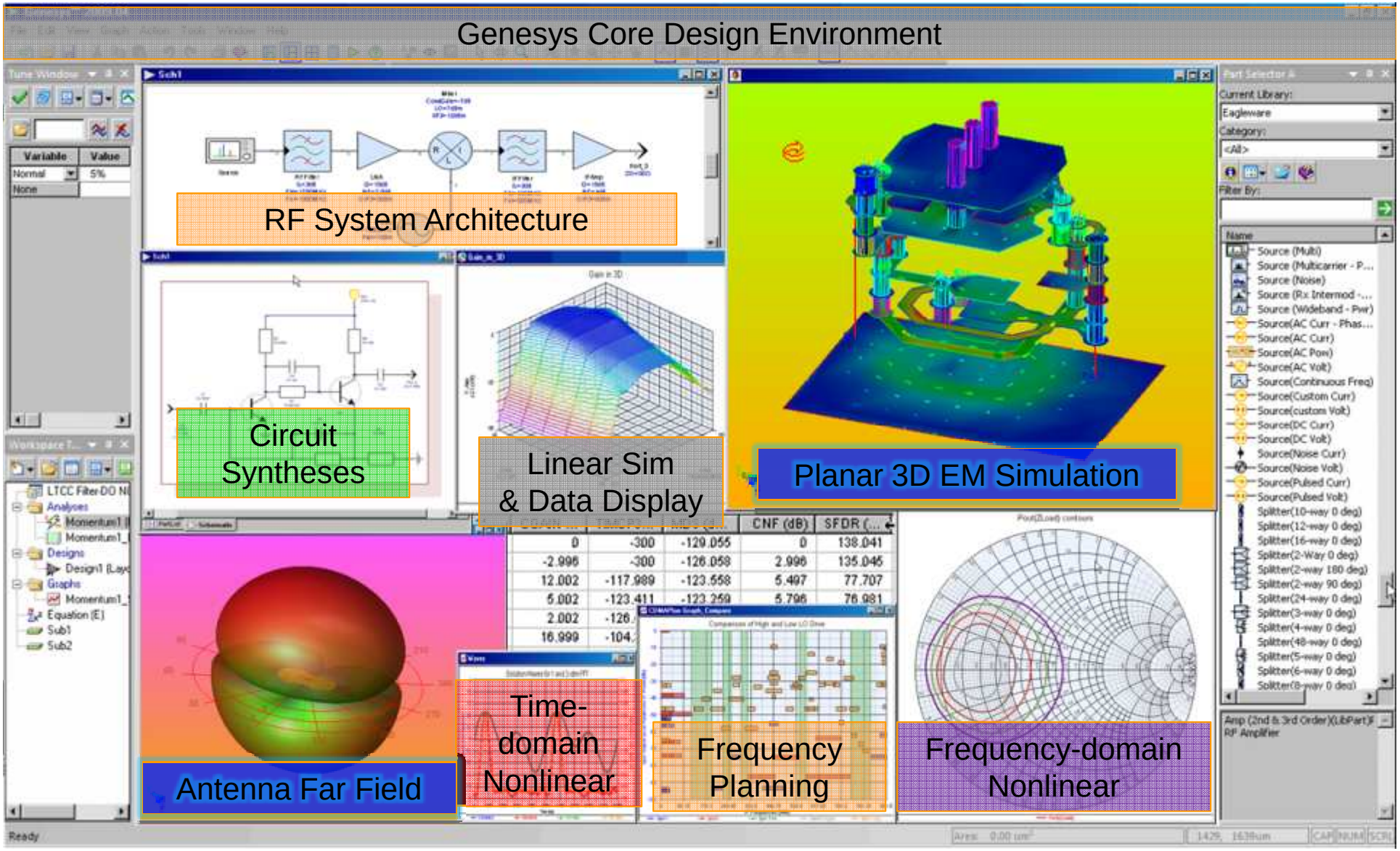
1. High-Speed Characterization (effect of 4.5 GHz Notch in test fixture)
2. BGA probe setup in infiniisim Virtual Probe
3. Tuned, measurement enhanced, IBIS parameters for DDR
4. *Creating S2P (touchstone) files from Gerber files*
5. Basic Steps for Optimizing a Serial Link
6. Serial Data Analysis Solutions: 8b10b Trigger, Decode, Search and Listing Feature
7. Small peek inside the 90.000 X 32 GHz scope

Practical example 4:
Creating S2P files from Gerber files

1. Import Layout from mechanical CAD software into Genesys or ADS
2. Inspect layer stack and ensure material properties are correct
3. Insert EM Ports and Add Momentum Planar EM simulation controller
4. Run EM simulation and Graph Results
5. Export Touchstone file to use in de-embedding network in Scope



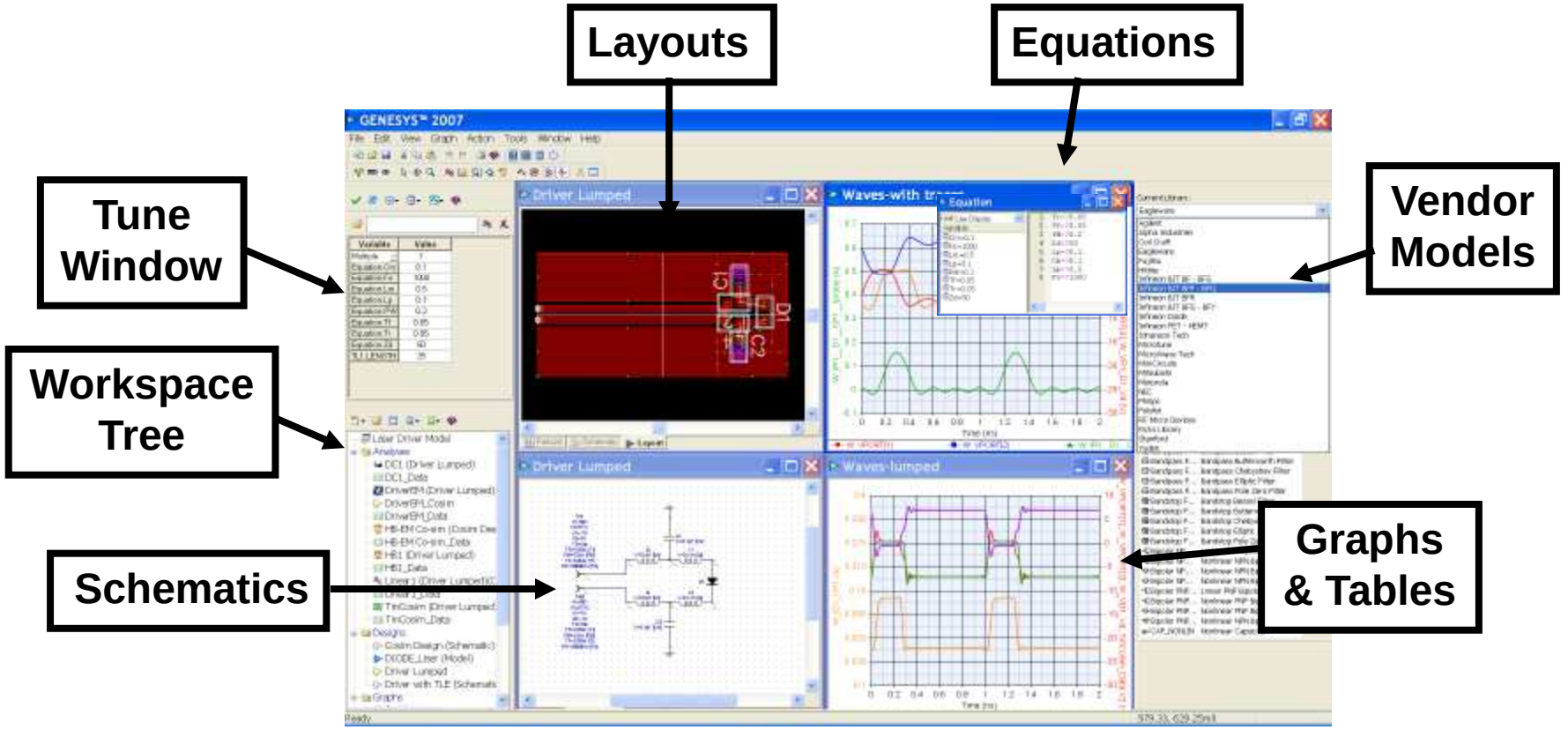
Agilent Genesys : Cost Efficient, High Performance RF/MW Board Design Software



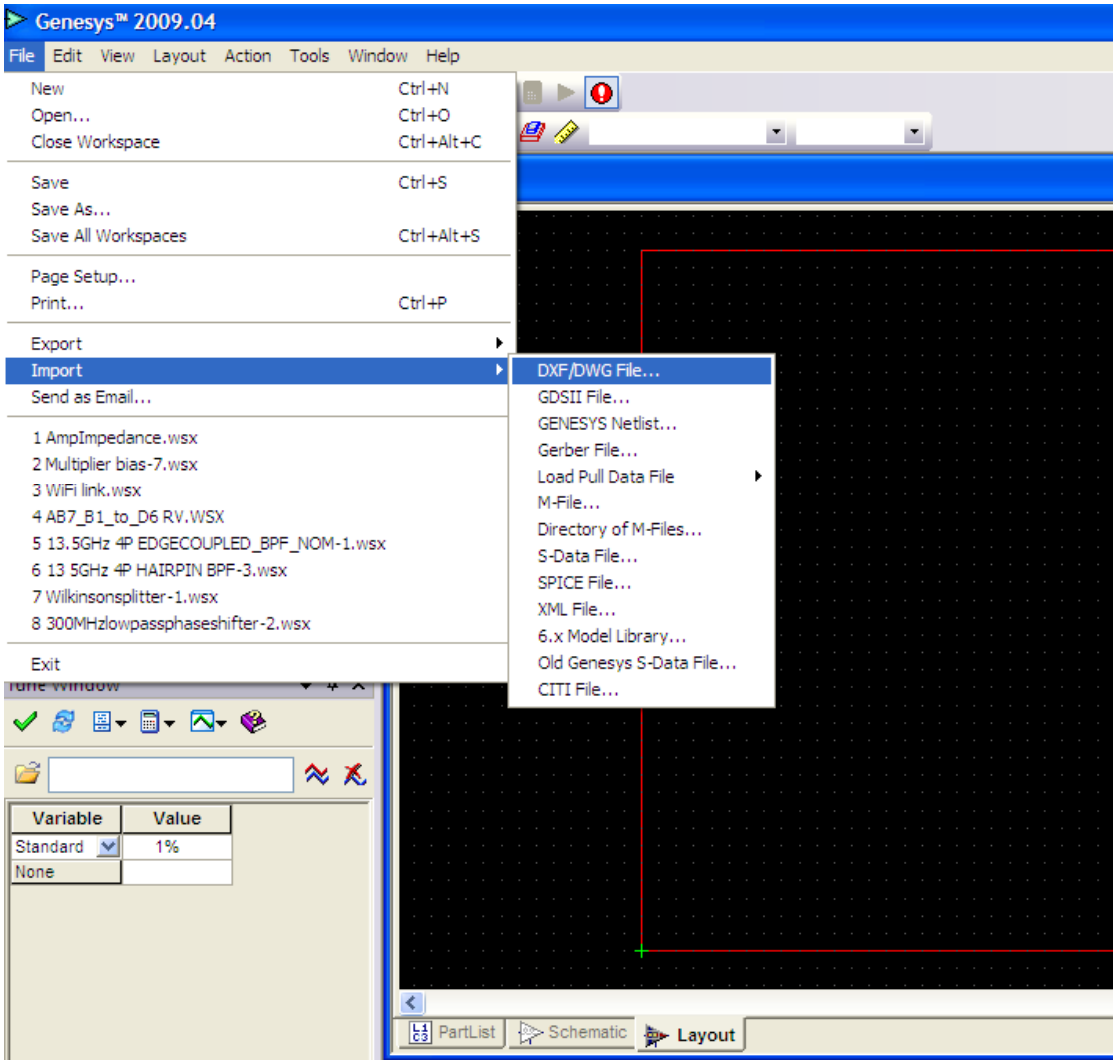
GENESYS: An Advanced User Interface

A modern, integrated Windows environment

Easy-to-use - “Hard to forget”



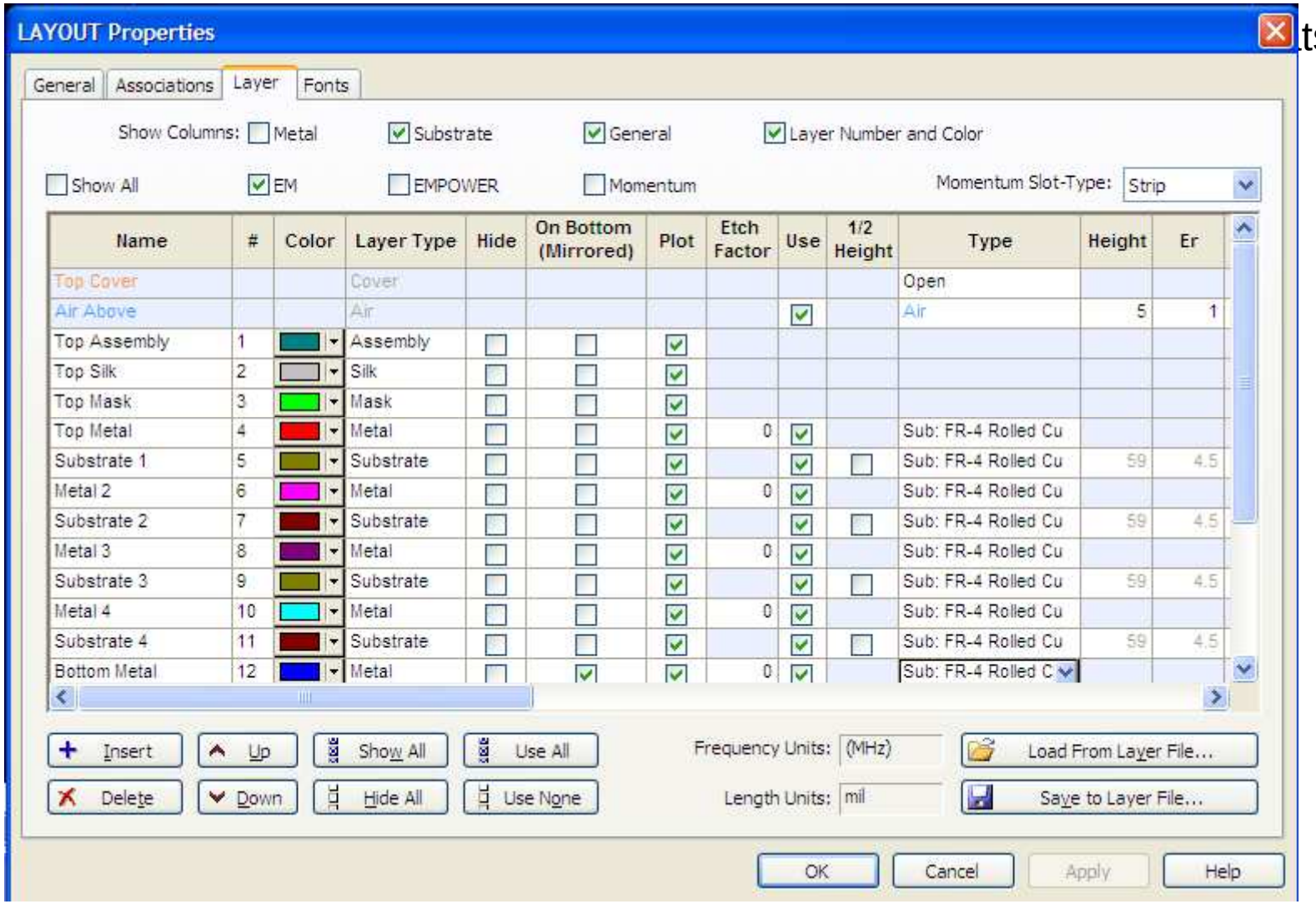
STEP 1: Import Layout from mechanical CAD software into Genesys



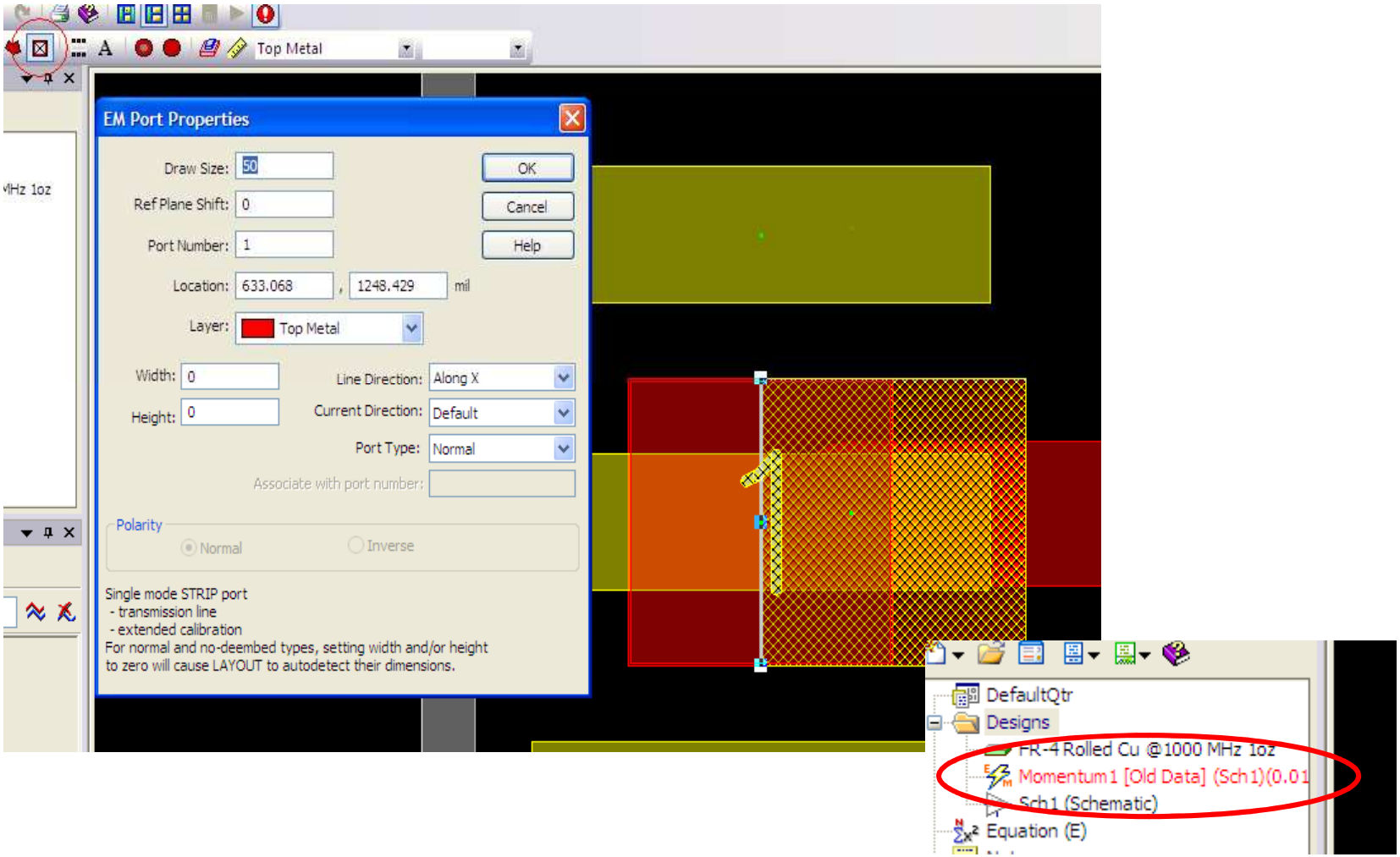
Supported File Formats for import:

- DXF DWG
- GDS II
- Gerber

STEP 2: Inspect layer stack and ensure material properties are correct



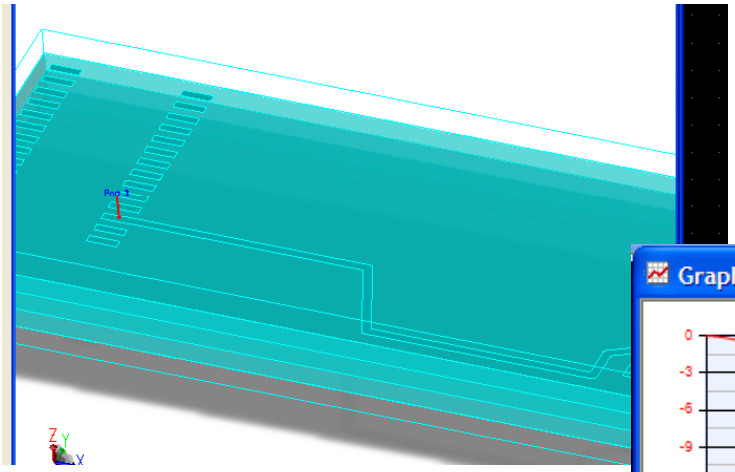
STEP 3: Insert EM Ports and Add Momentum Planar EM simulation controller



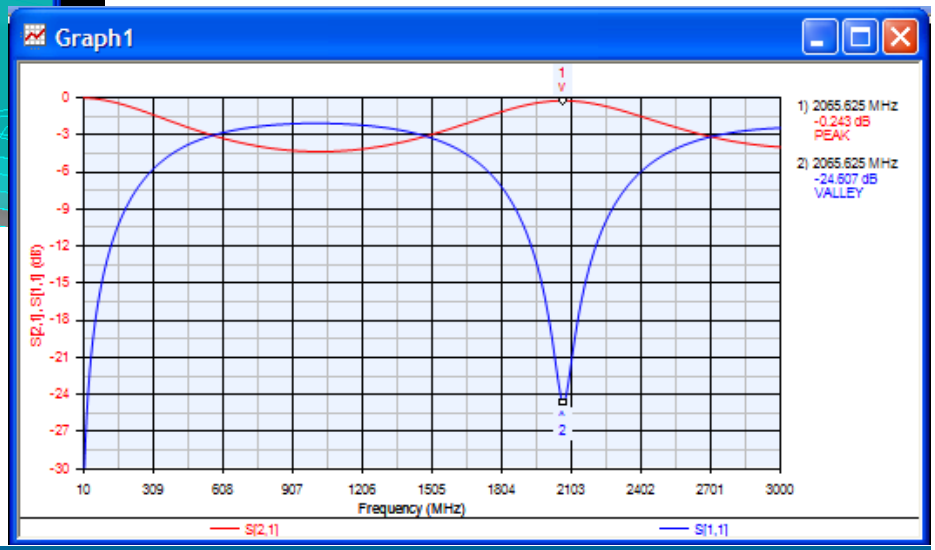
STEP 4: Run EM simulation and Graph Results

- Layout with Momentum Mesh overlay

- Layout 3D View

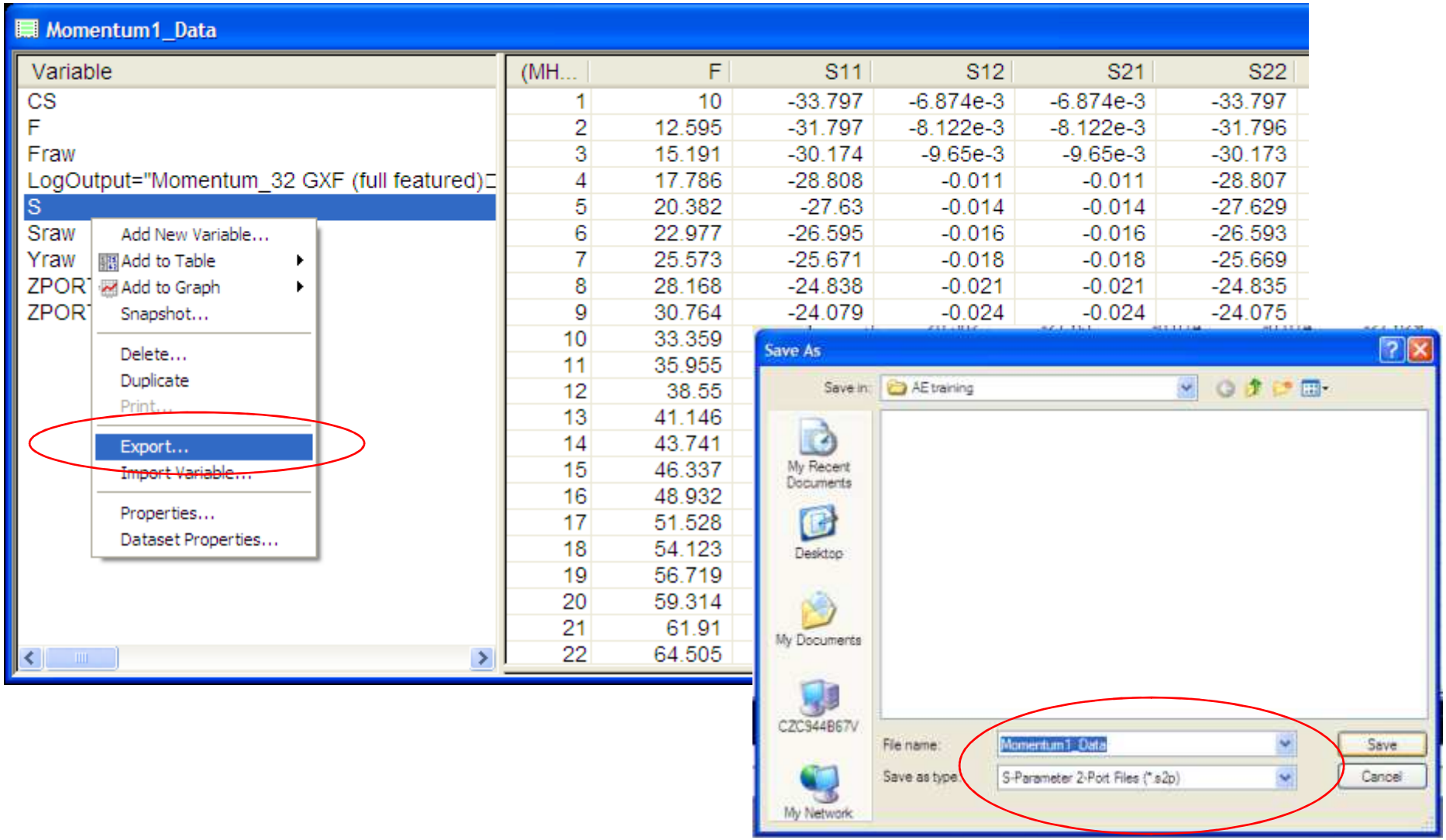


-Graph of S-parameters



Very simple to setup for accurate results. All simulation options left to default (automatic)

STEP 5: Export Touchstone file to use in de-embedding network in Scope



Agenda

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2. BGA probe setup in infiniisim Virtual Probe
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5. ***Basic Steps for Optimizing a Serial Link***
6. Serial Data Analysis Solutions: 8b10b Trigger, Decode, Search and Listing Feature

7. Small peek inside the 90.000 X 32 GHz scope

Practical example 5:
Basic Steps for Optimizing a Serial Link

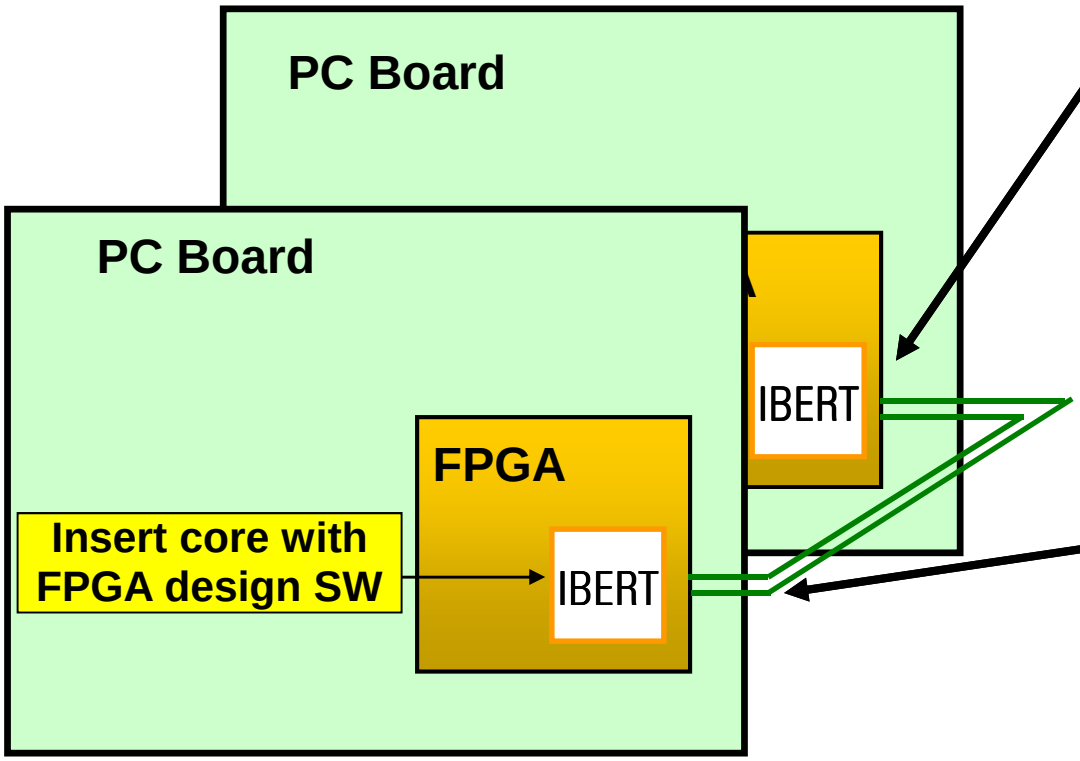
Optimizing a Serial Link

Xilinx:

Multi-Gigabit Transceivers (MGTs)

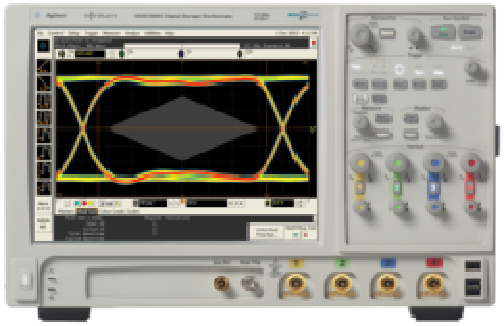
\+ IBERT Test Core

- IBERT core provides stimulus,
- Tx & Rx setting control, and
- BER measurement capability



Agilent:

Measurement instruments for analysis and optimization of signal integrity of Rocket IO signals



DSA9000 series & N5461A Equalization Analysis allows to analyze and optimize the signal integrity including automated tap optimizer for opening the eye. Graphical margin analysis via eye diagram measurements including mask templates allows to control optimization process.

N4903B BERT and N4916B De-Emphasized Signal Converter allows to generate any pre-emphasis signal.

Optimizing Rocket IO Signal Integrity

Basic Steps for Optimizing a Serial Link:

1. **Specify MGT configuration** using Xilinx ISE tools, per your design's characteristics.

2. **Specify IBERT core parameters** using Xilinx ChipScope Pro Core Generator consistent with #1 above; create IBERT core.

3. **Load IBERT core and generate serial data**.

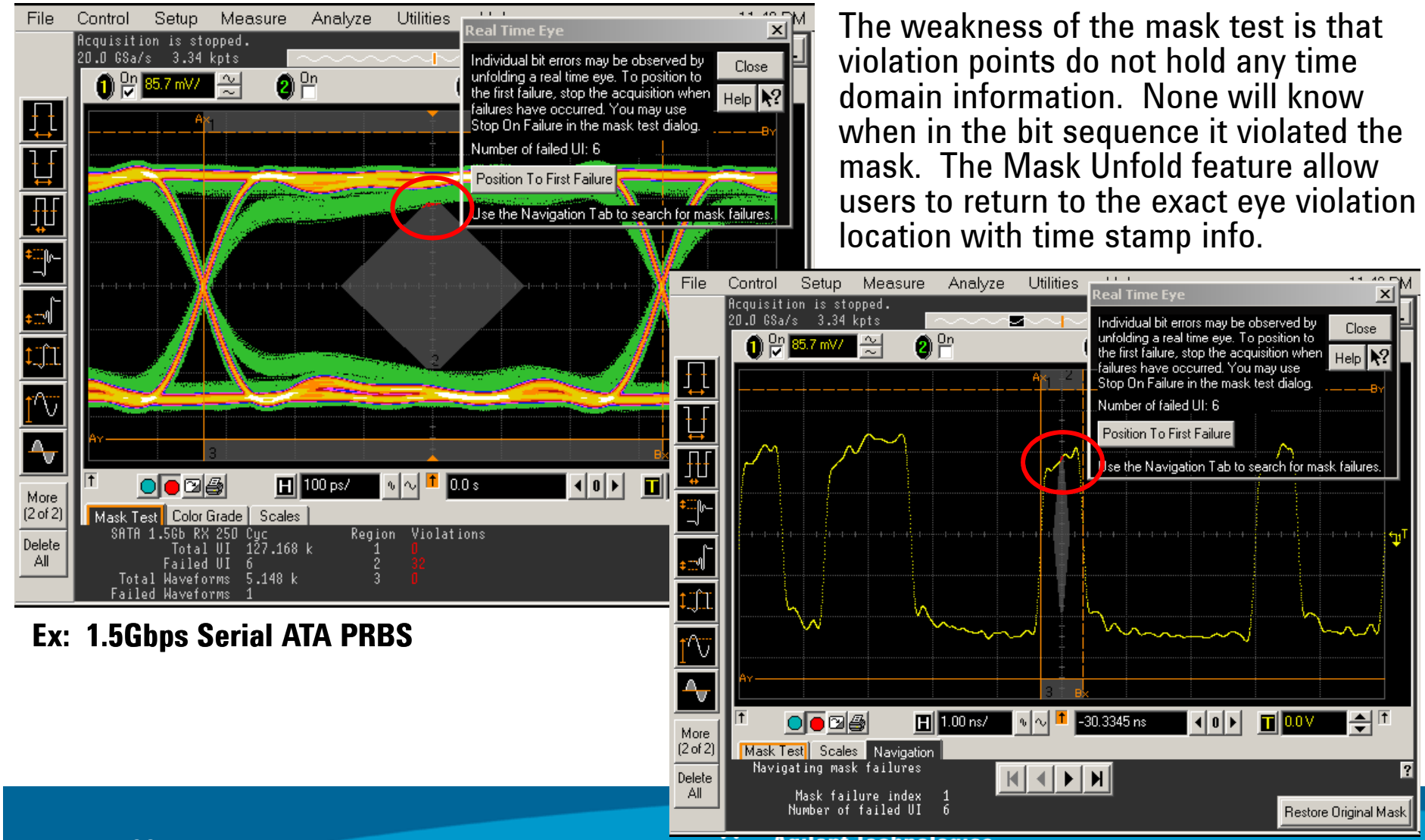
4. **Replace IBERT Tx by SerialBERT + De-Emphasized Signal Converter and optimize pre-emphasis** controlled by BER measurement in IBERT Rx or JBERT N4903B. Alternatively, the optimal pre-emphasis setting could be controlled by using the eye opening measurement in the Realtime Scope 90000 series. The results of the optimization taps for Pre-emphasis could directly be used in the Multi-Gigabit Transceivers (MGT) of Tx.

5. **Replace IBERT Rx by Scope and determine the optimal tap values for equalizer** in the Rx using automated tap finder routine in the N5461A Equalization Software. The result of optimal equalization could be controlled by eye opening measurement in the Realtime Scope 90000 series at Rx. The optimal settings for equalization taps could directly be used in the MGT of the Rx.

Practical example 6
Serial Data Analysis Solutions

1. Mask Unfold Feature
2. 8b10b Trigger, Decode Feature,
3. Search and Listing Feature

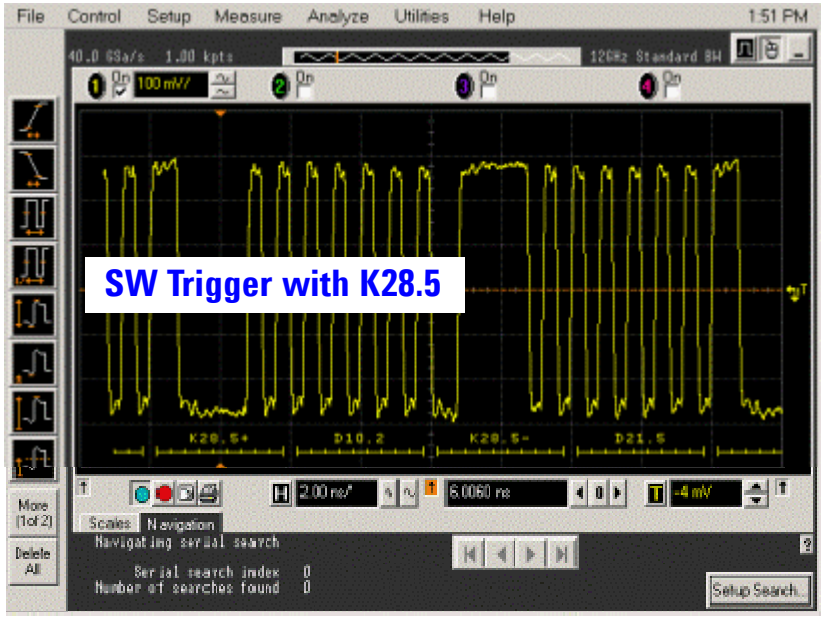
Serial Data Analysis Solutions
Mask Unfold Feature

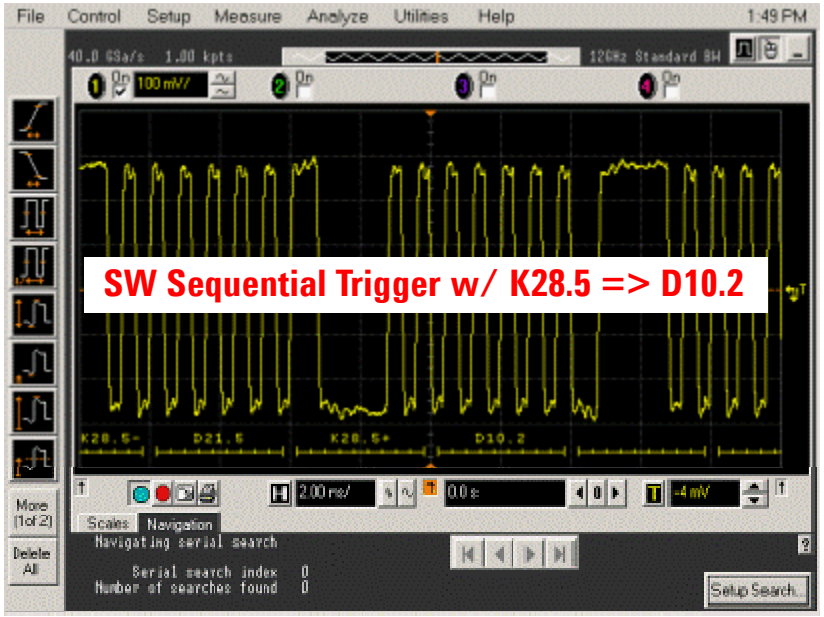


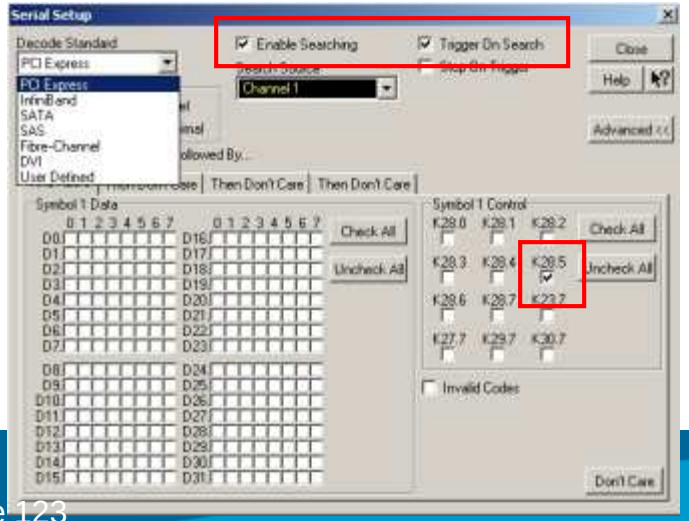
Ex: 1.5Gbps Serial ATA PRBS

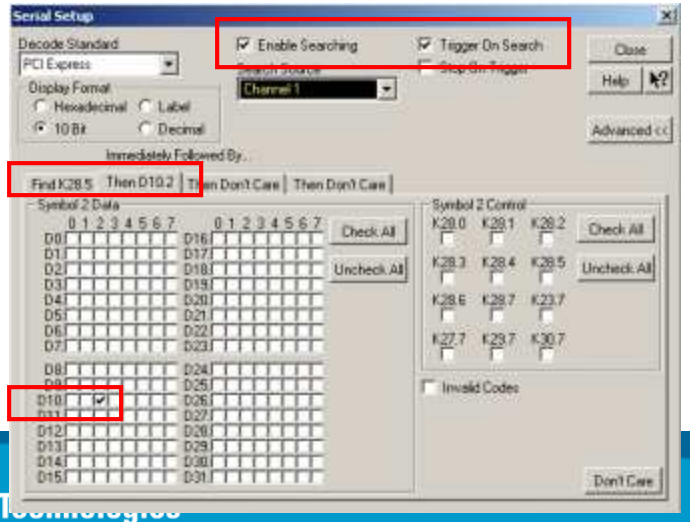
The weakness of the mask test is that violation points do not hold any time domain information. None will know when in the bit sequence it violated the mask. The Mask Unfold feature allow users to return to the exact eye violation location with time stamp info.

Serial Data Analysis Solutions: 8b10b Trigger, Decode, Search and Listing Feature









Agilent Technologies

Serial Data Analysis Solutions:
8b10b Trigger, Decode, Search and Listing Feature

Please refer to application note 5989-0108EN for more detail

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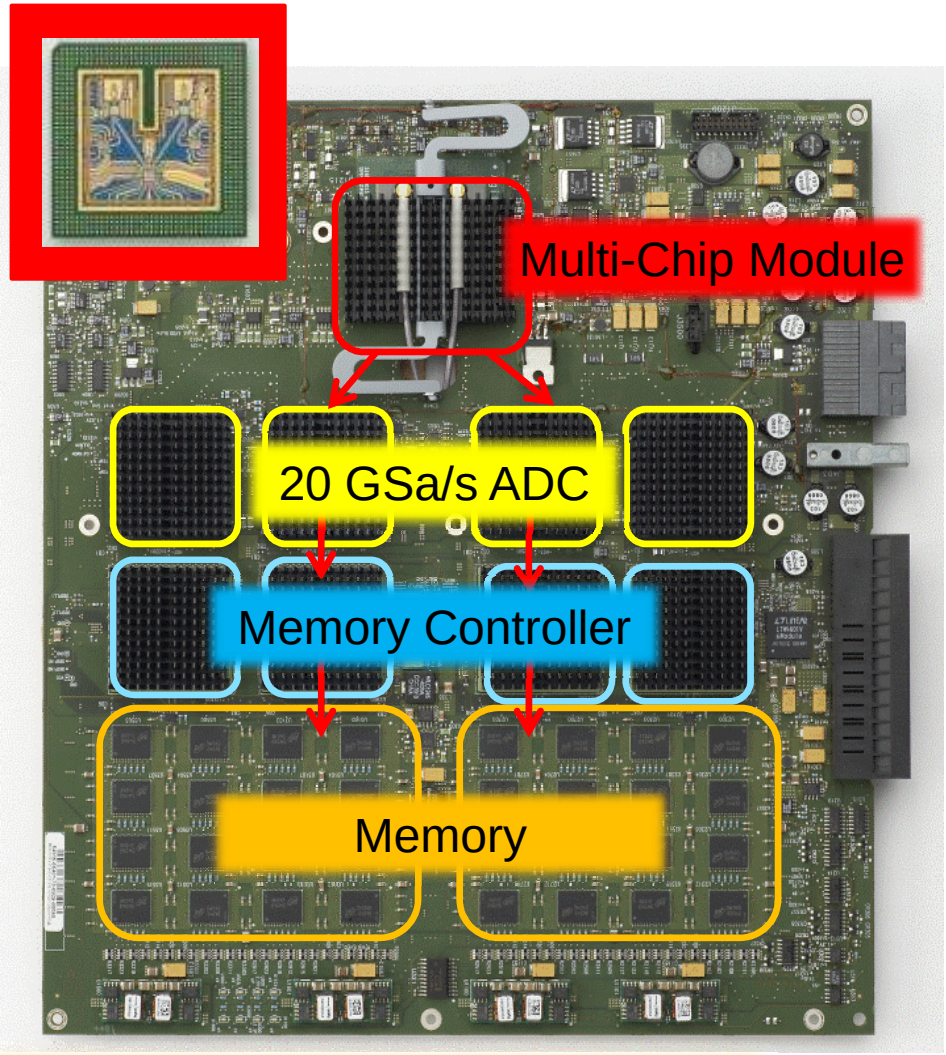
90.000X Example of a good Signal Integrity Design

What it takes to deliver:

► An excellent IC process with high bandwidth capacity and low parasitic capacitance for low noise, customized for test for measurement

► IC package technology for isolation and reliability

► Pure signal path with other high performance components



Technology investments deliver the highest measurement accuracy.

True Analog Bandwidth Delivers …

High Measurement Accuracy

The 90000 “X” Series represents Agilent’s largest oscilloscope investment in its history

The new multi-chip module has five new chips all developed in an Agilent proprietary (200 GHz F_T) InP chip process

New packaging technology enables the InP chips to be embedded in the packaging to minimize wire bond and inductance

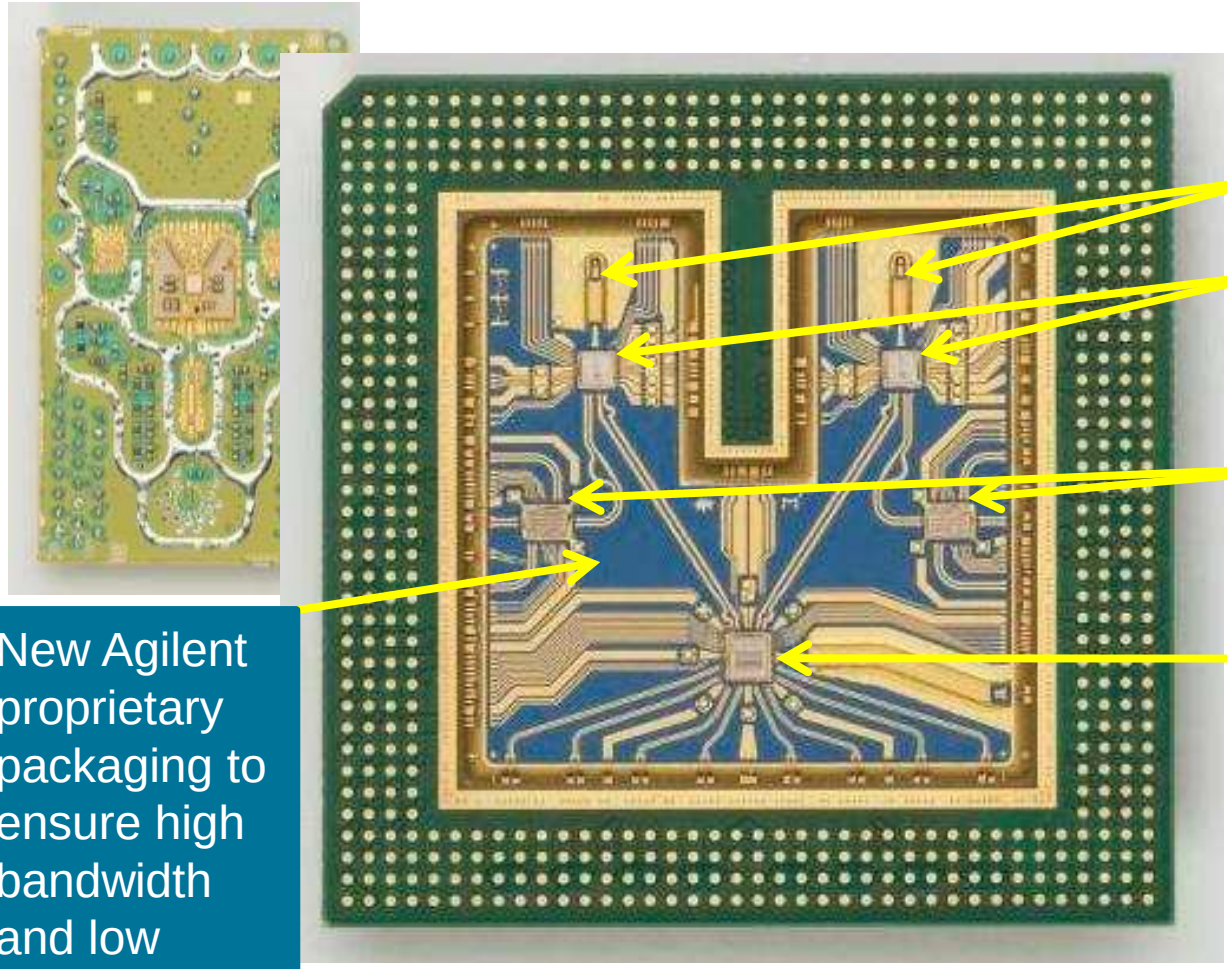
High F_T, BS vias, high resistivity substrates enable flatter response to higher frequencies

Investment and Technology Results in Analog Bandwidth to 32 GHz without DSP boosting or Frequency Interleaving!

True Analog Bandwidth that Delivers …

High Measurement Accuracy

The Evolution of the Infiniium Front End



Quasi-coax to ensure signal shielding

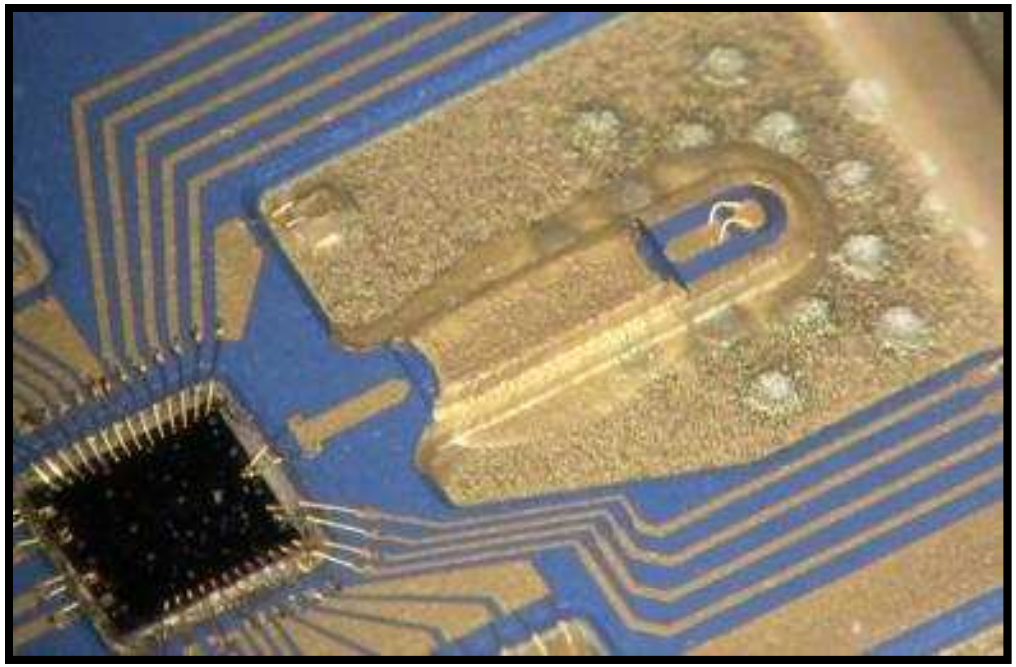
Industry's fastest preamplifier (32 GHz)

Industry's fastest edge trigger chip (>20 GHz)

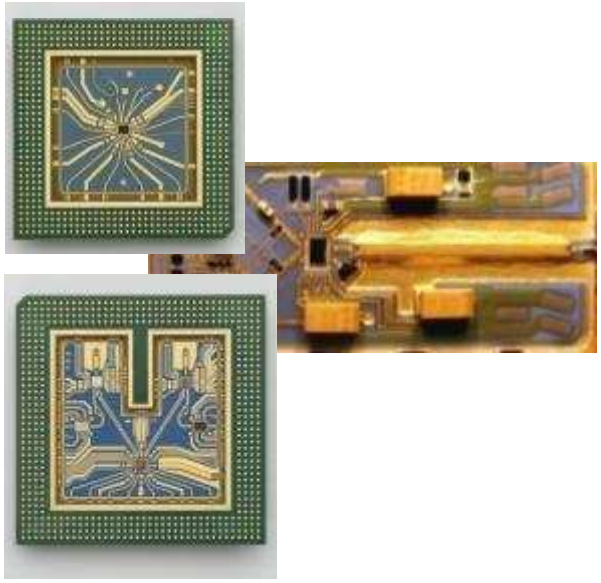
New 32 GHz sampler with sample and filter technology

New Agilent proprietary packaging to ensure high bandwidth and low noise

Signal Integrity Example: Coax on PCB



True Analog Bandwidth Delivers…
High Measurement Accuracy



The Tchnology Investment to Reach High Bandwidth

- ✓ Agilent proprietary fabrication facility
- ✓ Agilent proprietary Indium Phosphide chip process
- ✓ Agilent proprietary packaging technology
- ✓ Agilent proprietary preamplifier design
- ✓ Agilent proprietary probe design
- ✓ Agilent proprietary sampling chip design
- ✓ Agilent proprietary board design

Agenda

1. Introduction
2. Eye Masks & TDR with an Network Analyzer
3. Pre-Emphasis
4. Equalization
5. Virtual probing / De-Embedding
6. Probing Hardware
7. Practical examples
8. ***Summary***

Questions?