

PCLK=53.52MHz @ (53.52MHzx35bit) payload =1.87Gbps

Total Bandwidth: 53.52MHz x 28 bit = 1.498 Gbps ?

Symbol Clock is 53.52MHz ?

100Ω Balanced individually shielded twisted pair w/drain

Output	B7	B6	B5	B4	B3	B2	B1	G7	G6	G5	G4	G3	G2	G1	R7	R6	R5	R4	R3	R2	R1	B5	B4	B3	B2	B1	B0	
1 st picture	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
2 nd picture	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Test picture

Output	RXOUT3 +/-				RXOUT2 +/-				RXOUT1 +/-				RXOUT0 +/-														
	B	G	G	R	B	G	G	R	B	G	G	R	B	G	G	R											
1 st picture	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
2 nd picture	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
CLKIN frequency @ Frame Rate= 60Hz	fcik	20	53.52	71	Mhz
Horizontal Display Area	thd	-	1024	-	CLKI
1 Horizontal Line	th	1074	1104	1400	
HSD Blanking	thb+thfp	50	80	376	N
Vertical display area	tvd	-	768	-	H
1 Vertical Line	tv	778	808	868	
VDS Blanking	tvb+tvfp	11	40	100	

TFT panel timing

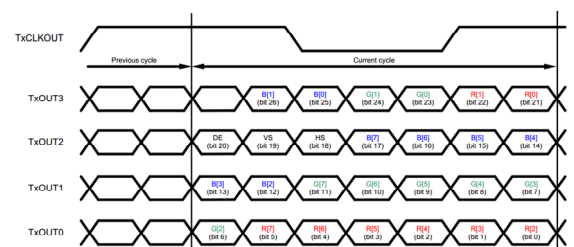


Figure 19. 24-bit Color FPD-Link Mapping: LSBs on TxOUT3 (MAPSEL=L) DS90UH928Q Out