

TLK6002 HSPICE Model Guide

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This document describes the HSPICE models for the TLK6002 device. There are four models within this release, a HSTL transmitter, a HSTL receiver, a serial line driver and a serial termination. The release contains this document and files in the following subdirectories.

- models
- pvt_includes
- include
- sample_tests
- fr4_models

models subdirectory

The models subdirectory contains the model statements for all of the devices used in the design. Files have been included for nominal, weak and strong models.

pvt_includes subdirectory

The HSTL driver and receiver in the TLK6002 are connected to a controller that tunes out process, voltage and temperature variations using an external resistor. Since the tuning circuitry represented such a large portion of the HSTL buffers and the adaptation required 2.5us of simulation, the tuning has been precomputed at a wide range of conditions and the associated circuitry has been removed to speed up link simulations. Therefore it is required when simulating the parallel interface to use one of the files in this directory to define the environmental conditions.

All files in this directory are of the form process_temp_vddq_dvdd.hsp

- process can be one of three values: nominal, strong, weak
- temp can be one of m40c, 0c, 25c, 70c, 85c, 105c or 125c
- vddq can be one of vddq1p4, vddq1p5, vddq1p6, vddq1p7, vddq1p8, vddq1p9
- dvdd can be one of dvdd1p0, dvdd0p95 or dvdd1.05

include subdirectory

The include subdirectory contains the four I/O's that are included in this release.

tlk6002_txserial.inc

The file, tlk6002_txserial.inc, contains the serial output driver for the TLK6002. This buffer is capable of operating up to 6.25Gbps.

Port	Description
txp_ball	Positive output
txn_ball	Negative output
clk	Clock with period equal to 2UI
clkb	Complement of clk
deven	Deven and dodd specify the data two be transmitted. These signal

dodd	must transition on the falling edge of clk. Deven is transmitted first.
swing_reg2p3_3	Swing control equal to MDIO register 2.3
swing_reg2p2_2	Swing control equal to MDIO register 2.2
swing_reg2p1_1	Swing control equal to MDIO register 2.1
swing_reg2p0_0	Swing control equal to MDIO register 2.0
twpre_reg2p7_3	TWPRE control equal to MDIO register 2.7
twpre_reg2p6_2	TWPRE control equal to MDIO register 2.6
twpre_reg2p5_1	TWPRE control equal to MDIO register 2.5
twpre_reg2p4_0	TWPRE control equal to MDIO register 2.4
twpost1_reg2p12_4	TWPOST1 control equal to MDIO register 2.12
twpost1_reg2p11_3	TWPOST1 control equal to MDIO register 2.11
twpost1_reg2p10_2	TWPOST1 control equal to MDIO register 2.10
twpost1_reg2p9_1	TWPOST1 control equal to MDIO register 2.9
twpost1_reg2p8_0	TWPOST1 control equal to MDIO register 2.8
vddt	Analog supply (1.0V +/- 5%)
vddr	Analog supply (nominal 1.5 or 1.8 +/- 0.1V) Same as HSTL.
vssa	Analog Ground

tlk6002_rxserial.inc

The file, tlk6002_rxserial.inc, contains the serial termination for the TLK6002.

Port	Description
rxp_ball	Positive input
rxn_ball	Negative input
vddt	Analog supply (1.0V +/- 5%)
vssa	Analog Ground

tlk6002_hstl_rd.inc

The file, tlk6002_hstl_rd.inc, contains the HSTL output buffer used to drive the RDA and RDB buses. As described earlier, the circuitry to implement PVT correction has been removed and one of the files contained in the pvt_includes directory must be used to set the proper buffer strength.

Port	Description
rd	RDA or RXB output of the TLK6002
rd_core	Input data. Must swing between dgnd and dvdd
hstl_slew_rate_reg6p2	Slew rate control equal to MDIO register 6.2
dvdd	Digital core supply (1.0V +/- 5%)
vddq	HSTL supply (nominal 1.5 or 1.8 +/- 0.1V)
dgnd	Digital Ground

tlk6002_hstl_td.inc

The file, tlk6002_hstl_td.inc, contains the HSTL input buffer used for the TDA and TDB buses. As described earlier, the circuitry to implement PVT correction has been removed and one of the files contained in the pvt_includes directory must be used to set the proper buffer strength.

Port	Description
td	RDA or RXB input of the TLK6002
td_core	Core-side buffer output
hstl_term_reg6p1	Termination control equal to MDIO register 6.1
hstl_term_reg6p0	Termination control equal to MDIO register 6.0
hvdd	Digital core supply (1.0V +/- 5%)
vddq	HSTL supply (nominal 1.5 or 1.8 +/- 0.1V)
dgnd	Digital Ground

sample_tests subdirectory

The sample_tests directory contains example link simulation using a simple 4-in FR4 line model from the fr4_models directory. The serial link simulation connects the serial driver to the serial termination through the trace model and ac-coupling caps. The parallel simulations connect an HSTL output buffer to an HSTL input buffer through the trace model.

Fr4_models subdirectory

This directory contains models for fr4 traces varying from 4-in to 36-in. All models are 4-ports for direct use on the serial links. When used in the single-ended HSTL simulations, one side of the 4-port is simple grounded.