SONY

Diagonal 6.4 mm (Type 1/2.9) CMOS Image Sensor with Square Pixel for Color Cameras

IMX122LQJ-C

Description

The IMX122LQJ-C is a diagonal 6.4 mm (Type 1/2.9) CMOS active pixel type image sensor with a square pixel array and approximately 2.43 M effective pixels. This chip operates with analog 2.7 V, digital 1.2 V and interface 1.8 V triple power supplies. High sensitivity, low dark current and no smear are achieved through the adoption of R, G and B primary color pigment mosaic filters. This chip features an electronic shutter with variable integration time. (Applications: Surveillance cameras)

Features

- CMOS active pixel type dots
- Input clock frequency: 54 MHz/37.125 MHz
- Readout mode
  All-pixel scan mode
  HD1080 p mode (when INCK = 37.125 MHz)
  HD720 p mode (when INCK = 37.125 MHz)
  Window cropping mode
  Horizontal vertical 2 × 2 binning mode
  Vertical 1/2 subsampling mode
- Variable-speed shutter function (Minimum unit: One horizontal sync signal period (1XHS))
- H driver, V driver and serial communication circuit on chip
- CDS/PGA on chip
  0 dB to 24 dB: Analog Gain 24 dB (step pitch 0.3 dB)
  24.3 dB to 42 dB: Analog Gain 24 dB + Digital Gain 0.3 to 18 dB (step pitch 0.3 dB)
- 10-bit/12-bit A/D converter on-chip
- Output method switchable
  - CMOS logic parallel SDR/DDR output Data-Clock output
  - Low voltage LVDS serial 1ch/2ch output Data-Strobe output
- R, G, B primary color pigment mosaic filters on chip
- Recommended lens F value: 2.8 or more (close side)
- Recommended exit pupil distance: –30 mm to –∞

Exmor™

* “Exmor” is a trademark of Sony Corporation. The “Exmor” is a version of Sony's high performance CMOS image sensor with high-speed processing, low noise and low power dissipation by using column-parallel A/D conversion.

Device Structure

- ◆ CMOS image sensor
- ◆ Image size
  Diagonal 6.4 mm (Type 1/2.9)
- ◆ Total number of pixels
  All-pixel scan: 2000 (H) × 1241 (V) approx. 2.48 M pixels
  HD1080 p: 2000 (H) × 1121 (V) approx. 2.24 M pixels
- ◆ Number of effective pixels
  All-pixel scan: 1984 (H) × 1225 (V) approx. 2.43 M pixels
  HD1080 p: 1984 (H) × 1105 (V) approx. 2.19 M pixels
- ◆ Number of active pixels
  All-pixel scan: 1936 (H) × 1217 (V) approx. 2.36 M pixels
  HD1080 p: 1936 (H) × 1097 (V) approx. 2.12 M pixels
- ◆ Number of recommended recording pixels
  All-pixel scan: 1920 (H) × 1200 (V) approx. 2.30 M pixels
  HD1080 p: 1920 (H) × 1080 (V) approx. 2.07 M pixels
- ◆ Chip size
  7.60 mm (H) × 5.80 mm (V)
- ◆ Unit cell size
  2.8 µm (H) × 2.8 µm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 16 pixels, rear 0 pixels
  Vertical (V) direction: Front 16 pixels, rear 0 pixels
- ◆ Dummy
  Horizontal (H) direction: Front 0 pixels, rear 0 pixels
  Vertical (V) direction: Front 7 pixels, rear 0 pixels
- ◆ Substrate material
  Silicon

Absolute Maximum Ratings

Supply voltage (analog 2.7 V)	AV_{DD}	–0.3 to +3.3	V
Supply voltage (digital 1.2 V)	DV_{DD}	–0.3 to +2.0	V
Supply voltage (digital 1.8 V)	OV_{DD}	–0.3 to +3.3	V
Input voltage (digital)	V_I	–0.3 to OV_{DD} +3.3	V
Output voltage (digital)	V_O	–0.3 to OV_{DD}+3.3	V
Guaranteed Operating temperature	Topr	–10 to +60	°C
Guaranteed storage temperature	Tstg	–30 to +80	°C
Guaranteed performance temperature	Tspc	–10 to +60	°C

Recommended Operating Conditions

Supply voltage (analog 2.7 V)	AV_{DD}	2.7 ± 0.1	V
Supply voltage (digital 1.2 V)	DV_{DD}	1.2 ± 0.1	V
Supply voltage (digital 1.8 V)	OV_{DD}	1.8 ± 0.1	V
Input voltage (digital)	V_I	–0.1 to OV_{DD}+0.1	V
Output voltage (digital)	V_O	–0.1 to OV_{DD}+0.1	V

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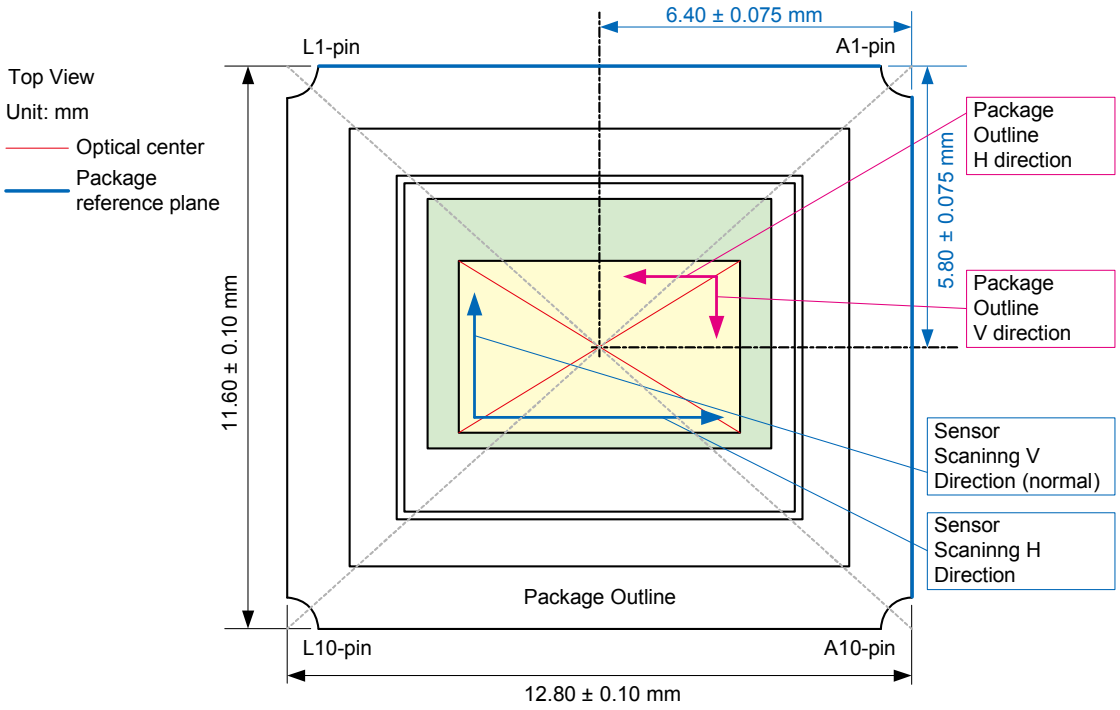
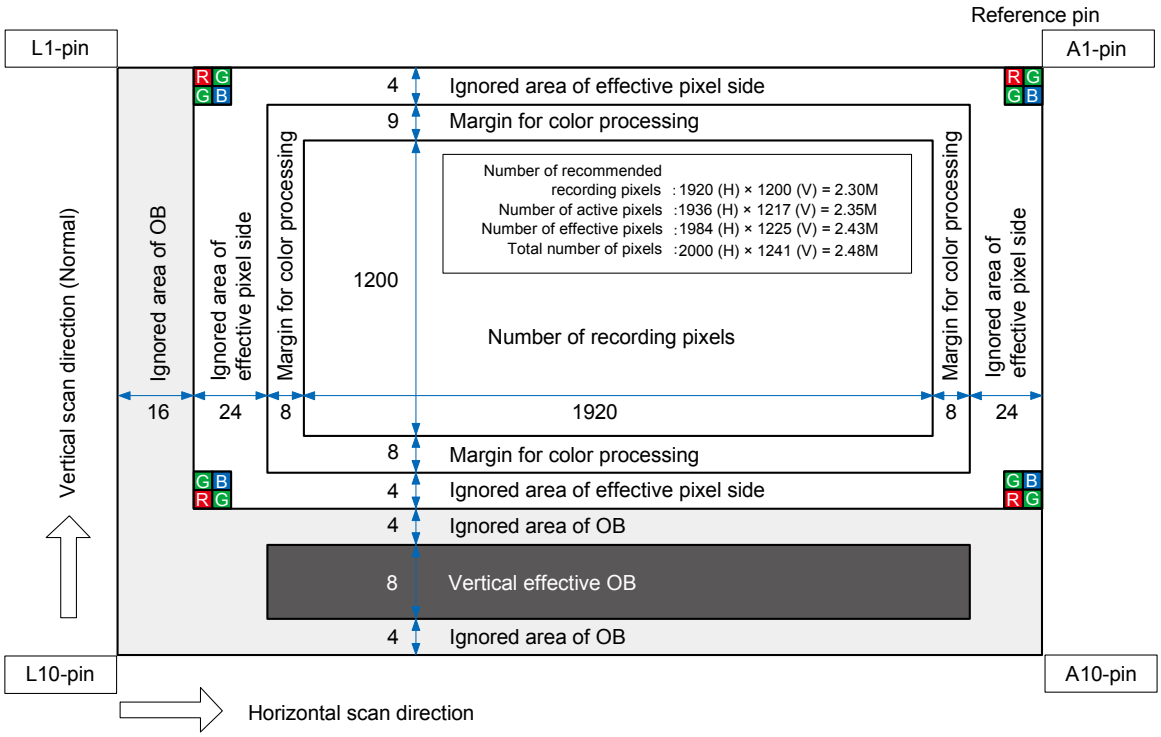
Chip Center and Optical Center



Optical Center

Pixel Arrangement

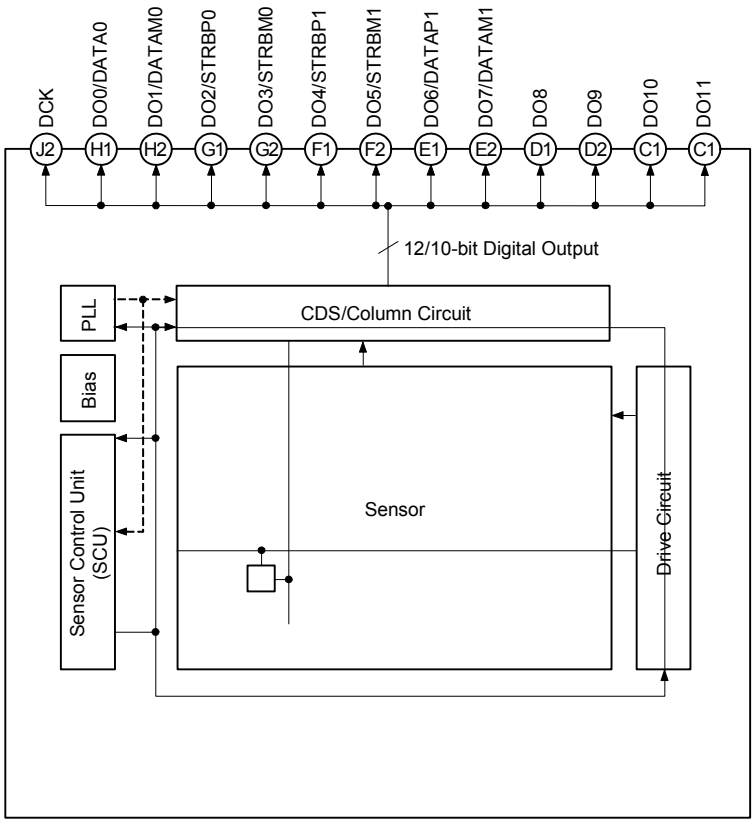
(Top View)



Pixel Arrangement - Physical Image

Block Diagram and Pin Configuration

(Top View)



Block Diagram

	L	K	J	H	G	F	E	D	C	B	A
1	N.C.	N.C.	TEST7	DO0 / DATAP0	DO2 / STRBP0	DO4 / STRBP1	DO6 / DATAP1	DO8	DO10	N.C.	N.C.
2	N.C.	N.C.	DCK	DO1 / DATAM0	DO3 / STRBM0	DO5 / STRBM1	DO7 / DATAM1	DO9	DO11	N.C.	N.C.
3	XVS	INCK	VSSL	XCLR	XHS	VSSL	VSSL	VDDM	VDDM	VSSL	TEST3
4	VDDL	VSSL	VSSL	VDDL				VDDL	VSSL	VSSL	VDDL
5	VDDH	VSSH	VSSL	VDDL				VSSH	VDDH	VSSL	VDDL
6	VDDH	VSSH	VSSL	VDDL				VDDH	SDI	SDO	SCK
7	VDDH	VSSH	VSSH	VDDH2				XMASTER	TEST2	VSSM	VDDM
8	VDDH	VSSH	VSSL	VDDL	VDDL	VDDL	VSSM	TEST1	XCE	VSSH	VDDH
9	TEST6	N.C.	Vcap2	VSSL	VSSL	VSSL	VSSM	TEST4	VCP	N.C.	N.C.
10	N.C.	N.C.	Vcap1	VSSH	VSSH	VDDH	VDDH	TEST5	VRL	N.C.	N.C.

IMX122 TOP View

Pin Configuration

Pin Description

No.	Pin. No.	I/O	Analog/ Digital	Symbol		Description	Remarks
				CMOS parallel	LVDS serial		
1	A1	—	—	N.C.	N.C.	Not connected.	OPEN
2	A2	—	—	N.C.	N.C.	Not connected.	OPEN
3	A3	TEST	D	TEST3	TEST3	Test	Low level fixed
4	A4	Power	D	VDDL	VDDL	1.2 V power supply	
5	A5	Power	D	VDDL	VDDL	1.2 V power supply	
6	A6	I	D	SCK	SCK	Serial I/F (Communication clock input)	
7	A7	Power	D	VDDM	VDDM	1.8 V power supply	
8	A8	Power	A	VDDH	VDDH	2.7 V power supply	
9	A9	—	—	N.C.	N.C.	Not connected.	OPEN
10	A10	—	—	N.C.	N.C.	Not connected.	OPEN
11	B1	—	—	N.C.	N.C.	Not connected.	OPEN
12	B2	—	—	N.C.	N.C.	Not connected.	OPEN
13	B3	GND	D	VSSL	VSSL	1.2 V GND	
14	B4	GND	D	VSSL	VSSL	1.2 V GND	
15	B5	GND	D	VSSL	VSSL	1.2 V GND	
16	B6	O	D	SDO	SDO	Serial I/F (Register value output)	
17	B7	GND	D	VSSM	VSSM	1.8 V GND	
18	B8	GND	A	VSSH	VSSH	2.7 V GND	
19	B9	—	—	N.C.	N.C.	Not connected.	OPEN
20	B10	—	—	N.C.	N.C.	Not connected.	OPEN
21	C1	O	D	DO10	TEST11	When CMOS output: Digital output When LVDS output: Open	
22	C2	O	D	DO11	TEST12	When CMOS output: Digital output When LVDS output: Open	
23	C3	Power	D	VDDM	VDDM	1.8 V power supply	
24	C4	GND	D	VSSL	VSSL	1.2 V GND	
25	C5	Power	A	VDDH	VDDH	2.7 V power supply	
26	C6	I	D	SDI	SDI	Serial I/F (Register value input)	
27	C7	TEST	D	TEST2	TEST2	Test	Low level fixed
28	C8	I	D	XCE	XCE	Serial I/F (Communication enable)	
29	C9	O	A	VCP	VCP	Connected to VRL	Connected to an external capacitor.
30	C10	I	A	VRL	VRL	Connected to VCP	Connected to an external capacitor.
31	D1	O	D	DO8	TEST9	When CMOS output: Digital output When LVDS output: Open	
32	D2	O	D	DO9	TEST10	When CMOS output: Digital output When LVDS output: Open	
33	D3	Power	D	VDDM	VDDM	1.8 V power supply	
34	D4	Power	D	VDDL	VDDL	1.2 V power supply	
35	D5	GND	A	VSSH	VSSH	2.7 V GND	
36	D6	Power	A	VDDH	VDDH	2.7 V power supply	
37	D7	I	D	XMASTER	XMASTER	Slave Mode: High / Master Mode: Low	High:1.8 V Low:GND
38	D8	TEST	D	TEST1	TEST1	Test	10 kΩPull-Up
39	D9	TEST	D	TEST4	TEST4	Test	OPEN
40	D10	TEST	D	TEST5	TEST5	Test	OPEN

No.	Pin. No.	I/O	Analog/ Digital	Symbol		Description	Remarks
				CMOS parallel	LVDS serial		
41	E1	O	D	DO6	DATAP1	When CMOS output: Digital output When LVDS output: LVDS DATAP1 signal output of low power version	
42	E2	O	D	DO7	DATAM1	When CMOS output: Digital output When LVDS output: LVDS DATAM1 signal output of low power version	
43	E3	GND	D	VSSL	VSSL	1.2 V GND	
44	E8	GND	D	VSSM	VSSM	1.8 V GND	
45	E9	GND	D	VSSM	VSSM	1.8 V GND	
46	E10	GND	A	VDDH	VDDH	2.7 V power supply	
47	F1	O	D	DO4	STRBP1	When CMOS output: Digital output When LVDS output: LVDS strobeP1 signal output of low power version	
48	F2	O	D	DO5	STRBM1	When CMOS output: Digital output When LVDS output: LVDS strobeM1 signal output of low power version	
49	F3	GND	D	VSSL	VSSL	1.2 V GND	
50	F8	Power	D	VDDL	VDDL	1.2 V power supply	
51	F9	GND	D	VSSL	VSSL	1.2 V GND	
52	F10	Power	A	VDDH	VDDH	2.7 V power supply	
53	G1	O	D	DO2	STRBP0	When CMOS output: Digital output When LVDS output: LVDS strobeP0 signal output of low power version	
54	G2	O	D	DO3	STRBM0	When CMOS output: Digital output When LVDS output: LVDS strobeM0 signal output of low power version	
55	G3	I/O	D	XHS	XHS	Horizontal sync signal input/output	When LVDS output : Only input
56	G8	Power	D	VDDL	VDDL	1.2 V power supply	
57	G9	GND	D	VSSL	VSSL	1.2 V GND	
58	G10	GND	A	VSSH	VSSH	2.7 V GND	
59	H1	O	D	DO0	DATAP0	When CMOS output: Digital output When LVDS output: LVDS DATAP0 signal output of low power version	
60	H2	O	D	DO1	DATAM0	When CMOS output: Digital output When LVDS output: LVDS DATAM0 signal output of low power version	
61	H3	I	D	XCLR	XCLR	System clear	
62	H4	Power	D	VDDL	VDDL	1.2 V power supply	
63	H5	Power	D	VDDL	VDDL	1.2 V power supply	
64	H6	Power	D	VDDL	VDDL	1.2 V power supply	
65	H7	Power	A	VDDH2	VDDH2	2.7 V power supply	
66	H8	Power	D	VDDL	VDDL	1.2 V power supply	
67	H9	GND	D	VSSL	VSSL	1.2 V GND	
68	H10	GND	A	VSSH	VSSH	2.7 V GND	
69	J1	O	D	TEST7	TEST7	Test	
70	J2	O	D	DCK	TEST8	When CMOS output: clock output. When LVDS output: open	
71	J3	GND	D	VSSL	VSSL	1.2 V GND	
72	J4	GND	D	VSSL	VSSL	1.2 V GND	
73	J5	GND	D	VSSL	VSSL	1.2 V GND	
74	J6	GND	D	VSSL	VSSL	1.2 V GND	
75	J7	GND	A	VSSH	VSSH	2.7 V GND	
76	J8	GND	D	VSSL	VSSL	1.2 V GND	
77	J9	TEST	A	Vcap2	Vcap2	Test	Connected to an external capacitor.
78	J10	TEST	A	Vcap1	Vcap1	Test	Connected to an external capacitor.

No.	Pin. No.	I/O	Analog/ Digital	Symbol		Description	Remarks
				CMOS parallel	LVDS serial		
79	K1	—	—	N.C.	N.C.	Not connected.	OPEN
80	K2	—	—	N.C.	N.C.	Not connected.	OPEN
81	K3	I	D	INCK	INCK	Master clock	
82	K4	GND	D	VSSL	VSSL	1.2 V GND	
83	K5	GND	A	VSSH	VSSH	2.7 V GND	
84	K6	GND	A	VSSH	VSSH	2.7 V GND	
85	K7	GND	A	VSSH	VSSH	2.7 V GND	
86	K8	GND	A	VSSH	VSSH	2.7 V GND	
87	K9	—	—	N.C.	N.C.	Not connected.	OPEN
88	K10	—	—	N.C.	N.C.	Not connected.	OPEN
89	L1	—	—	N.C.	N.C.	Not connected.	OPEN
90	L2	—	—	N.C.	N.C.	Not connected.	OPEN
91	L3	I/O	D	XVS	XVS	Horizontal sync signal input/output Slave mode : Input , Master mode : Output	When LVDS output : Only input
92	L4	GND	D	VDDL	VDDL	1.2 V power supply	
93	L5	Power	A	VDDH	VDDH	2.7 V power supply	
94	L6	Power	A	VDDH	VDDH	2.7 V power supply	
95	L7	Power	A	VDDH	VDDH	2.7 V power supply	
96	L8	Power	A	VDDH	VDDH	2.7 V power supply	
97	L9	TEST	D	TEST6	TEST6	Test	OPEN
98	L10	—	—	N.C.	N.C.	Not connected.	OPEN

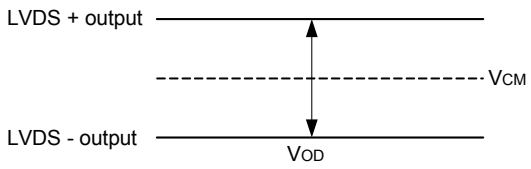
Electrical Characteristics

The electrical characteristics of this device is shown below.

DC Characteristics

Item		Pin	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	$V_{DD}H$	AV_{DD}	—	2.6	2.7	2.8	V
	Digital	$V_{DD}M$	OV_{DD}	—	1.7	1.8	1.9	V
		$V_{DD}L$	DV_{DD}	—	1.1	1.2	1.3	V
Digital input voltage		XHS XVS XCLR INCK XMASTER XCE SDI SCK	V_{IH}	XVS/XHS: In slave mode	$0.8OV_{DD}$	—	—	V
			V_{IL}		—	—	$0.2OV_{DD}$	V
Digital output voltage		DO [11:0] DCK	V_{OH}	CMOS output I_{OH} = -4 mA	OV_{DD} – 0.4	—	—	V
			V_{OL}	CMOS output I_{OL} = 4 mA	—	—	0.4	V
		DATA0/1 STRB0/1	V_{CM}	LVDS output Terminating resistance: 100 Ω	$OV_{DD}/2$ – 0.1	$OV_{DD}/2$	$OV_{DD}/2$ + 0.1	V
			V_{OD}		100	150	200	mV
		XHS XVS SDO	V_{OH}	XVS/XHS: In master mode, CMOS output	OV_{DD} – 0.4	—	—	V
			V_{OL}		—	—	0.4	V

LVDS Output



Current Consumption

Item, conditions	Pin	Symbol	Typ.		Max.		Unit
			Standard Luminous intensity	Saturated luminous intensity	Standard Luminous intensity	Saturated Luminous intensity	
All-pixel mode Parallel CMOS-SDR output INCK = 54 MHz 10 bit/12 bit 19.64 frame/s	$V_{DD}H$	IAV_{DD}	36	36	46	46	mA
	$V_{DD}L$	IDV_{DD}	34	43	46	52	
	$V_{DD}M$	IOV_{DD}	25	5	31	8	
All-pixel mode Serial LVDS-2ch output INCK = 54 MHz 10 bit/12 bit 19.64 frame/s	$V_{DD}H$	IAV_{DD}	36	36	46	46	mA
	$V_{DD}L$	IDV_{DD}	36	45	50	54	
	$V_{DD}M$	IOV_{DD}	12	12	18	18	
HD1080 p mode Parallel CMOS-SDR output INCK = 37.125 MHz 10 bit/12 bit 30 frame/s	$V_{DD}H$	IAV_{DD}	36	36	46	46	mA
	$V_{DD}L$	IDV_{DD}	36	49	47	58	
	$V_{DD}M$	IOV_{DD}	33	5	42	8	
HD1080 p mode Serial LVDS-2ch output INCK = 37.125 MHz 10 bit/12 bit 30 frame/s	$V_{DD}H$	IAV_{DD}	36	36	46	46	mA
	$V_{DD}L$	IDV_{DD}	39	52	51	62	
	$V_{DD}M$	IOV_{DD}	12	12	18	18	
Standby current	$V_{DD}H$	IAV_{DD}_STB	3		47		μA
	$V_{DD}L$	IDV_{DD}_STB	400		2200		
	$V_{DD}M$	IOV_{DD}_STB	5		143		

Typ.: AV_{DD} = 2.7 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Ta = 25 °C
Max.: AV_{DD} = 2.8 V, OV_{DD} = 1.9 V, DV_{DD} = 1.3 V, Ta = 60 °C
Standard luminous intensity: Luminous intensity at standard imaging condition I
Saturated luminous intensity: Luminous intensity when the sensor is saturated

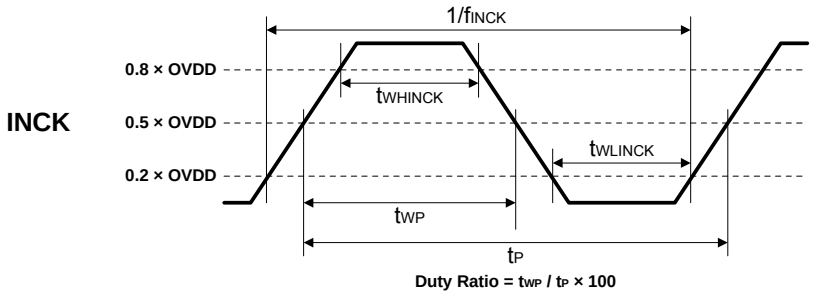
Power Consumption

Item, conditions	Pin	Symbol	Typ.		Max.		Unit
			Standard Luminous intensity	Saturated luminous intensity	Standard Luminous intensity	Saturated Luminous intensity	
All-pixel mode Parallel CMOS-SDR output INCK = 54 MHz 10 bit/12 bit 19.64 frame/s	$V_{DD}H$	IAV_{DD}	97.2	97.2	128.8	128.8	mW
	$V_{DD}L$	IDV_{DD}	40.8	51.6	59.8	67.6	
	$V_{DD}M$	IOV_{DD}	45.0	9.0	58.9	15.2	
	TOTAL	PV_{DD}	183.0	157.8	247.5	211.6	
All-pixel mode Serial LVDS-2ch output INCK = 54 MHz 10 bit/12 bit 19.64 frame/s	$V_{DD}H$	IAV_{DD}	97.2	97.2	128.8	128.8	mW
	$V_{DD}L$	IDV_{DD}	43.2	54.0	65.0	70.2	
	$V_{DD}M$	IOV_{DD}	21.6	21.6	34.2	34.2	
	TOTAL	PV_{DD}	162	172.8	228.0	233.2	
HD1080 p mode Parallel CMOS-SDR output INCK=37.125 MHz 10 bit/12 bit 30 frame/s	$V_{DD}H$	IAV_{DD}	97.2	97.2	128.8	128.8	mW
	$V_{DD}L$	IDV_{DD}	43.2	58.8	61.1	75.4	
	$V_{DD}M$	IOV_{DD}	59.4	9.0	79.8	15.2	
	TOTAL	PV_{DD}	199.8	165.0	269.7	219.4	
HD1080 p mode Serial LVDS-2ch output INCK = 37.125 MHz 10 bit/12 bit 30 frame/s	$V_{DD}H$	IAV_{DD}	97.2	97.2	128.8	128.8	mW
	$V_{DD}L$	IDV_{DD}	46.8	62.4	66.3	80.6	
	$V_{DD}M$	IOV_{DD}	21.6	21.6	34.2	34.2	
	TOTAL	PV_{DD}	165.6	181.2	229.3	243.6	

* The condition of measuring Typ. value and Max. value are the same as current consumption.

AC Characteristics

a) Master clock (INCK)

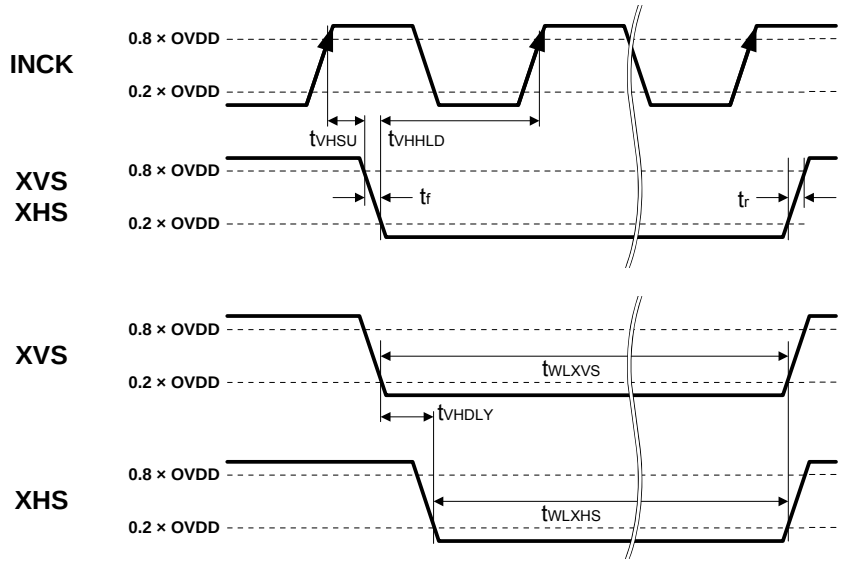


Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	53	54	55	MHz	
INCK Low level width	t_{WLINCK}	6.5	—	—	ns	
INCK High level width	t_{WHINCK}	6.5	—	—	ns	
INCK clock duty	—	45	50	55	%	Defined with 0.5 × OV_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	*1	37.125	*1	MHz	
INCK Low level width	t_{WLINCK}	10.3	—	—	ns	
INCK High level width	t_{WHINCK}	10.3	—	—	ns	
INCK clock duty	—	45	50	55	%	Defined with 0.5 × OV_{DD}

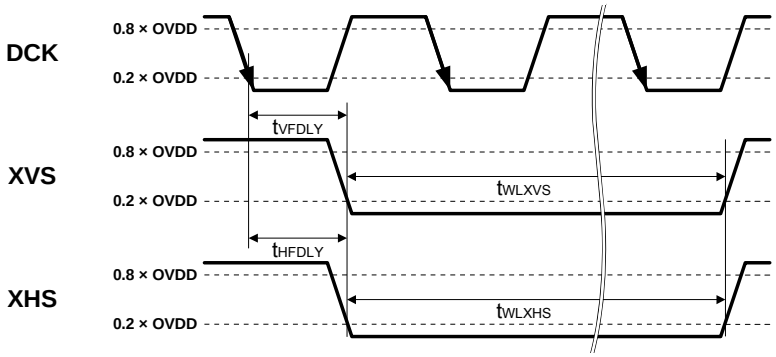
*1 The INCK fluctuation affects the frame rate. 37.125 MHz is the value of INCK for HD1080 p mode and the sensor does not operate with specified 30 frame/s except for typical value.

b) XVS and XHS Input Characteristics (In Slave Mode)



Item	Symbol	Min.	Typ.	Max.	Unit
XVS fall time	tf	—	—	5	ns
XVS rise time	tr	—	—	5	ns
XHS fall time	tf	—	—	5	ns
XHS rise time	tr	—	—	5	ns
XVS, XHS input setup time	t_{VHSU}	0	—	—	ns
XVS, XHS input hold time	t_{VHHLD}	5	—	—	ns
XVS Low level pulse width	t_{WLXVS}	4	—	100	INCK
XHS Low level pulse width	t_{WLXHS}	4	—	100	INCK
XVS-XHS fall delay	t_{VHDLY}	—	—	1	INCK

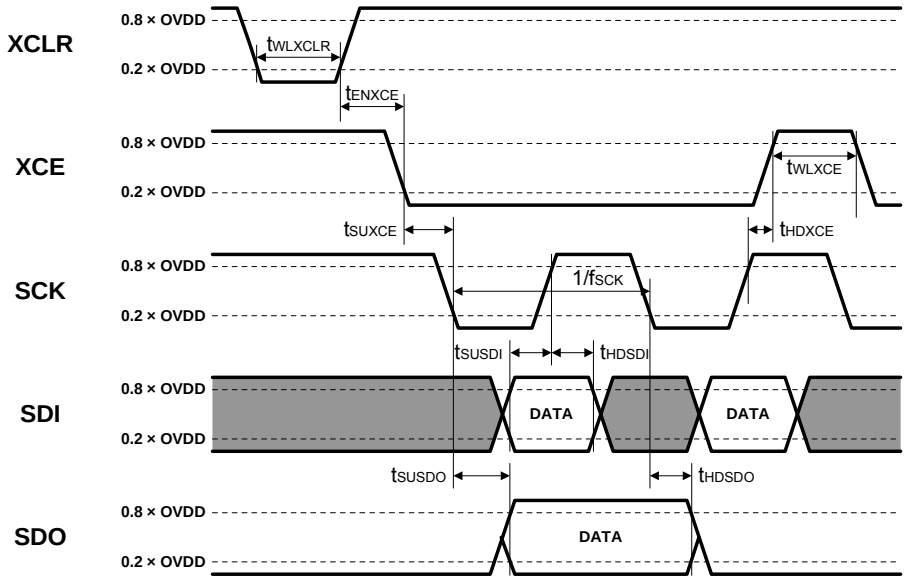
c) XVS, XHS Output Characteristics (In Master Mode, CMOS Output)



(Load capacitance: 20 pF)

Item	Symbol	Min.	Typ.	Max.	Unit
XVS Low level pulse width	t_{WLXVS}	1	1	8	H
XHS Low level pulse width	t_{WLXHS}	6	6	128	DCK
DCK-XVS fall delay	t_{VFDLY}	–1	—	15	ns
DCK-XHS fall delay	t_{HFDLY}	–1	—	15	ns

d) Serial Communication (4-wire Serial)

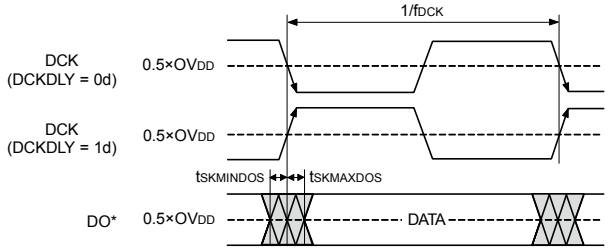


(Output load capacitance: 20 pF)

Item	Symbol	Min.	Typ.	Max.	Unit
SCK clock frequency	f_{SCK}	—	13.5	28	MHz
XCLR Low level pulse width	t_{WLXCLR}	500	—	—	ns
XCE effective margin	t_{ENXCE}	100	—	—	ns
XCE input setup time	t_{SUXCE}	20	—	—	ns
XCE input hold time	t_{HDXCE}	20	—	—	ns
XCE High level pulse width	t_{WLXCE}	20	—	—	ns
SDI input setup time	t_{SUSDI}	10	—	—	ns
SDI input hold time	t_{HDSDI}	10	—	—	ns
SDO output setup time	t_{SUSDO}	—	—	25	ns
SDO output hold time	t_{HDSDO}	0	—	—	ns

e) DCK and DO Output Characteristics (Parallel CMOS Output Mode)

e-1) SDR Output (FRSEL = 1d)

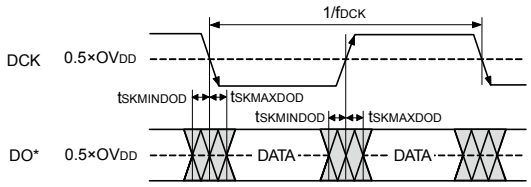


(Output load capacitance: 20 pF)

Item	Symbol	Min.	Typ.	Max.	Unit
DCK clock frequency	f_{DCK}	—	INCK	—	MHz
DCK clock duty	—	40	50	60	%
Maximum skew between DCK and DO*	$t_{SKMAXDOS}$	—	—	2	ns
Minimum skew between DCK and DO*	$t_{SKMINDOS}$	—	—	2	ns

The DCK frequency is the same as that of INCK. It is 54 MHz for all-pixel mode or other modes and 37.125 MHz for HD720 p mode.

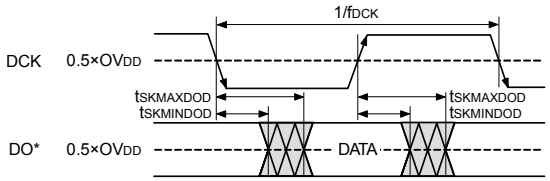
e-2) DDR Output In-phase Output (DCKDLY = 0d) (FRSEL = 1d)



(Output load capacitance: 20 pF)

Item	Symbol	Min.	Typ.	Max.	Unit
DCK clock frequency	f_{DCK}	—	INCK/2	—	MHz
DCK clock duty	—	40	50	60	%
Maximum skew between DCK and DO*	$t_{SKMAXDOD}$	—	—	2	ns
Minimum skew between DCK and DO*	$t_{SKMINDOD}$	—	—	2	ns

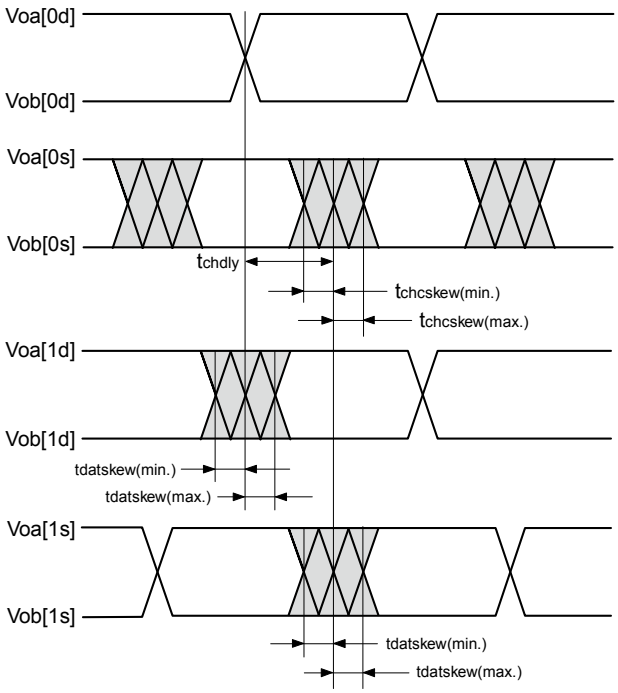
e-3) DDR Output 90 ° Phase Delay Output (DCKDLY = 1d) (FRSEL = 1d)



(Output load capacitance: 20 pF)

Item	Symbol	Min.	Typ.	Max.	Unit
DCK clock frequency	f_{DCK}	—	INCK/2	—	MHz
DCK clock duty	—	40	50	60	%
Maximum skew between DCK and DO*	$t_{SKMAXDOD}$	—	—	6.6	ns
Minimum skew between DCK and DO*	$t_{SKMINDOD}$	3.2	—	—	ns

f) DATA/STROBE Output Characteristics (Serial LVDS Output Mode)



Note)

1. Voa/Vob: Differential signals which are paired
   DATAM0 / DATAP0
   DATAM1 / DATAP1
   STRBM0 / STRBP0
   STRBM1 / STRBP1

2. Characteristics in [ ] indicate the followings
   Figure (0/1): Output channel
   Alphabet (d/s): d: Data
   s: Strobe

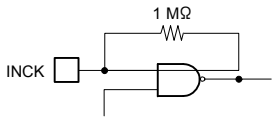
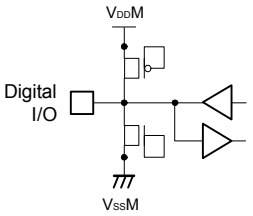
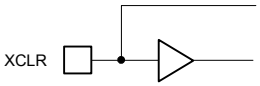
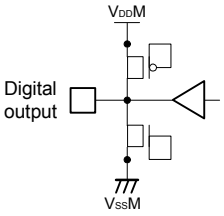
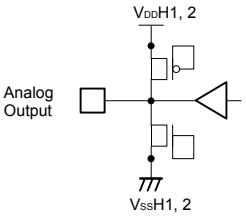
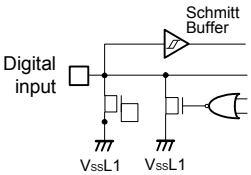
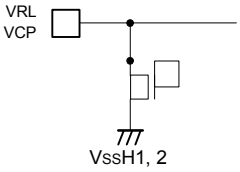
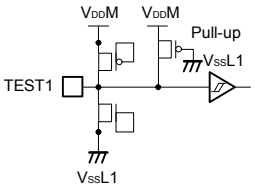
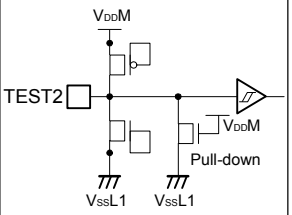
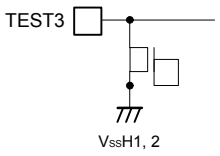
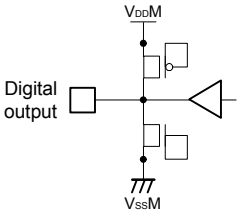
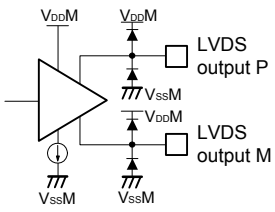
3. $T_{chcskew}$ uses the cross point of Voa and Vob as a reference.
   The skew of STRB signal is set with the DATA clock as a reference in the diagram.

Item	Symbol	Min.	Typ.	Max.	Unit
Skew between differential signal clocks	$t_{chcskew}$	–400	—	400	ps
Skew between different signals	$t_{datskew}$	–250	—	250	ps
Difference between data and strobe edges*1	t_{chdly}	1	—	—	bit

*1 The offset of data output waveform edge and strobe output waveform are represented.
The diagram above indicates the difference from data output edge to strobe output edge.

I/O Equivalent Circuit Diagram

□ : External pin

Symbol	Equivalent circuit	Symbol	Equivalent circuit
INCK		XVS/XHS	
XCLR		SDO	
TEST4 TEST5 TEST6 Vcap1 Vcap2		SDI SCK XCE	
VRL VCP		TEST1	
TEST2		TEST3	
DOx DCK		DATAPx DATAMx STRBPx STRBMx	

Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics.)

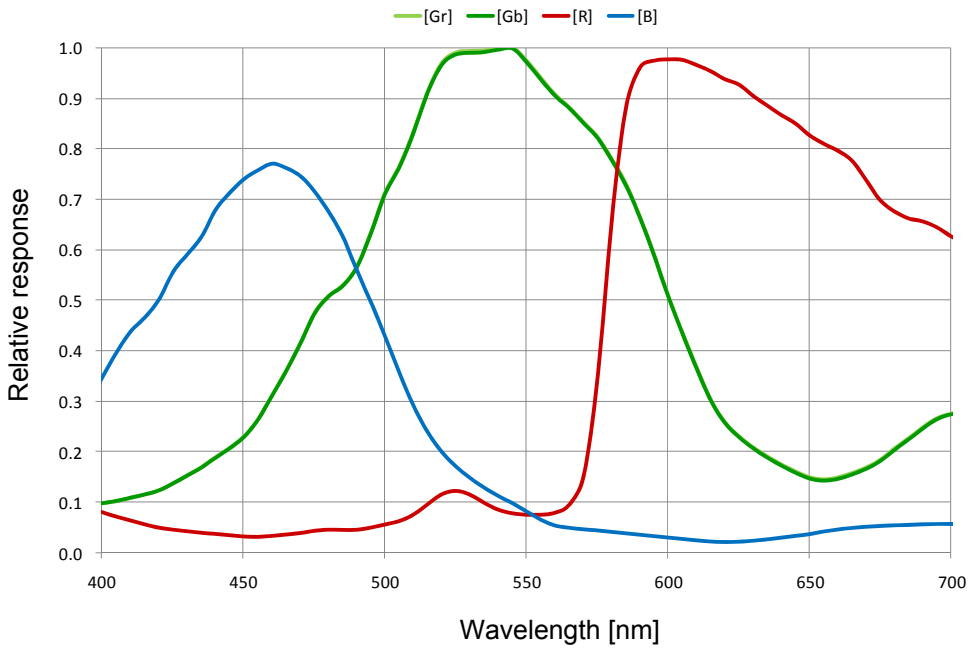


Image Sensor Characteristics

(VA_{DD} = 2.7 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Ta = 60 °C, All-pixel scan 12 bits 19.64 frame/s, Gain: 0 dB)

Item		Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G sensitivity		Sg	1664 (370)	1911 (425)	—	Digit (mV)	1	1/30 s integration
Sensitivity ratio	R/G	Rr	0.45	—	0.6	—	2	
	B/G	Rb	0.35	—	0.5	—		
Saturation signal	Zone0-I*3	Vsat01	3696 (822)	—	—	Digit (mV)	3	Ta= 60 °C
	Zone0-II'*3	Vsat2D	3651 (812)	—	—	Digit (mV)		
Video signal shading	Zone0-I*3	SH01	—	—	20	%	4	
	Zone0-II'*3	SH2D	—	—	25	%		
Dark signal		Vdt	—	—	0.67 (0.15)	Digit (mV)	5	Ta = 60 °C, 1/30 s integration
Dark signal shading		ΔVdt	—	—	0.67 (0.15)	Digit (mV)	6	Ta = 60 °C, 1/30 s integration
Line crawl R		Lcr	—	—	6	%	7	
Line crawl B		Lcb	—	—	6	%		
Lag		Lag	—	—	0.5	%	8	

*1 Conversion is executed with 1 digit = 0.890 mV for 10-bit output and 1 digit = 0.222 mV for 12-bit output.
*2 The video signal shading is the measured value in the wafer status (including color filter) and does not include the seal glass characteristics.
*3 See the Zone Definition of Video Signal Shading (diagram below) for Zone.

Zone Definition of Video Signal Shading

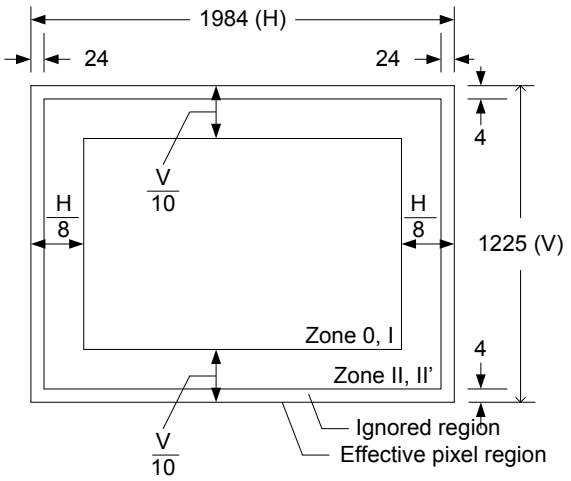


Image Sensor Characteristics Measurement Method

Measurement Conditions

In the following measurements, the device drive conditions are at the typical values of the bias conditions and clock voltage conditions.
In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, which is taken as the value of the Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

Color Coding of this Image Sensor and Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure below. Gr and Gb represent the G signal on the same line as the R and B signals, respectively. The Gb signal and B signal lines and the R signal and Gr signal lines are output successively.

Gb	B	Gb	B
R	Gr	R	Gr
Gb	B	Gb	B
R	Gr	R	Gr

Color Coding Diagram

Definition of standard imaging conditions

◆ Standard imaging condition I:

Use a pattern box (luminance: 706 cd/m^{2,} color temperature of 3200 K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:

Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

◆ Standard imaging condition III:

Image a light source (color temperature of 3200 K) with a uniformity of brightness within 2 % at all angles. Use a testing standard lens (exit pupil distance -30 mm) with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

Measurement Method

1. Sensitivity
   Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100 s, measure the Gr and Gb signal outputs (VGr, VGb) at the center of the screen, and substitute the values into the following formula.

   $$Sg = (VGr + VGb)/2 \times 100/30 \text{ [mV]}$$

2. Sensitivity ratio
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr and Gb signal outputs to 425 mV, measure the R signal output (VR [mV]), the Gr and Gb signal outputs (VGr, VGb [mV]) and the B signal output (VB [mV]) at the center of the screen in frame readout mode, and substitute the values into the following formulas.

   $$VG = (VGr + VGb)/2$$
   $$Rr = VR/VG$$
   $$Rb = VB/VG$$

3. Saturation signal
   Set the measurement condition to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr and Gb signal outputs, 425 mV, measure the average values of the Gr, Gb, R and B signal outputs.

4. Video signal shading
   Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F2.8, adjust the luminous intensity so that the average value of the Gr and Gb signal outputs is 425 mV. Then measure the maximum value (Gmax [mV]) and the minimum value (Gmin [mV]) of the Gr and Gb signal outputs, and substitute the values into the following formula.

   $$SH = (Gmax - Gmin)/425 \times 100 \text{ [\%]}$$

5. Dark signal
   With the device ambient temperature of 60 °C and the device in the light-obstructed state, divide the output difference between 1/30 s integration and 1/300 s integration by 0.9, and calculate the signal output converted to 1/30 s integration. Measure the average value of this output (Vdt [mV]).

6. Dark signal shading
   After the measurement item 5, measure the maximum value (Vdmax [mV]) and the minimum value (Vdmin [mV]) of the dark signal output, and substitute the values into the following formula.

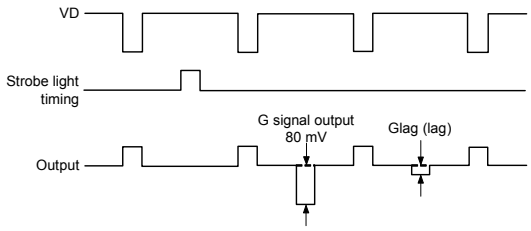
   $$\Delta Vdt = Vdmax - Vdmin \text{ [mV]}$$

7. Line crawl
   Set the measurement condition to the standard imaging condition II. After adjusting the average value of the Gr signal output to 400 mV, insert R and B filters and measure the difference between G signal lines (ΔGlr, ΔGlb[mV]) as well as the average values of the G signal outputs (Gar, Gab). Substitute the values into the following formula.

   $$Lci = (\Delta Gli/Gai) \times 100 \text{ [\%]} \quad (i = r, b)$$

8. Lag
   Adjust the G signal output value generated by strobe light to 80 mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Glag), and substitute the value into the following formula.

   Lag = (Glag/80) × 100 [%]



Setting Registers with Serial Communication

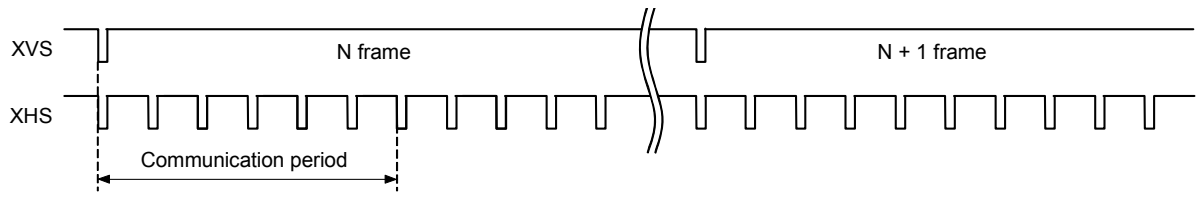
Description of Setting Registers

This sensor can write and read the setting values of the various registers shown in the Register Map by 3-wire serial communication. See the Register Map for the addresses and setting values to be set. The serial data input order is LSB-first transfer. The table below shows the various data types and descriptions.

Type	Description
ChipID	02h: Write to the CID = 02h register 03h: Write to the CID = 03h register 82h: Read from the CID = 02h register 83h: Read from the CID = 03h register
Address	Designate the address according to the Register Map. When using a communication method that designates continuous addresses, the address is automatically incremented from the previously transmitted address.
Data	Input the setting values according to the Register Map.

Register Communication Timing

Perform register communication within the 6H period after the falling edge of XVS. Register setting values are reflected at the following timing. When communication is performed during the communication period shown in the figure below, items noted as “V” in the “Reflection timing” column of the Register Map are output in the state with the setting value reflected in the N frame. However, note that although the integration time setting is reflected in the N frame, it is reflected to shutter control after N frame readout, so the setting value is reflected to the output in the N + 1 frame. Items that are reflected instantly are reflected at the timing when communication is performed.



Register Reflection Timing

Register Write and Read

◆ Follow the communication procedure below when writing registers.

(1) Set XCE Low to enable the chip's communication function.
Serial data input is executed using SCK and SDI.

(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)

(3) Input the Chip ID (CID = 02h or 03h) to the first byte. If the Chip ID differs, subsequent data is ignored.

(4) Input the start address to the second byte. The address is automatically incremented.

(5) Input the data to the third and subsequent bytes. The data in the third byte is written to the register address designated by the second byte, and the register address is automatically incremented thereafter when writing the data for the fourth and subsequent bytes. Normal register data is loaded to the inside of the sensor and established in 8-bit units.

(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The register values before the write operation are output. The actual register values are the input data.

(7) Set XCE High to end communication.

◆ Follow the communication procedure below when reading registers.

(1) Set XCE Low to enable the chip's communication function.
Serial data input is executed using SCK and SDI.

(2) Transmit data in sync with SCK 1 bit at a time from the LSB using SDI. Transfer SDI in sync with the falling edge of SCK. (The data is loaded at the rising edge of SCK.)

(3) Input Chip ID (CID = 82h or 83h) to the first byte. If the Chip ID differs, subsequent data is ignored.

(4) Input the start address to the second byte. The address is automatically incremented.

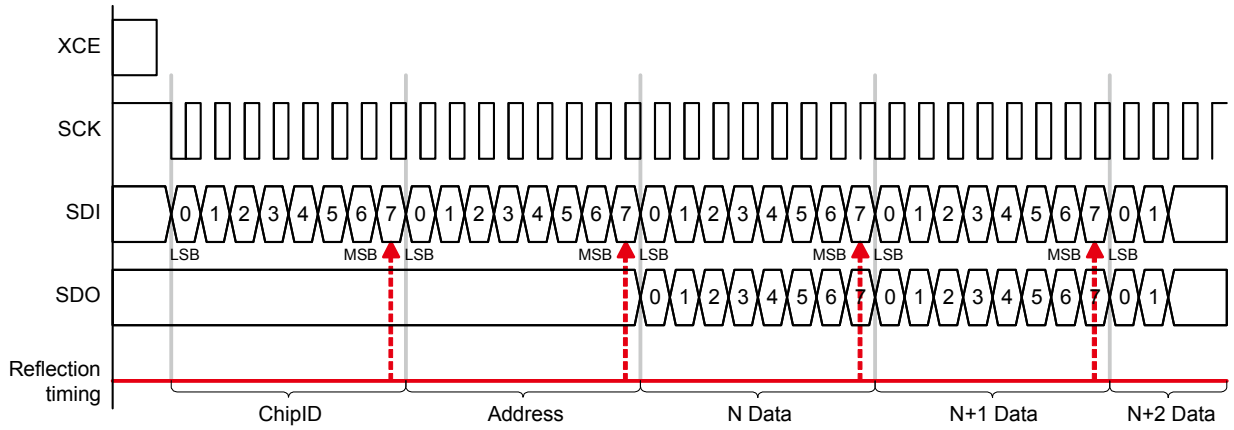
(5) Input data to the third and subsequent bytes. Input dummy data in order to read the registers. The dummy data is not written to the registers. To read continuous data, input the necessary number of bytes of dummy data.

(6) The register values starting from the register address designated by the second byte are output from the SDO pin. The input data is not written, so the actual register values are output.

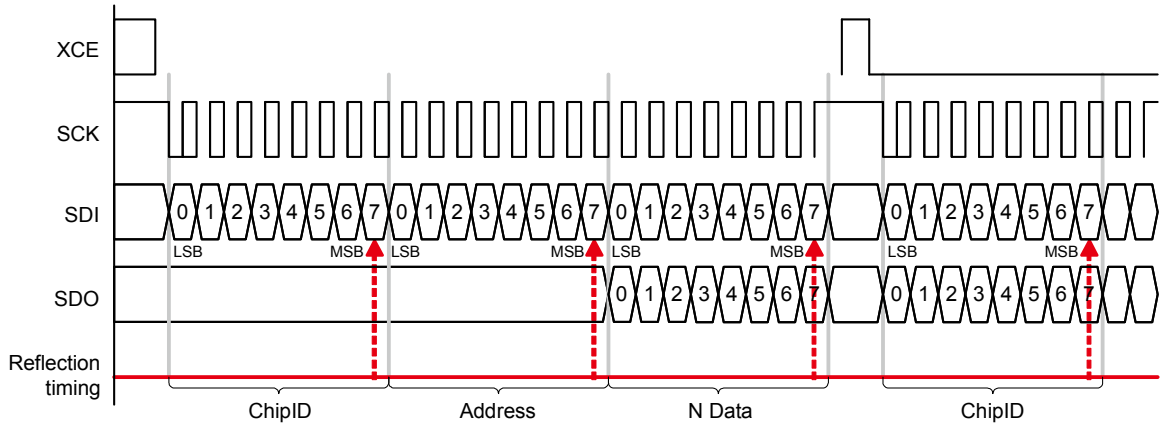
(7) Set XCE High to end communication.

Note) Even when changing register setting values during imaging, communication should finish within the 6H communication period. When writing data to multiple registers with discontinuous addresses, access to undesired registers can be avoided by repeating the above procedure multiple times. The figures on the following page show examples of transmission.

Communication Timing to Registers with Continuous Addresses



Communication Timing to Registers with Discontinuous Addresses



Register Map

ChipID: 02

Address	Bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
00h	0	STANDBY	STANDBY control 0: Normal operation, 1: STANDBY	1	01h	*1
	1		Fixed to “0”.	0		
	2		Fixed to “0”.	0		
	3		Fixed to “0”.	0		
	4	TESTEN [1:0]	Register write 0h: Invalid 3h: Valid Others: Invalid	0		Immediately
	5					
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		
01h	0	VREVERSE	Vertical (V) scanning direction control 0: Normal 1: Inverted	0	00h	V
	1		Fixed to “0”.	0		
	2		Fixed to “0”.	0		
	3		Fixed to “0”.	0		
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		
02h	0	MODE [3:0]	Readout mode designation 0h: All pixels (2.3 M) 1h:HD720 p 2h: Window cropping 3h: 2 × 2 binning 4h: Vertical 1/2 subsampling Fh: HD1080 p Others: Invalid	0	00h	V
	1					
	2					
	3					
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		

Address	Bit	Register name	Description	Default value after reset		Reflection timing
				By register	By address	
03h	0	HMAX [13:0]	LSB	044Ch	4Ch	V
	1					
	2					
	3					
	4					
	5					
	6					
	7		In master mode Horizontal (H) direction clock number designation Default: All-pixel 10 bits 39.27 frame/s			
04h	0				04h	
	1					
	2					
	3					
	4					
	5		MSB			
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		
05h	0	VMAX [15:0]	LSB	04E2h	E2h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7		In master mode Vertical (V) direction line number designation Default: All-pixel 10 bits 39.27 frame/s			
06h	0				04h	
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			
07h	[7:0]		Fixed to “00h”	00h	00h	

Address	Bit	Register name	Description	Default value after reset		Reflection timing
				By register	By register	
08h	0	SHS1[15:0]	LSB	0000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7		Integration time adjustment Designated in line units			
09h	0				00h	
	1					
	2					
	3					
	4					
	5					
	6					
	7		MSB			
0Ah	[7:0]		Fixed to “00h”	00h	00h	
0Bh	[7:0]		Fixed to “00h”	00h	00h	
0Ch	[7:0]		Fixed to “00h”	00h	00h	
0Dh	0	SPL[9:0]	LSB	000h	00h	V
	1					
	2					
	3					
	4		Integration time adjustment (Low-speed shutter) Designated in frame units			
	5					
	6					
	7					
0Eh	0				00h	
	1		MSB			
	2		Fixed to “0”.	0		
	3		Fixed to “0”.	0		
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		

Address	Bit	Register name	Description	Default value after reset		Reflection timing
				By register	By register	
0Fh	0	SVS [9:0]	LSB Integration time adjustment (Low-speed shutter) Designated in frame units	000h	00h	V
	1					
	2					
	3					
	4					
	5					
	6					
	7					
10h	0		MSB		00h	
	1					
	2		Fixed to “0”.	0		
	3		Fixed to “0”.	0		
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		
11h	0	FRSEL [2:0]	Output data rate designation 0: 2 times INCK 1: Equal to INCK 2: 1/2 of INCK (2 × 2 binning mode only) 3: 1/4 of INCK (2 × 2 binning mode only) Others: Invalid	0h	88h	V
	1					
	2					
	3	OPORTSEL [1:0]	Output system selection 0: Parallel CMOS SDR output 1: Parallel CMOS DDR output 2: Serial LVDS 1ch output 3: Serial LVDS 2ch output	1h		Immediately
	4					
	5	M12BEN [1:0]	The output resolution is set to 10 bit (2x2 binning mode only.) 0: disable 2:enable others: setting prohibited	0h		V
	6					
	7		Fixed to “0”. *2	1		Immediately
12h	0	SSBRK	Low-speed shutter forcible termination	0	80h	Immediately
	1	ADRES	AD gradation setting 0: 10 bits, 1: 12 bits	0		V
	2		Fixed to “0”.	0		
	3		Fixed to “0”.	0		
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “1”.	1		
13h	[7:0]		Fixed to “40h”.	00h	00h	Immediately

Address	Bit	Register name	Description	Default value after reset		Reflection timing
				By register	By register	
14h	0	WINPH [11:0]	LSB	000h	00h	V
	1					
	2					
	3					
	4					
	5		In window cropping mode Designation of upper left coordinate for cropping position (Horizontal position)			
	6					
	7					
15h	0				00h	
	1					
	2					
	3		MSB			
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		
16h	0	WINPV [11:0]	LSB	000h	00h	V
	1					
	2					
	3					
	4					
	5		In window cropping mode Designation of upper left coordinate for cropping position (Vertical position)			
	6					
	7					
17h	0				00h	
	1					
	2					
	3		MSB			
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		

Address	Bit	Register name	Description	Default value after reset		Reflection timing
				By register	By register	
18h	0	WINWH [11:0]	LSB	7C0h	C0h	V
	1					
	2					
	3					
	4					
	5		In window cropping mode Cropping size designation (Horizontal direction)			
	6					
	7					
19h	0				07h	
	1					
	2					
	3		MSB			
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		
1 Ah	0	WINWV [11:0]	LSB	4C9h	C9h	V
	1					
	2					
	3					
	4					
	5		In window cropping mode Cropping size designation (Vertical direction)			
	6					
	7					
1Bh	0				04h	
	1					
	2					
	3		MSB			
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		
1Ch	[7:0]		Fixed to “50h”	50h	50h	
1Dh	[7:0]		Fixed to “00h”	00h	00h	

Address	Bit	Register name	Description	Default value after reset		Reflection timing
				By register	By register	
1Eh	0	GAIN [7:0]	LSB	00h	00h	V
	1					
	2					
	3					
	4		Gain setting			
	5					
	6					
	7		MSB			
1Fh	[7:0]		Fixed to “31h”.	31h	31h	
20h	0	BLKLEVEL [8:0]	LSB	03Ch	3Ch	Immediately
	1					
	2					
	3					
	4		Black level offset value setting			
	5					
	6					
	7					
21h	0		MSB		00h	
	1		Fixed to “0”.	0		
	2		Fixed to “0”.	0		
	3		Fixed to “0”.	0		
	4	XHSLNG [1:0]	XHS low level width setting 0h: 6 clk, 1h: 12 clk, 2h: 22 clk, 3h: 128 clk	0h		Immediately
	5					
	6		Fixed to “0”.	0		
	7	10BITA	Setting registers for 10 bit.	0		Immediately
22h	0	XVSLNG [2:0]	XVS low level width setting. 0h: 1 line, 1h: 2line, 2h: 4line, 3h: 8 line, others: Invalid	0h	00h	Immediately
	1					
	2					
	3		Fixed to “0”.	0		
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “1”. *2	0		
	7	720PMODE	Fixed to 1 for HD720 p mode.	0		V
23h to 26h	[7:0] to [7:0]		Do not communicate			
27h	[7:0]		Fixed to “20”.	21h		Immediately
28h to 2Bh	[7:0] to [7:0]		Do not communicate			

Address	Bit	Register name	Description	Default value after reset		Reflection timing
				By register	By register	
2Ch	0	XMSTA	Trigger for master mode operation start 0:Master mode operation start 1: Trigger standby	1	01h	Immediately
	1		Fixed to “0”.	0		
	2		Fixed to “0”.	0		
	3		Fixed to “0”.	0		
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		
2Dh	0		Fixed to “0”.	0	40h	
	1	DCKDLY	DCK phase delay For SDR output ... 0: 0 °, 1: 180 ° For DDR output... 0: 0 °, 1: 90 °	0		V
	2		Fixed to “0”	0		
	3	BITSEL	10-bit output 2-bit shift 0: Left justified, 1: Right justified	0		V
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “1”.	1		
	7		Fixed to “0”.	0		
2Eh to 3Ah	[7:0] to [7:0]		Do not communicate.			
3Bh	[7:0]	SYNCCODE [7:0]	Sync code setting	E0h	E0h	V
3Ch to 79h	[7:0] to [7:0]		Do not communicate.			
7Ah	[7:0]	10BITB	Setting registers for 10 bit.	00h	00h	Immediately
7Bh	[7:0]	10BITC	Setting registers for 10 bit.	00h	00h	Immediately
7Ch to 97h	[7:0] to [7:0]		Do not communicate.			

Address	Bit	Register name	Description	Default value after reset		Reflection timing
				By register	By register	
98h	0	10B1080 P [11:0]	LSB	226h	26h	
	1					
	2					
	3					
	4					
	5					
	6					
	7					
99h	0				02h	
	1					
	2					
	3		MSB			
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		
9Ah	0	12B1080 P [11:0]	LSB	44Ch	4Ch	Immediately
	1					
	2					
	3					
	4					
	5					
	6					
	7					
9Bh	0				04h	
	1					
	2					
	3		MSB			
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		

Address	Bit	Register name	Description	Default value after reset		Reflection timing
				By register	By register	
9Ch to CDh	[7:0] to [7:0]		Do not communicate			
CEh	0	PRES[6:0]	LSB	16h	16h	Immediately
	1					
	2					
	3		Adjustment registers for each operation mode.			
	4					
	5					
	6		MSB			
	7		Fixed to “0”.	0		
CFh	0	DRES	LSB	082h	82h	Immediately
	1					
	2					
	3					
	4		Adjustment registers for each operation mode.			
	5					
	6					
	7					
D0h	0		MSB		00h	
	1		Fixed to “0”.	0		
	2		Fixed to “0”.	0		
	3		Fixed to “0”.	0		
	4		Fixed to “0”.	0		
	5		Fixed to “0”.	0		
	6		Fixed to “0”.	0		
	7		Fixed to “0”.	0		

ChipID: 03

Address	Bit	Register name	Description	Default value after reset		Reflection timing
				By register	By register	
17h	[7:0]		Fixed to “0Dh” *2.	4Dh	4Dh	Immediately

*1 The STANDBY (Address 00h [0]) register is reflected at the following timings.
•When canceling standby mode: Reflected immediately
•When entering standby mode: Reflected immediately after the end of the frame during which the setting was made

*2 The values must be changed from the default values, so initial setting after reset is required after power-on. Subsequent setting by communication is not needed unless the power is turned Off or the system is reset.

*3 “V” in the “Reflection timing” column indicates that the setting value is reflected at the falling edge of the next XVS after the register communication is performed.

*4 Do not perform communication to addresses not listed in the Register Map. Doing so may result in malfunction. However, other registers that require communication to addresses not listed above may be added, so addresses up to FFh should be supported for both CID = 02h and 03h.

Readout Drive Mode

The table below lists the operating modes available with this sensor.

Drive mode	Imaging conditions							
	INCK [MHz]	Frame rate [frame/s]	Output Resolution [bit]	Number of effective pixels		Data width*1		1H period [µs]
				H [pixels]	V [lines]	H [INCK]	V [lines]	
All-pixel scan	54	19.64	10/12	1984	1225	2200	1250	40.74
		39.27	10			1100		20.37
HD1080 p	37.125	15.00	10/12	1984	1105	2200	1125	59.26
		25.00	10/12			1320		35.56
		30.00	10/12			1100		29.63
HD720 p	37.125	30.00	10/12	1344	745	1650	750	44.44
		60.00	10			825		22.22
Window cropping (UXGA)	54	14.985	10/12	1664	1225	2200	1638	40.74
		29.97	10			1100		20.37
2 × 2 binning readout	54	14.985	10/12*2	992	612	4400	819	81.48
		29.97	10/12*2			2200		40.74
Vertical 1/2 subsampling	54	29.97	10/12	1368	524	2200	819	40.74
		59.94	10			1100		20.37

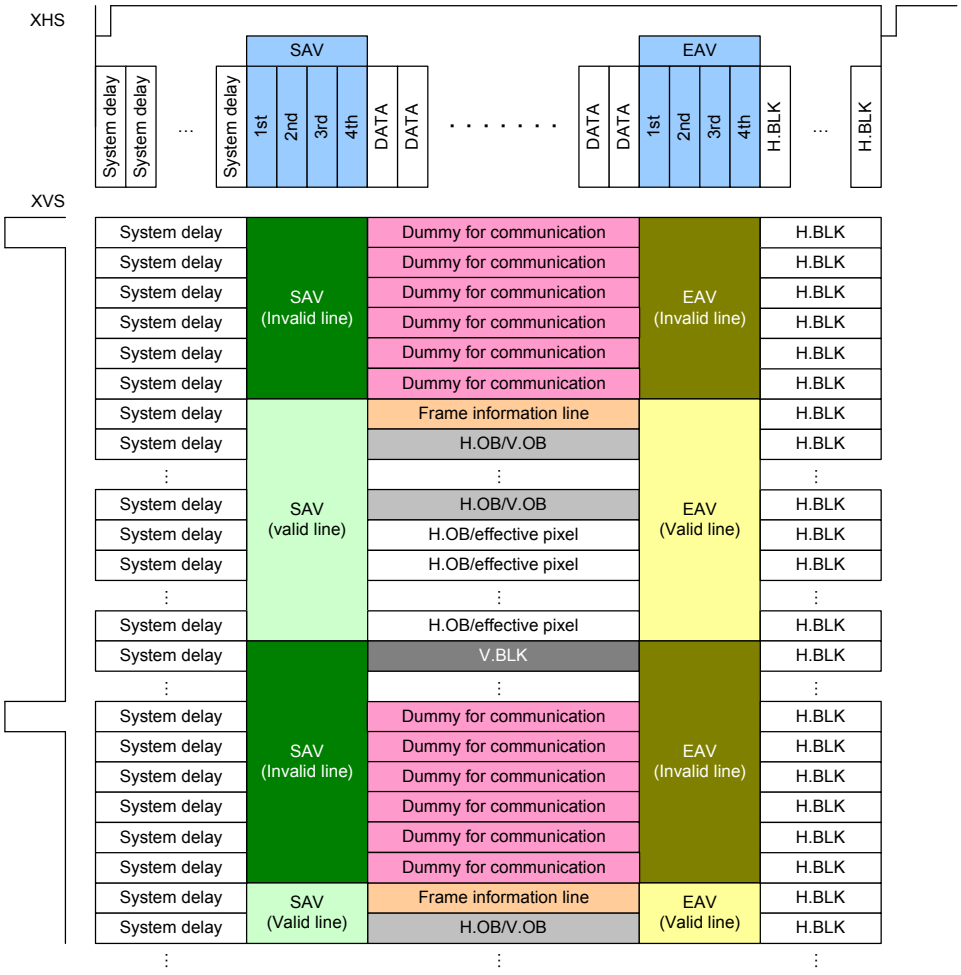
*1 The data width indicates the output sync signal period in master mode. In slave mode the data width is the input XVS and XHS clock interval.

*2 In 2 × 2 binning readout mode, the pixel signals are converted to 10 bits and digitally added. The output gradation can be selected from 10 bits or 12 bits.

Drive mode	Imaging conditions			Data rate			
	INCK [MHz]	Frame rate [frame/s]	Output resolution [bit]	Parallel CMOS output		Serial LVDS output	
				SDR	DDR	1ch	2ch
All-pixel scan	54	19.64	10/12	54	54	648	648
		39.27	10	N/A	108	N/A	1296
HD1080 p	37.125	15.00	10/12	37.125	37.125	445.5	445.5
		25.00	10/12	74.25	74.25	N/A	891
		30.00	10/12	74.25	74.25	N/A	891
HD720 p	37.125	30.00	10/12	37.125	37.125	445.5	445.5
		60.00	10	74.25	74.25	N/A	891
Window cropping (UXGA)	54	14.985	10/12	54	54	648	648
		29.97	10	N/A	108	N/A	1296
2 × 2 binning readout	54	14.985	10/12	13.5	13.5	162	162
		29.97	10/12	27	27	324	324
Vertical 1/2 sub sampling	54	29.97	10/12	54	54	648	648
		59.94	10	N/A	108	N/A	1296

Sync Code (Parallel CMOS Output Mode)

The sync code is added immediately before and after “dummy signal + OB signal + effective pixel data” and then output. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd. (BLK: Blanking period)

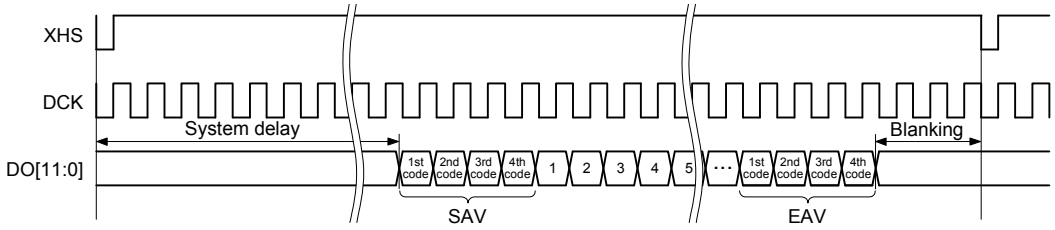


Sync code	1st code		2nd code		3rd code		4th code	
	10 bit	12 bit	10 bit	12 bit	10 bit	12 bit	10 bit	12 bit
SAV(Valid line)	3FFh	FFFh	000h	000h	000h	000h	200h	800h
EAV(Valid line)	3FFh	FFFh	000h	000h	000h	000h	274h	9D0h
SAV(Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2ACh	AB0h
EAV(Invalid line)	3FFh	FFFh	000h	000h	000h	000h	2D8h	B60h

Sync Code Output Timing (Parallel CMOS Output)

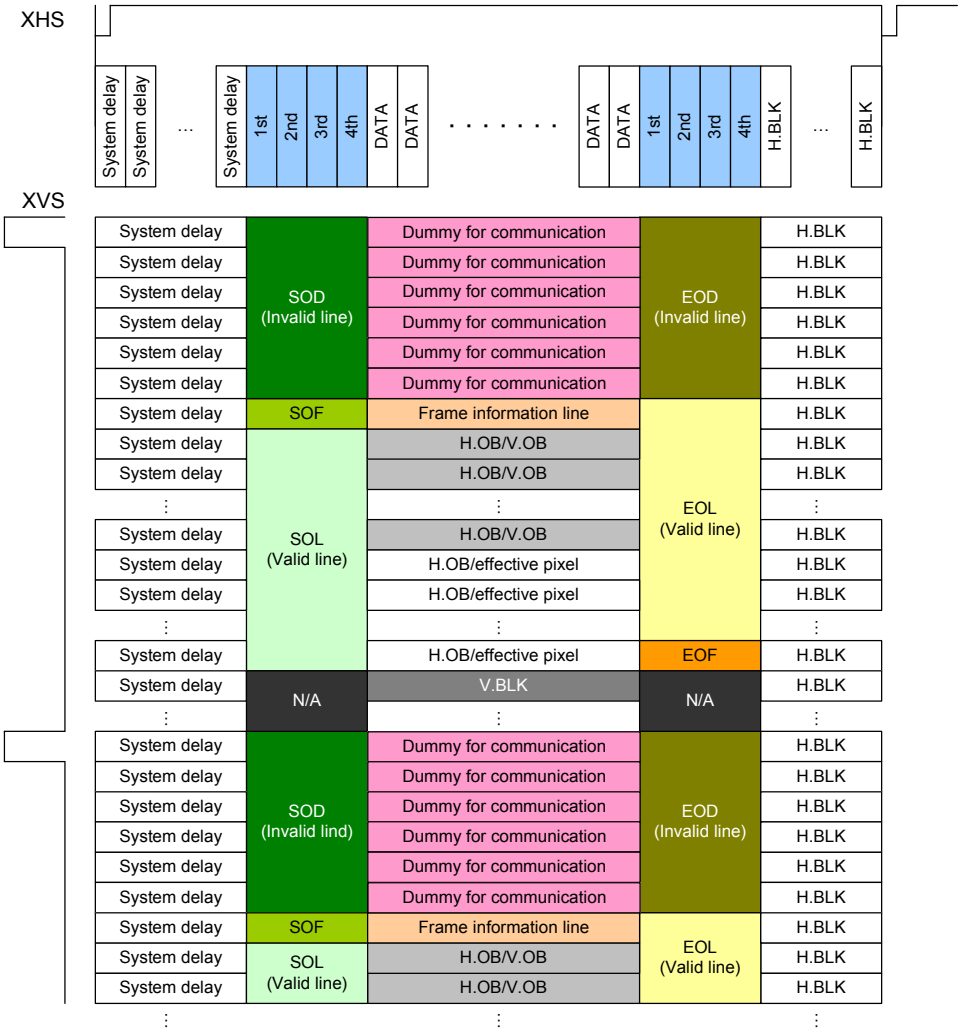
Sync Code Output Timing (Parallel CMOS Output Mode)

The sensor output signal passes through the internal circuits and is output with a latency time (system delay) relative to the horizontal sync signal. This system delay value is undefined for each line, so refer to the sync codes output from the sensor and perform synchronization.



Sync Code (Serial LVDS Output Mode)

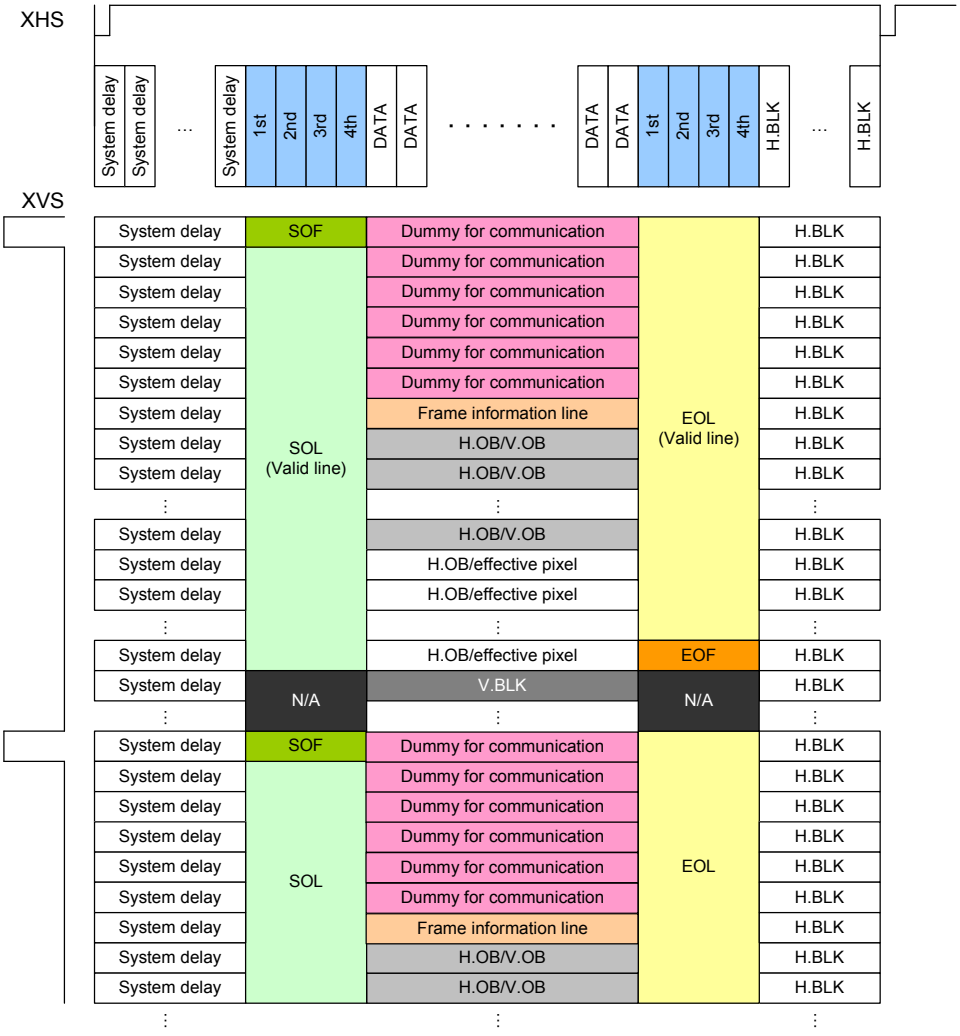
The sync code is added immediately before and after “dummy signal + OB signal + effective pixel data” and then output. The sync code is output in order of 1st, 2nd, 3rd and 4th. The fixed value is output for 1st to 3rd. (BLK: Blanking period)



Sync code	Output	1st code	2nd code	3rd code	4th code
SOD(Invalid line) Dummy start code	DATA0	0Fh	00h	00h	80h
	DATA1	0Fh	00h	00h	C0h
EOD(Invalid line) Dummy end code	DATA0	0Fh	00h	00h	88h
	DATA1	0Fh	00h	00h	C8h
SOL(Valid line) Line start code	DATA0	0Fh	00h	00h	00h
	DATA1	0Fh	00h	00h	40h
EOL(Valid line) Line end code	DATA0	0Fh	00h	00h	08h
	DATA1	0Fh	00h	00h	48h
SOF Frame start code	DATA0	0Fh	00h	00h	10h
	DATA1	0Fh	00h	00h	50h
EOF Frame end code	DATA0	0Fh	00h	00h	18h
	DATA1	0Fh	00h	00h	58h
N/A	DATA0/1	xxh	xxh	xxh	xxh

* N/A : The minimum sensor output value is output (Not 00h)

Sync Code 1 Output Timing (Serial LVDS Output)



Sync code	Output	1st code	2nd code	3rd code	4th code
SOL Line start code	DATA0	0Fh	00h	00h	00h
	DATA1	0Fh	00h	00h	40h
EOL Line end code	DATA0	0Fh	00h	00h	08h
	DATA1	0Fh	00h	00h	48h
SOF Frame start code	DATA0	0Fh	00h	00h	10h
	DATA1	0Fh	00h	00h	50h
EOF Frame end code	DATA0	0Fh	00h	00h	18h
	DATA1	0Fh	00h	00h	58h
N/A	DATA0/1	xxh	xxh	xxh	xxh

* N/A : The minimum sensor output value is output. (Not 00h)

Sync Code 2 Output Timing (Serial LVDS Output)

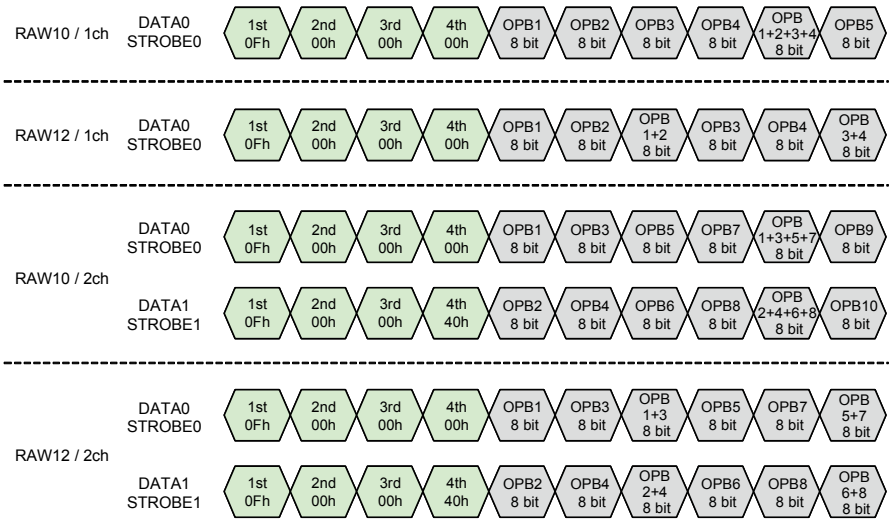
Sync Code Output Timing (Serial LVDS Output Mode)

In serial LVDS output mode, the sync codes can be selected from sync code 1 that is output added to the effective signal line, and sync code 2 that are not added during the vertical blanking period. The figure below shows examples of the two sync code types. In addition, the sync codes are output in the order of 1st → 2nd → 3rd → 4th, and fixed values are output for the 1st to 3rd sync codes.
(BLK: Blanking period)
8 bits of sync codes are added, from 1st to 4th, regardless of the number of output bits (10 bits or 12 bits).
Codes supporting 1ch and 2ch are added in the 4th code and output. (See the figure below.)

List of Sync Code Setting Registers

Register details				Initial value	Setting value	Function
Register name	ChipID	Address	Bit			
SYNCCODE	02h	3Bh	[7:0]	E0h	E0h	In parallel CMOS output mode
					90h	Operation using sync code 1 in serial LVDS output mode
					D0h	Operation using sync code 2 in serial LVDS output mode

When outputting SOL (Code when starting an effective line)



Example of Sync Code Output

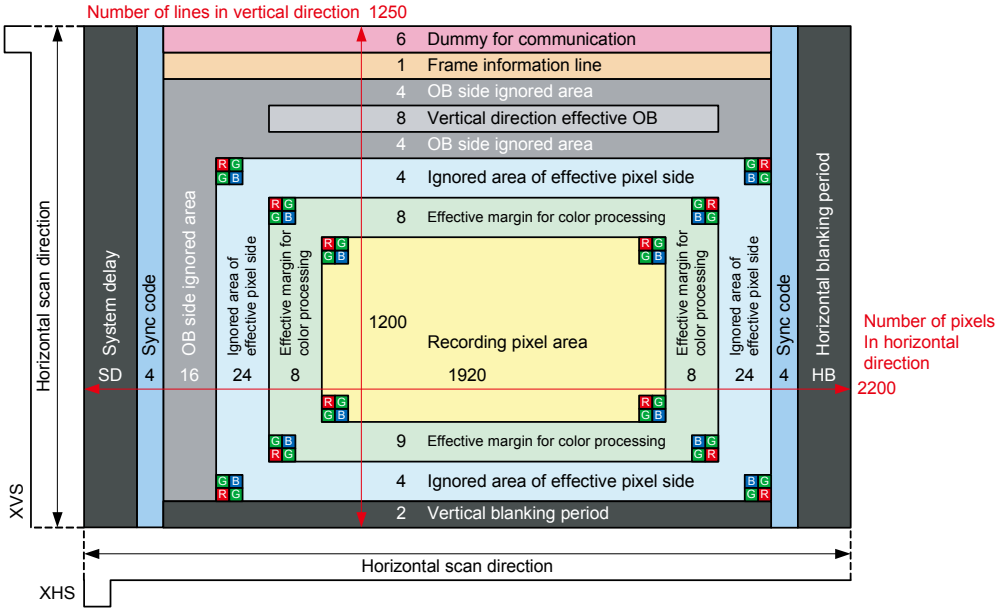
Image Data Output Format

All-pixel Scan Mode

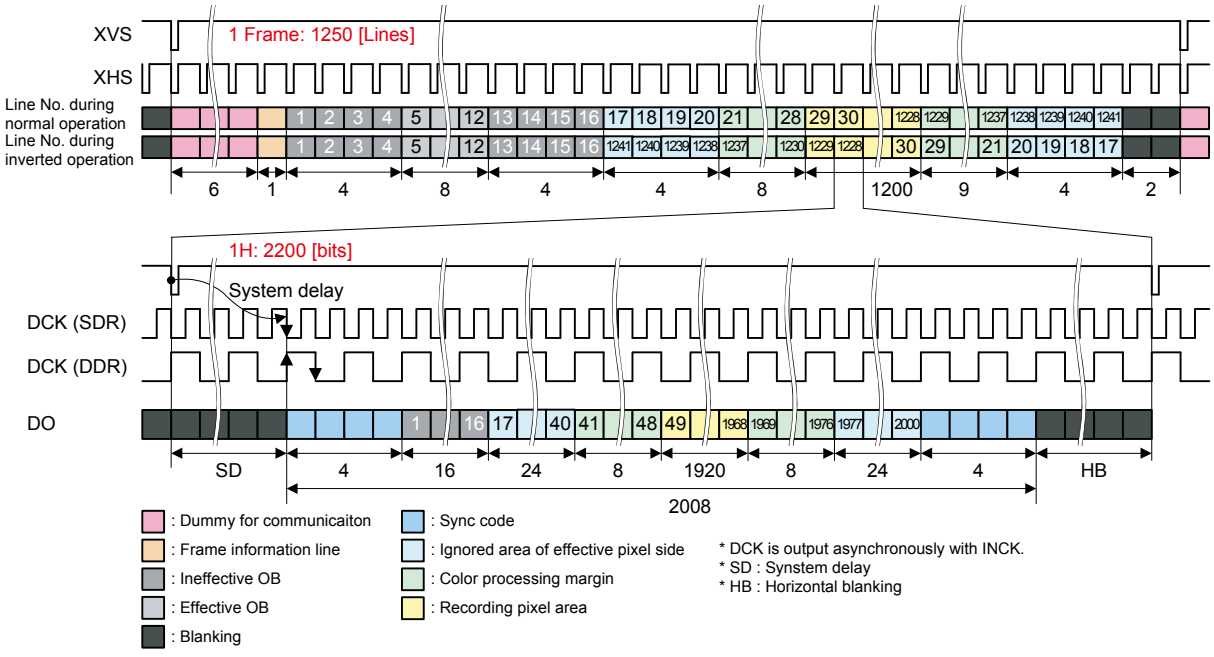
The all pixel signals of sensor are read.

Register List of All-pixel Mode Setting

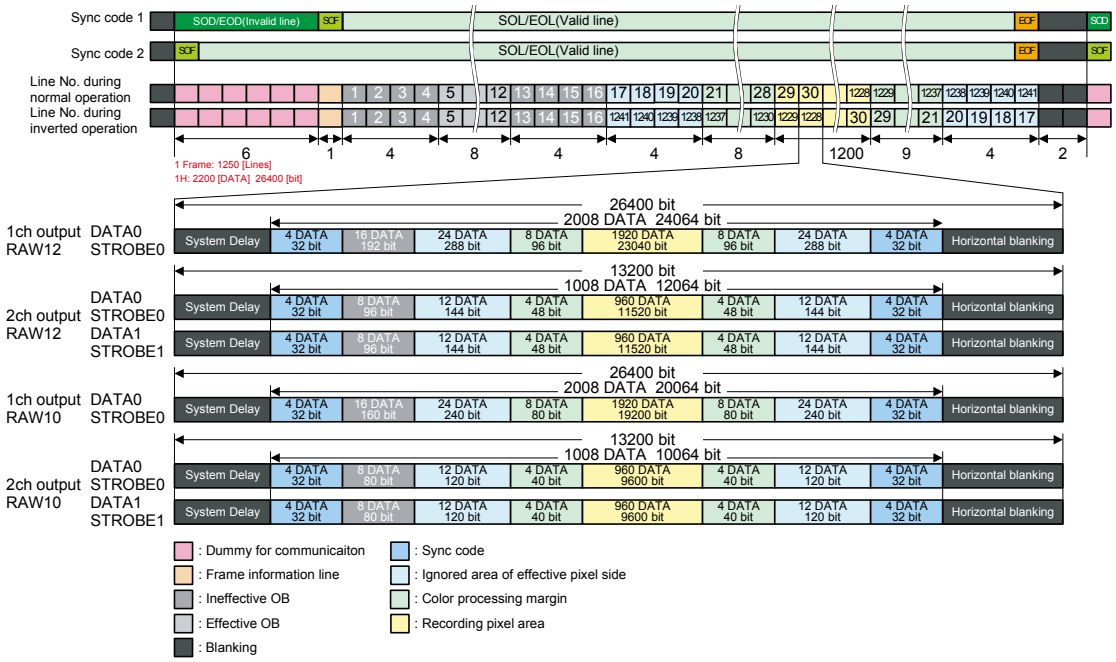
Register details			Initial value	Setting value			Function
				10 bit		12 bit	
Register name	Address	Bit		19.64 [frame/s]	39.27 [frame/s]	19.64 [frame/s]	
MODE	02h	[3:0]	00h	0h			All-pixel mode
HMAX	03h	[7:0]	044Ch	0898h	044Ch	0898h	Horizontal (H) direction clock number designation.
	04h	[5:0]					
VMAX	05h	[7:0]	04E2h	04E2h			Vertical (V) direction line number designation.
	06h	[7:0]					
FRSEL	11h	[2:0]	0h	1h	0h	1h	Output data rate designation.
OPORTSEL		[4:3]	1h	0h	N/A	0h	Parallel CMOS SDR output.
				1h	1h	1h	Parallel CMOS DDR output
				2h	N/A	2h	Serial LVDS 1ch output.
				3h	3h	3h	Serial LVDS 2ch output.
M12BEN		[6:5]	0h	0h			Output gradation setting
ADRES	12h	[1]	0h	0h		1h	AD gradation setting.
WINPH	14h	[7:0]	000h	000h			Designation of upper left coordinate for cropping position (Horizontal)
	15h	[3:0]					
WINPV	16h	[7:0]	000h	000h			Designation of upper left coordinate for cropping position (Vertical)
	17h	[3:0]					
WNIWH	18h	[7:0]	7C0h	7C0h			Cropping size designation (Horizontal)
	19h	[3:0]					
WINWV	1Ah	[7:0]	4C9h	4C9h			Cropping size designation (Vertical)
	1Bh	[3:0]					
10BITA	21h	[7]	0	1	0		Adjustments register for each operation mode.
720 P MODE	22h	[7]	0	0			Sets in 720 p mode only.
10BITB	7Ah	[7:0]	00h	40h	00h		Adjustments register for each operation mode.
10BITC	7Bh	[7:0]	00h	02h	00h		
10B1080 P	98h	[7:0]	226h	02h	00h		
	99h	[3:0]					
12B1080 P	9Ah	[7:0]	44Ch	44Ch			
	9Bh	[3:0]					
PRES	CEh	[6:0]	16h	16h		40h	
DRES	CFh	[7:0]	082h	082h		181h	
	D0h	[0]					



Pixel Array Image Drawing in All-pixel Scan Mode



Drive Timing Chart for Parallel CMOS Output in All-pixel Scan Mode



Drive Timing Chart for Serial LVDS Output in All-pixel Scan Mode

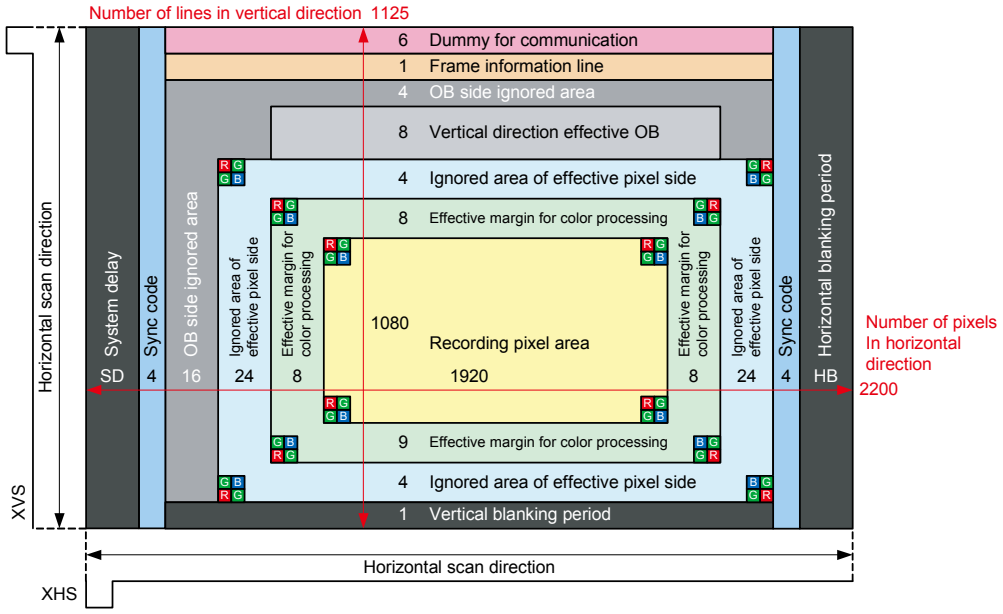
HD1080 p Mode

The sensor signal is cut out with the angle of view for HD1080 p (1920 × 1080) and read.
Input 37.125 MHz to INCK.

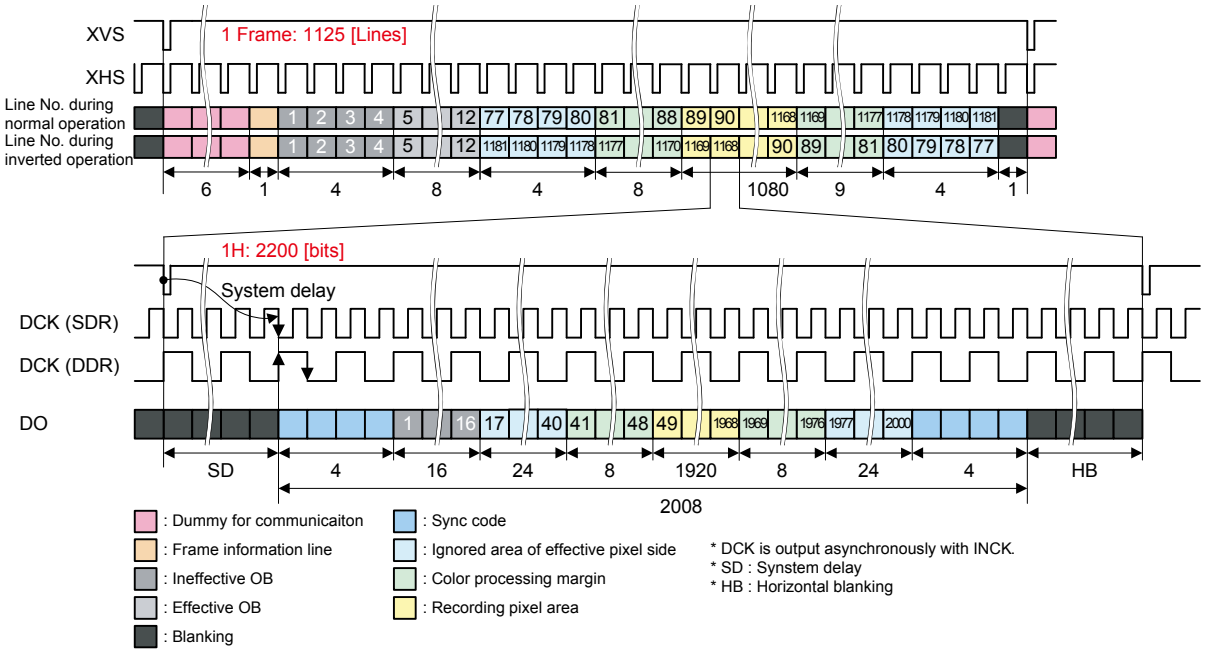
Register List for HD1080 p Mode Setting

Register details			Initial value	Setting value				Function
				10 bit		12 bit		
Register name	Address	Bit		15 [frame/s]	30 [frame/s]	15 [frame/s]	30 [frame/s]	
MODE	02h	[3:0]	00h	Fh				HD1080 p mode
HMAX	03h	[7:0]	044Ch	0898h	044Ch	0898h	044Ch	Horizontal (H) direction clock number designation
	04h	[5:0]						
VMAX	05h	[7:0]	04E2h	0465h				Vertical (V) direction line number designation
	06h	[7:0]						
FRSEL	11h	[2:0]	0h	1h	0h	1h	0h	Output data rate designation
OPORTSEL		[4:3]	1h	0h	0h	0h	0h	Parallel CMOS SDR output
				1h	1h	1h	1h	Parallel CMOS DDR output
				2h	N/A	2h	N/A	Serial LVDS 1ch output
				3h	3h	3h	3h	Serial LVDS 2ch output
M12BEN		[6:5]	0h	0h				Output gradation setting
ADRES	12h	[1]	0h	0h		1h		AD gradation setting
WINPH	14h	[7:0]	000h	000h				Designation of upper left coordinate for cropping position (Horizontal)
	15h	[3:0]						
WINPV	16h	[7:0]	000h	03Ch				Designation of upper left coordinate for cropping position (Vertical)
	17h	[3:0]						
WNIWH	18h	[7:0]	7C0h	7C0h				Cropping size designation (Horizontal)
	19h	[3:0]						
WINWV	1Ah	[7:0]	4C9h	451h				Cropping size designation (Vertical)
	1Bh	[3:0]						
10BITA	21h	[7]	0	1		0		Adjustments register for each operation mode.
720PMODE	22h	[7]	0	0				Sets in 720 p mode only.
10BITB	7Ah	[7:0]	00h	40h		00h		Adjustments register for each operation mode.
10BITC	7Bh	[7:0]	00h	02h		00h		
10B1080 P	98h	[7:0]	226h	44Ch		226h		
	99h	[3:0]						
12B1080 P	9Ah	[7:0]	44Ch	44Ch			226h	
	9Bh	[3:0]						
PRES	CEh	[6:0]	16h	16h	40h	16h		
DRES	CFh	[7:0]	082h	082h	181h	082h		
	D0h	[0]						

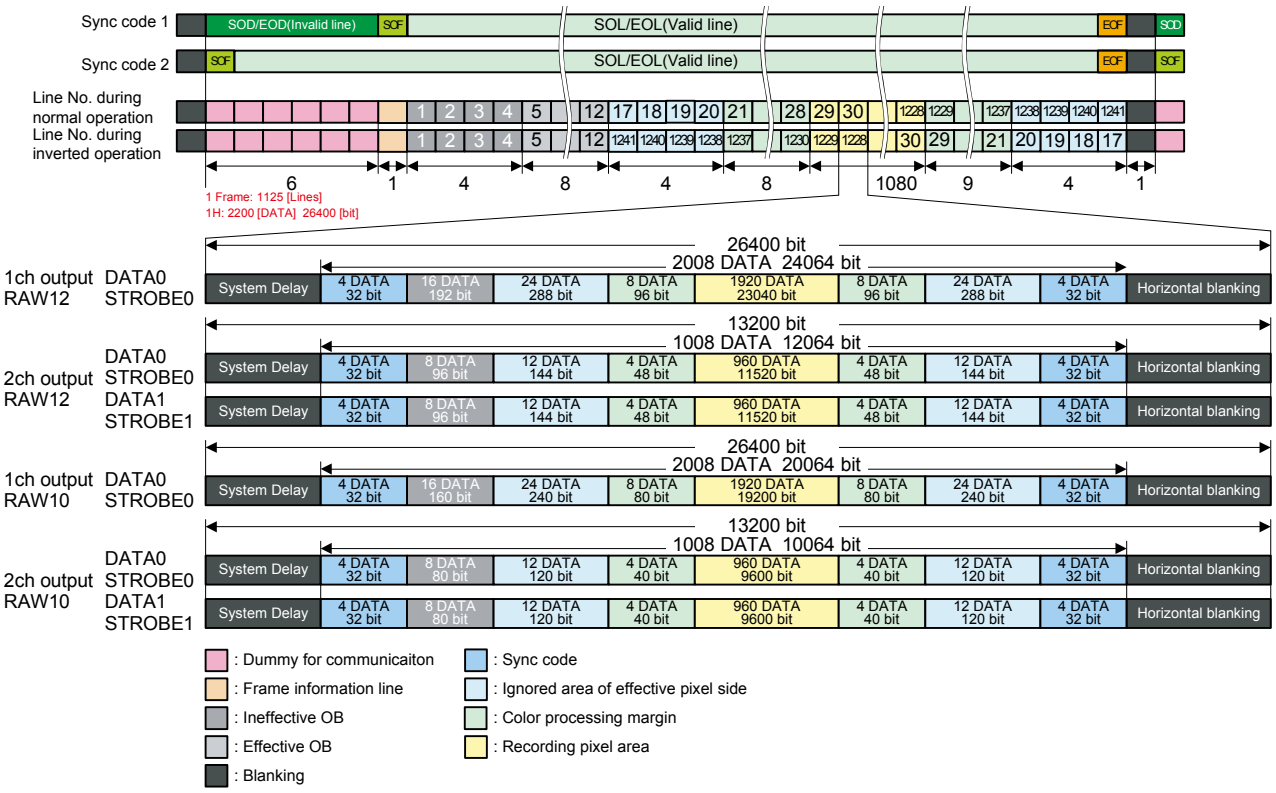
Register details			Initial value	Setting value		Function
Register name	Address	Bit		10 bit	12 bit	
				25 [frame/s]		
MODE	02h	[3:0]	00h	Fh		HD1080 p mode
HMAX	03h	[7:0]	044Ch	0528h		Horizontal (H) direction clock number designation.
	04h	[5:0]				
VMAX	05h	[7:0]	04E2h	0465h		Vertical (V) direction line number designation.
	06h	[7:0]				
FRSEL	11h	[2:0]	0h	0h		Output data rate designation.
OPORTSEL		[4:3]	1h	0h	0h	Parallel CMOS SDR output.
				1h	1h	Parallel CMOS DDR output
				N/A	N/A	Serial LVDS 1ch output.
				3h	3h	Serial LVDS 2ch output.
M12BEN		[6:5]	0h	0h		Output gradation setting
ADRES	12h	[1]	0h	0h	1h	AD gradation setting.
WINPH	14h	[7:0]	000h	000h		Designation of upper left coordinate for cropping position (Horizontal)
	15h	[3:0]				
WINPV	16h	[7:0]	000h	03Ch		Designation of upper left coordinate for cropping position (Vertical)
	17h	[3:0]				
WNIWH	18h	[7:0]	7C0h	7C0h		Cropping size designation (Horizontal)
	19h	[3:0]				
WINWV	1Ah	[7:0]	4C9h	451h		Cropping size designation (Vertical)
	1Bh	[3:0]				
10BITA	21h	[7]	0	1	0	Adjustments register for each operation mode.
720PMODE	22h	[7]	0	0		Sets in 720 p mode only.
10BITB	7Ah	[7:0]	00h	40h	00h	Adjustments register for each operation mode.
10BITC	7Bh	[7:0]	00h	02h	00h	
10B1080 P	98h	[7:0]	226h	294h	226h	
	99h	[3:0]				
12B1080 P	9Ah	[7:0]	44Ch	44Ch	226h	
	9Bh	[3:0]				
PRES	CEh	[6:0]	16h	40h	16h	
DRES	CFh	[7:0]	082h	181h	082h	
	D0h	[0]				



Pixel Array Image Drawing in HD1080 p Mode



Drive Timing Chart for Parallel CMOS Output in HD1080 p Mode



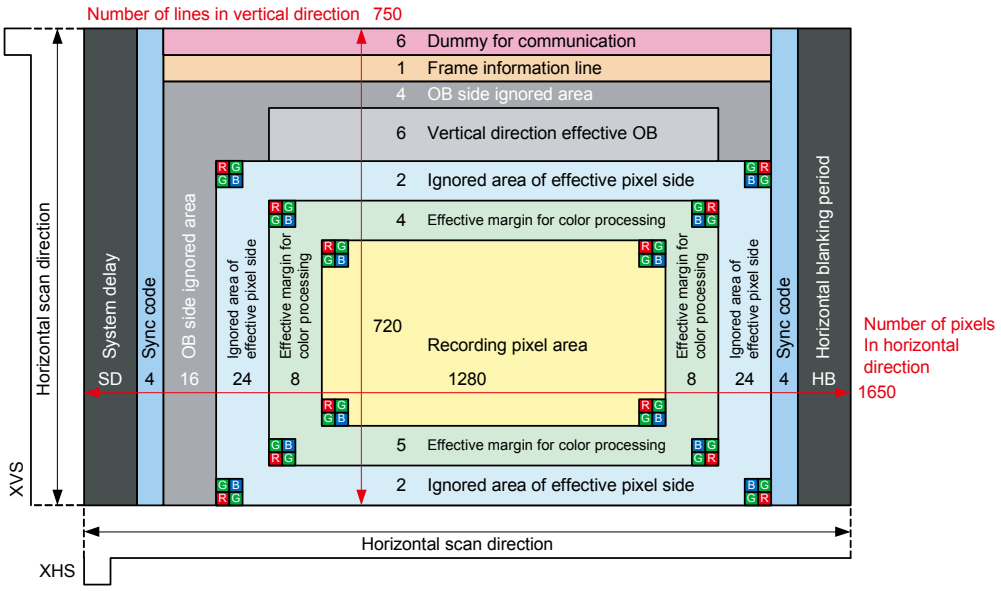
Drive Timing Chart for Serial LVDS Output in HD1080 p Mode

HD720 p mode

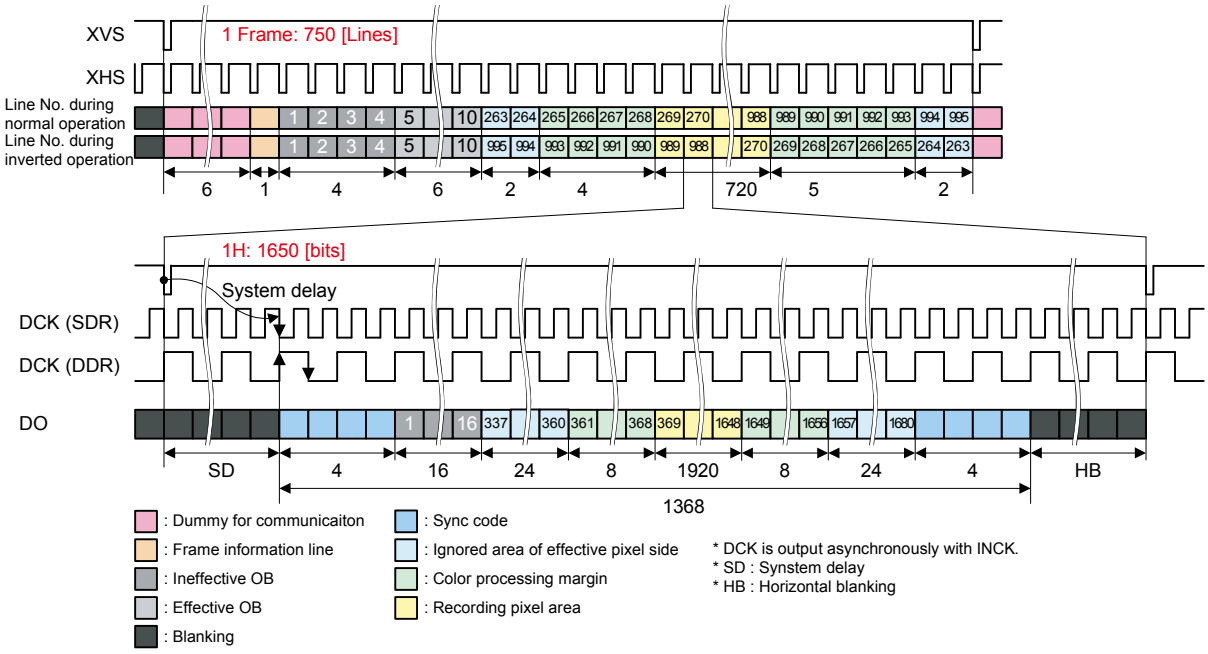
The sensor signal is cut out with the angle of view for HD720 p (1280 × 720) and read.
However,set “1” to the register 720 P MODE (Address 22h [7])
Input 37.125 MHz to INCK.

Register List for HD720 p Mode Setting

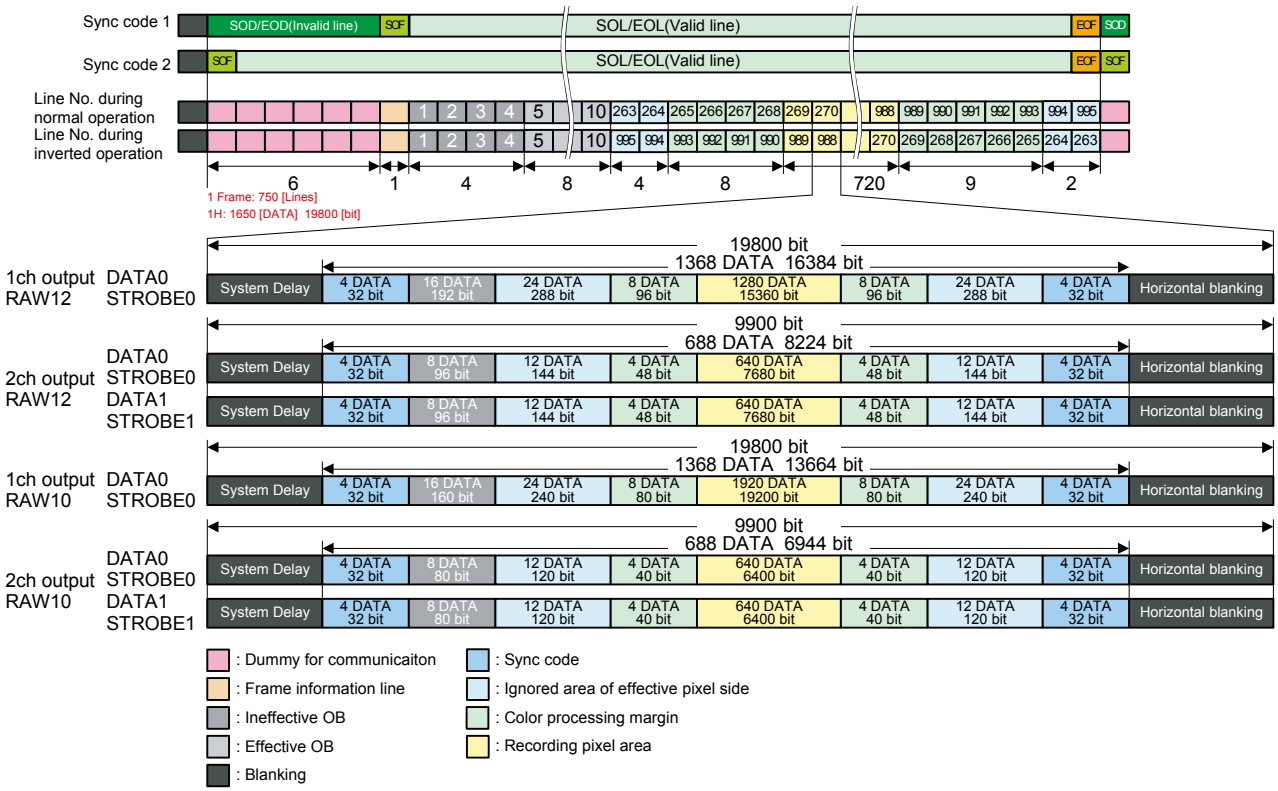
Register details			Initial value	Setting value			Function
				10 bit		12 bit	
Register name	Address	Bit		30 [frame/s]	60 [frame/s]	30 [frame/s]	
MODE	02h	[3:0]	00h	1h			HD720 p mode
HMAX	03h	[7:0]	044Ch	0672h	0339h	0672h	Horizontal (H) direction clock number designation.
	04h	[5:0]					
VMAX	05h	[7:0]	04E2h	02EEh			Vertical (V) direction line number designation.
	06h	[7:0]					
FRSEL	11h	[2:0]	0h	1h	0h	1h	Output data rate designation.
OPORTSEL		[4:3]	1h	0h	0h	0h	Parallel CMOS SDR output.
				1h	1h	1h	Parallel CMOS DDR output
				2h	N/A	2h	Serial LVDS 1ch output.
				3h	3h	3h	Serial LVDS 2ch output.
M12BEN		[6:5]	0h	0h			Output gradation setting
ADRES	12h	[1]	0h	0h		1h	AD gradation setting.
WINPH	14h	[7:0]	000h	140h			Designation of upper left coordinate for cropping position (Horizontal)
	15h	[3:0]					
WINPV	16h	[7:0]	000h	0F0h			Designation of upper left coordinate for cropping position (Vertical)
	17h	[3:0]					
WNIWH	18h	[7:0]	7C0h	540h			Cropping size designation (Horizontal)
	19h	[3:0]					
WINWV	1Ah	[7:0]	4C9h	2E9h			Cropping size designation (Vertical)
	1Bh	[3:0]					
10BITA	21h	[7]	0	1	0		Adjustments register for each operation mode.
720PMODE	22h	[7]	0	1			Sets in 720 p mode only.
10BITB	7Ah	[7:0]	00h	40h	00h		Adjustments register for each operation mode.
10BITC	7Bh	[7:0]	00h	02h	00h		
10B1080 P	98h	[7:0]	226h	226h			
	99h	[3:0]					
12B1080 P	9Ah	[7:0]	44Ch	44Ch			
	9Bh	[3:0]					
PRES	CEh	[6:0]	16h	00h		40h	
DRES	CFh	[7:0]	082h	000h		181h	
	D0h	[0]					



Pixel Array Image Drawing in HD720 p Mode



Drive Timing Chart for Parallel CMOS Output in HD720 p Mode



Drive Timing Chart for Serial LVDS Output in HD720 p Mode

Window Cropping Mode

Sensor signals are cut out and read out in arbitrary positions.
Use a fixed window cropping size and position. When changing the size or the position, set via the all-pixel scan mode.
In addition, when returning to all-pixel scan mode after setting window cropping mode, return WINPH, WINPV, WINWH and WINWV to the initial values.

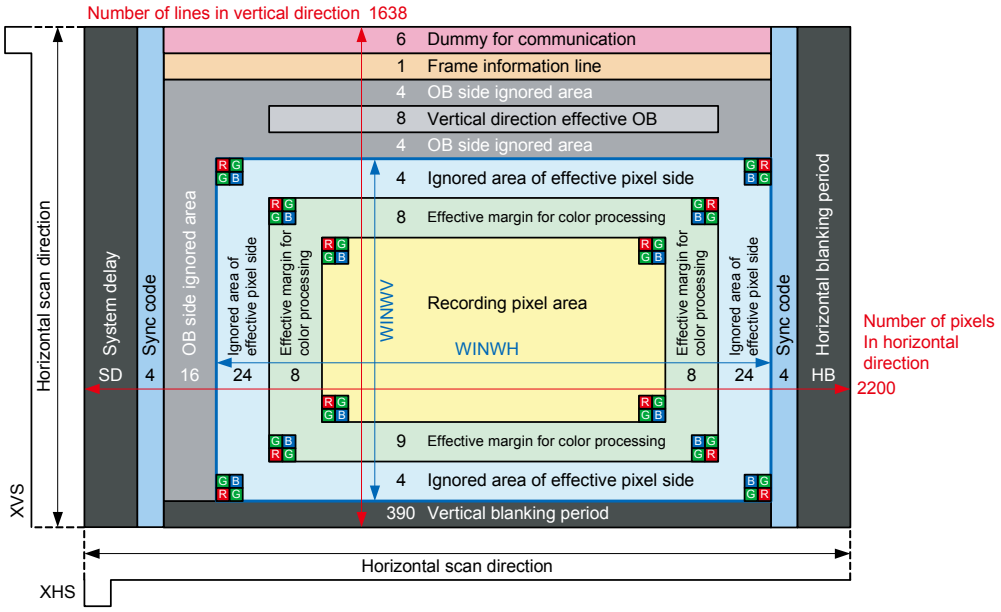
List of Window Cropping Mode Setting Registers

Register details			Initial value	Setting value			Function
				10 bit		12 bit	
Register name	Address	Bit		14.985 [frame/s]	29.97 [frame/s]	14.985 [frame/s]	
MODE	02h	[3:0]	00h	2h			Window cropping mode
HMAX	03h	[7:0]	044Ch	0898h	044Ch	0898h	Horizontal (H) direction clock number designation.
	04h	[5:0]					
VMAX	05h	[7:0]	04E2h	0666h			Vertical (V) direction line number designation.
	06h	[7:0]					
FRSEL	11h	[2:0]	0h	1h	0h	1h	Output data rate designation.
OPORTSEL		[4:3]	1h	0h	N/A	0h	Parallel CMOS SDR output.
				1h	1h	1h	Parallel CMOS DDR output
				2h	N/A	2h	Serial LVDS 1ch output.
				3h	3h	3h	Serial LVDS 2ch output.
M12BEN		[6:5]	0h	0h			Output gradation setting.
ADRES	12h	[1]	0h	0h		1h	AD gradation setting.
WINPH	14h	[7:0]	000h	0A0h(UXGA)*1,3			Designation of upper left coordinate for cropping position (Horizontal)
	15h	[3:0]					
WINPV	16h	[7:0]	000h	000h(UXGA)*1,3			Designation of upper left coordinate for cropping position (Vertical)
	17h	[3:0]					
WNIWH	18h	[7:0]	7C0h	680h(UXGA)*2,3			Cropping size designation (Horizontal)
	19h	[3:0]					
WINWV	1Ah	[7:0]	4C9h	4C9h(UXGA)*2,3			Cropping size designation (Vertical)
	1Bh	[3:0]					
10BITA	21h	[7]	0	1	0		Adjustments register for each operation mode.
720PMODE	22h	[7]	0	0			Sets in 720 p mode only.
							Adjustments register for each operation mode.
10BITB	7Ah	[7:0]	00h	40h	00h		
10BITC	7Bh	[7:0]	00h	02h	00h		
10B1080 P	98h	[7:0]	226h	44Ch	226h		
	99h	[3:0]					
12B1080 P	9Ah	[7:0]	44Ch	44Ch			
	9Bh	[3:0]					
PRES	CEh	[6:0]	16h	16h		40h	
DRES	CFh	[7:0]	082h	082h		181h	
	D0h	[0]					

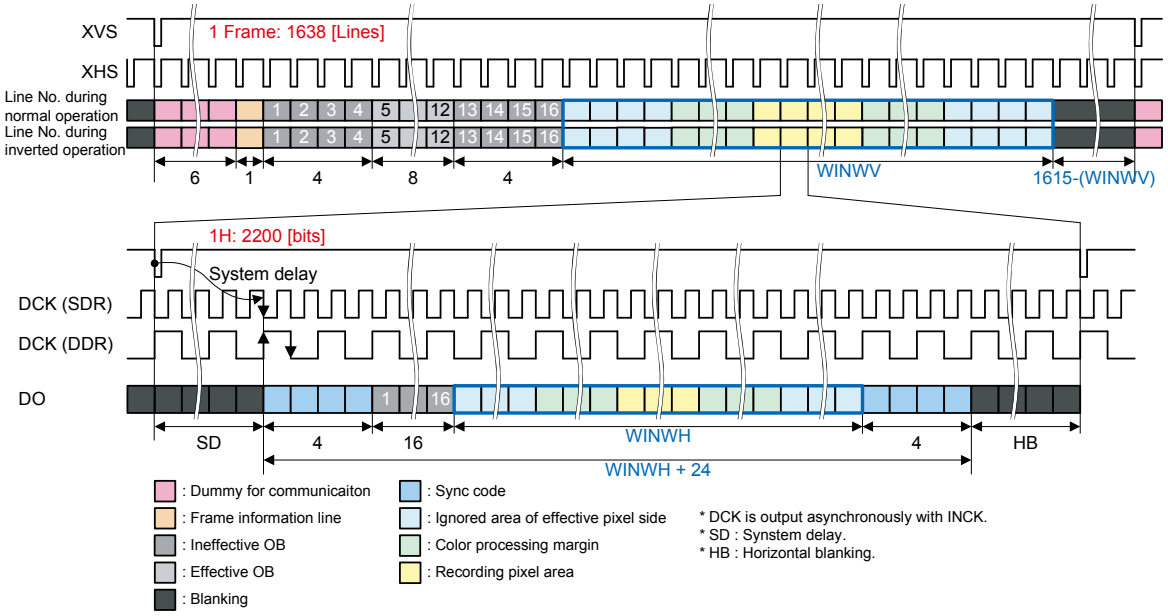
*1 The start position designation should satisfy the following conditions.
WINPH + WINWH < 7C0h
WINPV + WINWV < 4C9h

*2 Set the cropping size setting values as follows.
Horizontal direction: Multiple of 16
Vertical direction: Multiple of 4

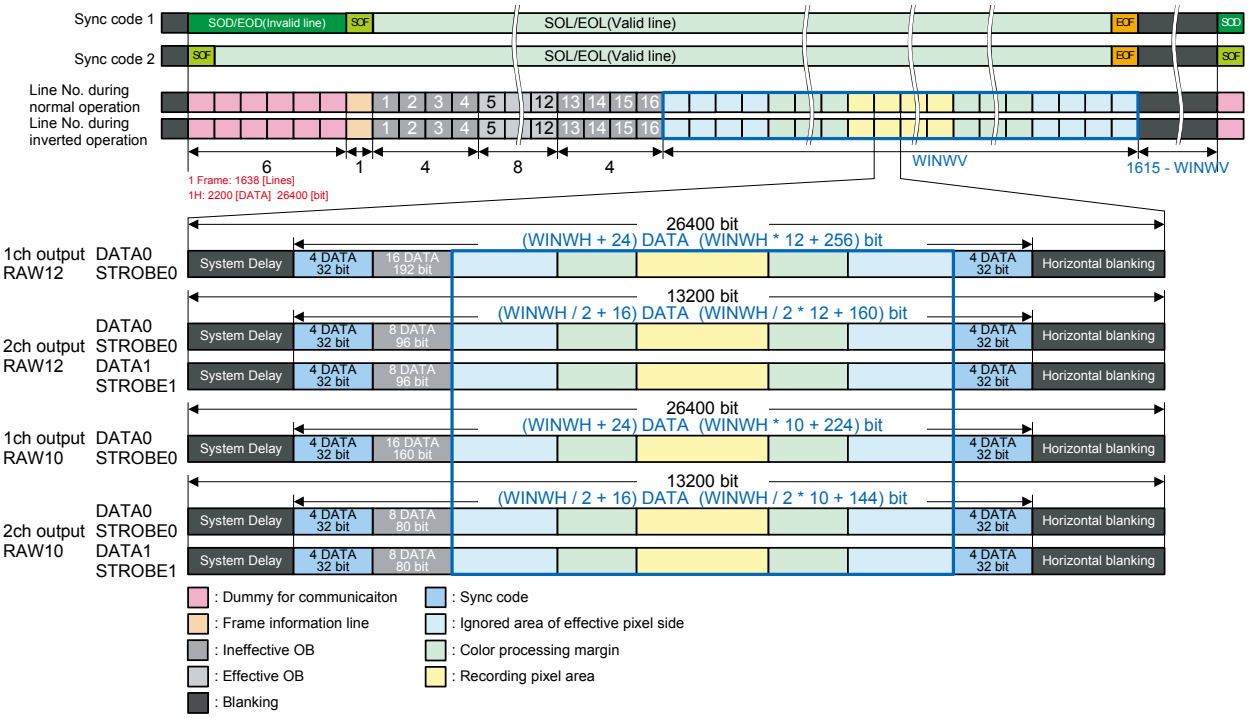
*3 Return to the initial values when transitioning from window cropping mode to all-pixel scan mode.



Pixel Array Image Drawing in Window Cropping Mode



Drive Timing Chart for Parallel CMOS Output in Window Cropping Mode



Drive Timing Chart for Serial LVDS Output in Window Cropping Mode

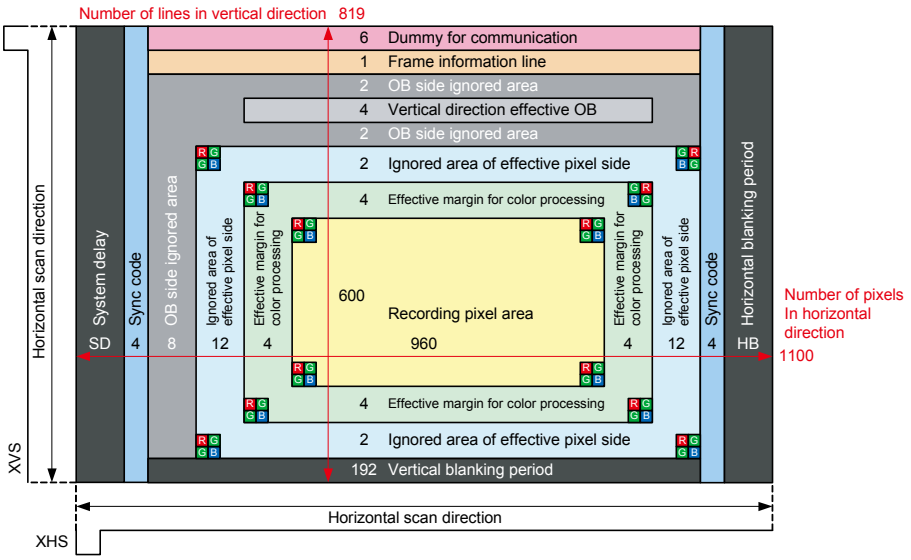
2 × 2 Binning Readout Mode

Sensor signals are read out by binning of 2 vertical pixels and 2 horizontal pixels.

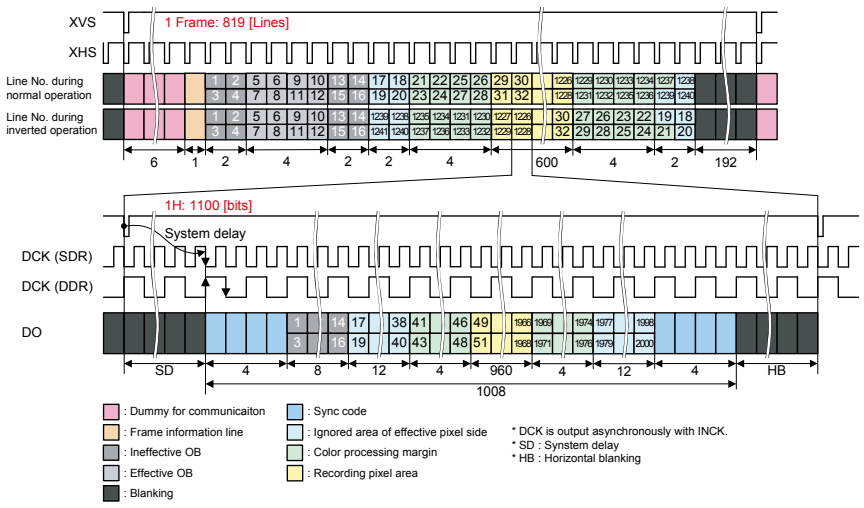
Note) The pixel signals are A/D converted to 10 bits, and 12-bit output is performed by digital binning of 4 same-color pixels.

List of 2 × 2 Binning Readout Mode Setting Registers

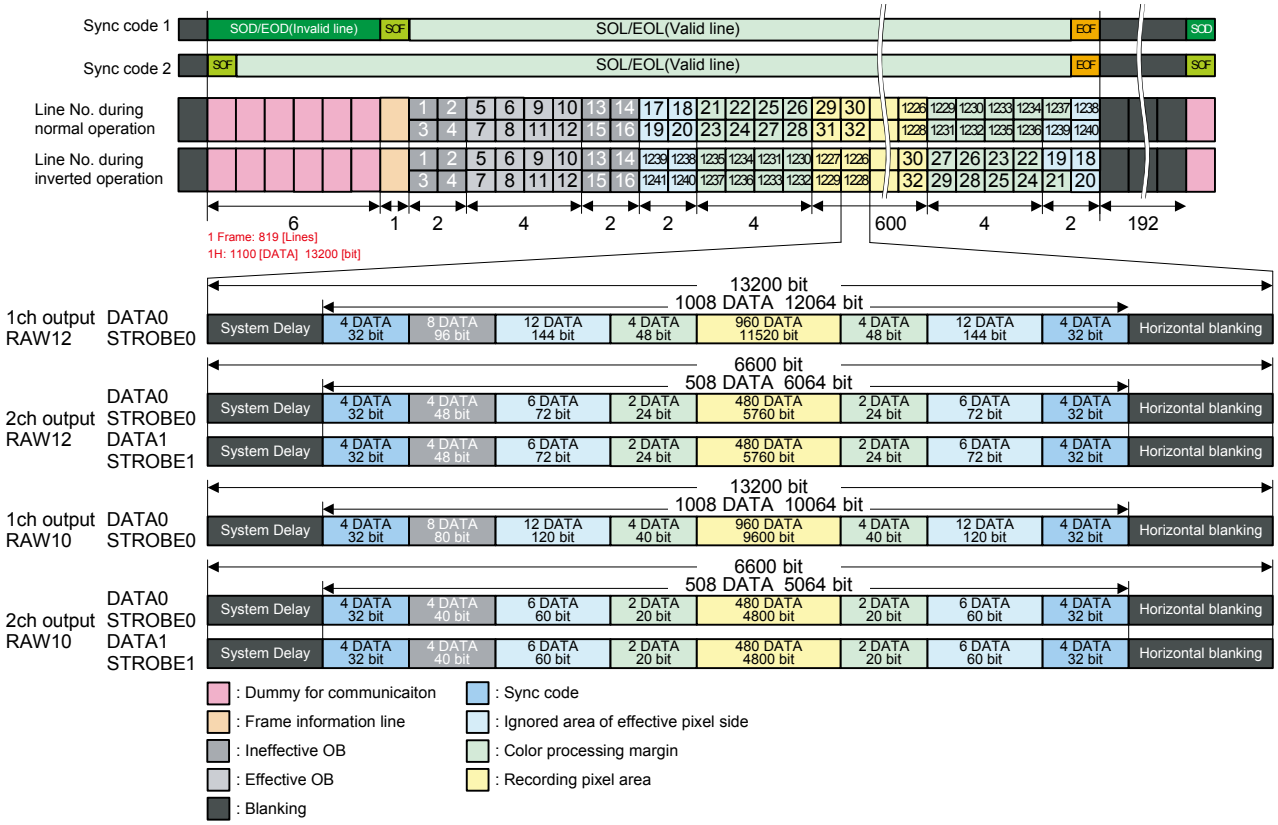
Register details			Initial value	Setting value				Function
				10 bit		12 bit		
Register name	Address	Bit		14.985 [frame/s]	29.97 [frame/s]	14.985 [frame/s]	29.97 [frame/s]	
MODE	02h	[3:0]	00h	3h				All-pixel mode
HMAX	03h	[7:0]	044Ch	1130h	0898h	1130h	0898h	Horizontal (H) direction clock number designation.
	04h	[5:0]						
VMAX	05h	[7:0]	04E2h	0333h				Vertical (V) direction line number designation.
	06h	[7:0]						
FRSEL	11h	[2:0]	0h	3h	2h	3h	2h	Output data rate designation.
OPORTSEL		[4:3]	1h	0h	0h	0h	0h	Parallel CMOS SDR output.
				1h	1h	1h	1h	Parallel CMOS DDR output
				2h	2h	2h	2h	Serial LVDS 1ch output.
				3h	3h	3h	3h	Serial LVDS 2ch output.
M12BEN		[6:5]	0h	2h		0h		Output gradation setting
ADRES	12h	[1]	0h	0h				AD gradation setting.
WINPH	14h	[7:0]	000h	000h				Designation of upper left coordinate for cropping position (Horizontal)
	15h	[3:0]						
WINPV	16h	[7:0]	000h	000h				Designation of upper left coordinate for cropping position (Vertical)
	17h	[3:0]						
WNIWH	18h	[7:0]	7C0h	7C0h				Cropping size designation (Horizontal)
	19h	[3:0]						
WINWV	1Ah	[7:0]	4C9h	4C9h				Cropping size designation (Vertical)
	1Bh	[3:0]						
10BITA	21h	[7]	0	1	0			Adjustments register for each operation mode.
720PMODE	22h	[7]	0	0				Sets in 720 p mode only.
10BITB	7Ah	[7:0]	00h	40h	00h			Adjustments register for each operation mode.
10BITC	7Bh	[7:0]	00h	02h	00h			
10B1080 P	98h	[7:0]	226h	44Ch	226h	44Ch	226h	
	99h	[3:0]						
12B1080 P	9Ah	[7:0]	44Ch	44Ch				
	9Bh	[3:0]						
PRES	CEh	[6:0]	16h	16h				
DRES	CFh	[7:0]	082h	082h				
	D0h	[0]						



Pixel Array Image Drawing in 2 × 2 Binning Readout Mode



Drive Timing Chart for Parallel CMOS Output in 2 × 2 Binning Readout Mode



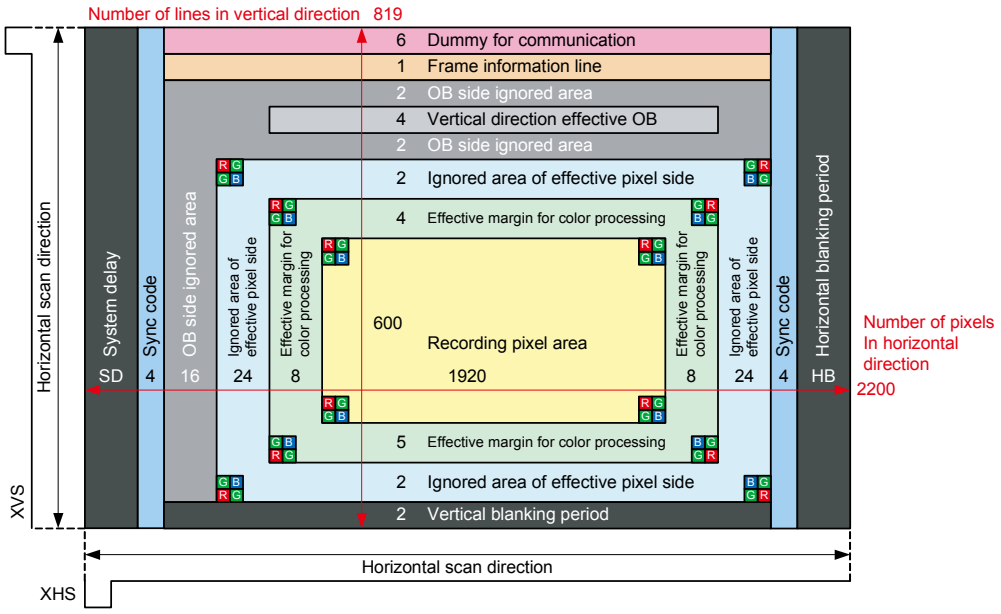
Drive Timing Chart for Serial LVDS Output in 2 × 2 Binning Readout Mode

Vertical 1/2 Subsampling Mode

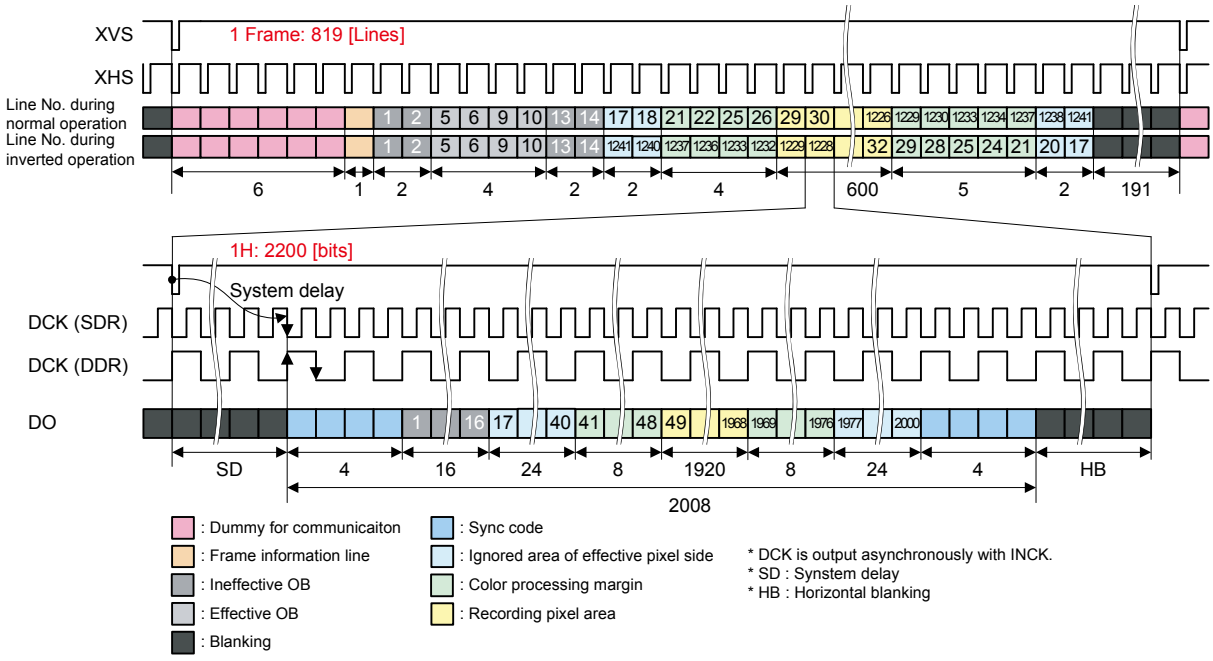
The sensor signal is read by eliminating it in vertical direction.

Register List of Vertical 1/2 Subsampling Mode Setting

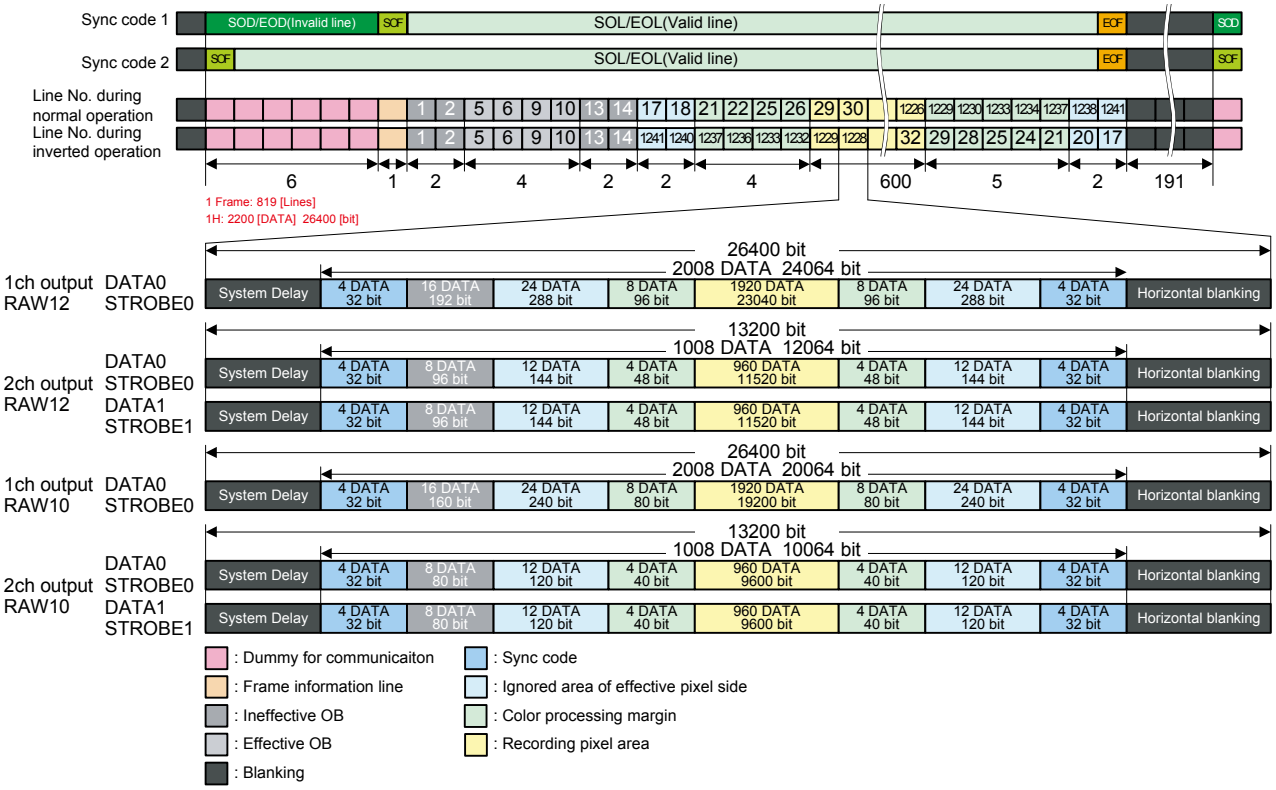
Register details			Initial value	Setting value			Function
				10 bit		12 bit	
Register name	Address	bit		29.97 [frame/s]	59.94 [frame/s]	29.97 [frame/s]	
MODE	02h	[3:0]	00h	4h			Vertical 1/2 subsampling mode
HMAX	03h	[7:0]	044Ch	0898h	044Ch	0898h	Horizontal (H) direction clock number designation
	04h	[5:0]					
VMAX	05h	[7:0]	04E2h	0333h			Vertical (V) direction line number designation
	06h	[7:0]					
FRSEL	11h	[2:0]	0h	1h	0h	1h	Output data rate designation
OPORTSEL		[4:3]	1h	0h	N/A	0h	Parallel CMOS SDR output
				1h	1h	1h	Parallel CMOS DDR output
				2h	N/A	2h	Serial LVDS 1ch output
				3h	3h	3h	Serial LVDS 2ch output
M12BEN		[6:5]	0h	0h			Output gradation setting
ADRES	12h	[1]	0h	0h		1h	AD gradation setting
WINPH	14h	[7:0]	000h	000h			Designation of upper left coordinate for cropping position (Horizontal)
	15h	[3:0]					
WINPV	16h	[7:0]	000h	000h			Designation of upper left coordinate for cropping position (Vertical)
	17h	[3:0]					
WNIWH	18h	[7:0]	7C0h	7C0h			Cropping size designation (Horizontal)
	19h	[3:0]					
WINWV	1Ah	[7:0]	4C9h	4C9h			Cropping size designation (Vertical)
	1Bh	[3:0]					
10BITA	21h	[7]	0	1	0		Adjustments register for each operation mode.
720PMODE	22h	[7]	0	0			Sets in 720 p mode only.
10BITB	7Ah	[7:0]	00h	40h	00h		Adjustments register for each operation mode.
10BITC	7Bh	[7:0]	00h	02h	00h		
10B1080 P	98h	[7:0]	226h	44Ch	226h		
	99h	[3:0]					
12B1080 P	9Ah	[7:0]	44Ch	44Ch			
	9Bh	[3:0]					
PRES	CEh	[6:0]	16h	16h		40h	
DRES	CFh	[7:0]	082h	082h		181h	
	D0h	[0]					



Pixel Array Image Drawing in Vertical 1/2 Subsampling Mode



Drive Timing Chart for Parallel CMOS Output in Vertical 1/2 Subsampling Mode



Drive Timing Chart for Serial LVDS Output in Vertical 1/2 Subsampling Mode

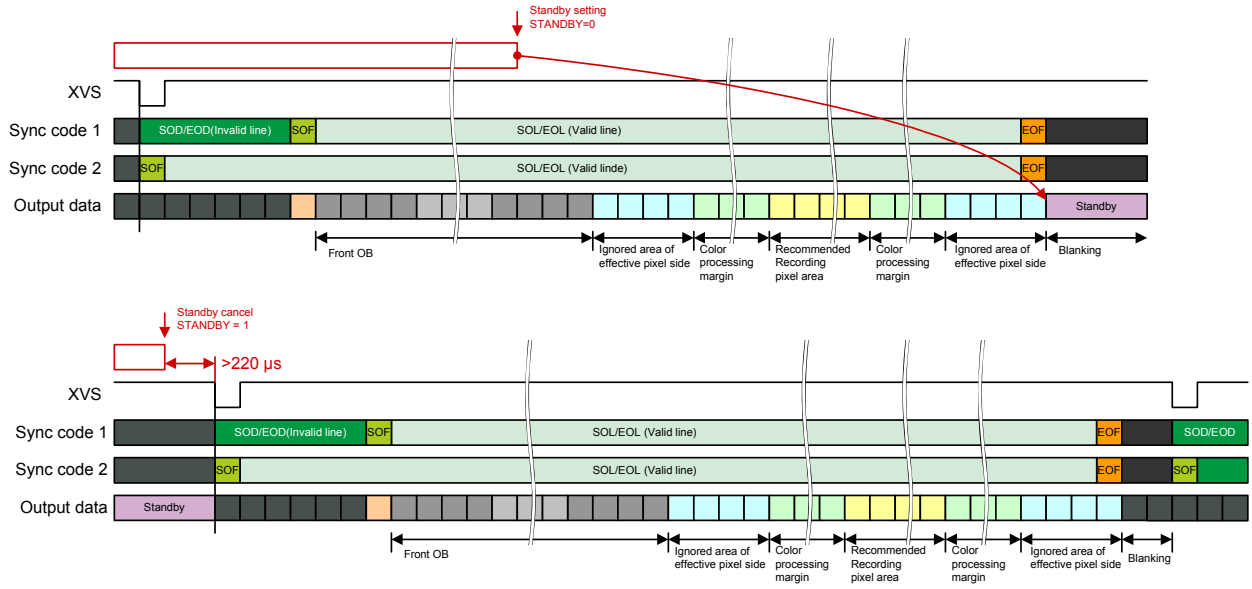
Description of Various Functions

Standby mode

This sensor stops its operation and goes into standby mode which reduces the power consumption by writing “1” to the standby control register STANDBY (address 00h, Bit [0]). (Standby mode immediately after power-on and reset)
Standby mode is reflected after V. OB after the set frame.
Write to register is possible because the serial communication function operates even in standby mode.
Set the STANDBY register to “0” to cancel standby mode. The standby cancel is immediately reflected from the communication.

List of Standby Mode Setting

Register details			Initial value	Setting value	Status		Remarks
Register name	Address	Bit			Digital circuit	Analog circuit	
STANDBY	00h	[0]	1	1 (Standby)	Stop	Stop	Register communication is executed even in standby mode.
				0	Operate	Operate	



Standby Mode Change Timing

Slave Mode and Master Mode

The sensor can be switched between slave mode and master mode. The switching is made by the XMASTER pin.
Set the XMSTA register (address 2Ch [0]) to “0” in order to start the operation after setting to master mode.
In addition, set the count number of sync signal in vertical direction by the VMAX register (address 05h [7:0], 06h [7:0]) and the clock number in horizontal direction by the HMAX register (address 03h [7:0], 04h [5:0]).
See the description of Operation Mode for details of drive mode.

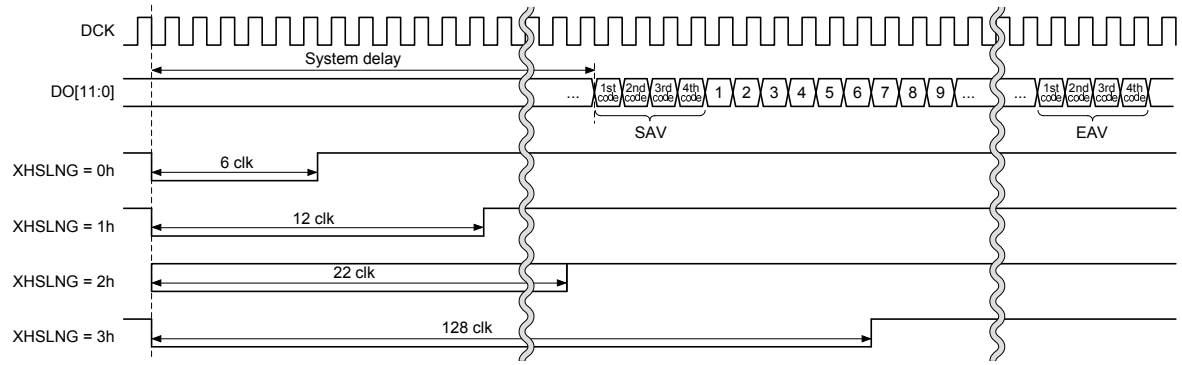
List of Slave and Master Mode Setting (e.g. All pixels 19.64 frame/s)

Pin name	Pin processing	Operation mode	Remarks
XMASTER pin	Low fixed	Master Mode	High: 1.8 V Low: GND
	High fixed	Slave Mode	

Description of register			Initial value	Setting value	Status	Remarks
Register name	Address	Bit			Master Mode	
XMSTA	2Ch	[0]	1	0	Master operation start	The master operation starts by setting to 0.
				1	Master operation ready	
XHSLNG	21h	[5:4]	0	See the diagram.		XHS width designated (XVS reference output)
XVSLNG	22h	[2:0]	0			XVS width designated
VMAX	05h	[7:0]	4E2h	See the each item in Operation Mode.		Line number per frame designated
	06h	[7:0]				
HMAX	03h	[7:0]	44Ch			Clock number per frame designated
	04h	[5:0]				

XHSLNG Selection

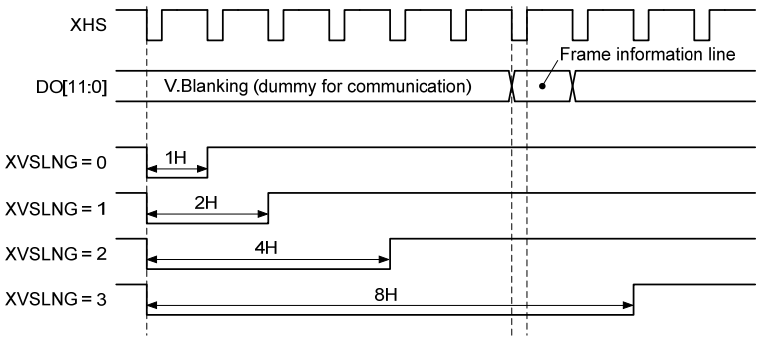
The signal of horizontal sync signal XHS is set by the XHSLNG register. The output has system delay from the XHS fall to effective data (sync code) output.



List of XHS Pulse Width Setting

XVSLNG Selection

The signal of vertical sync signal XVS is set.

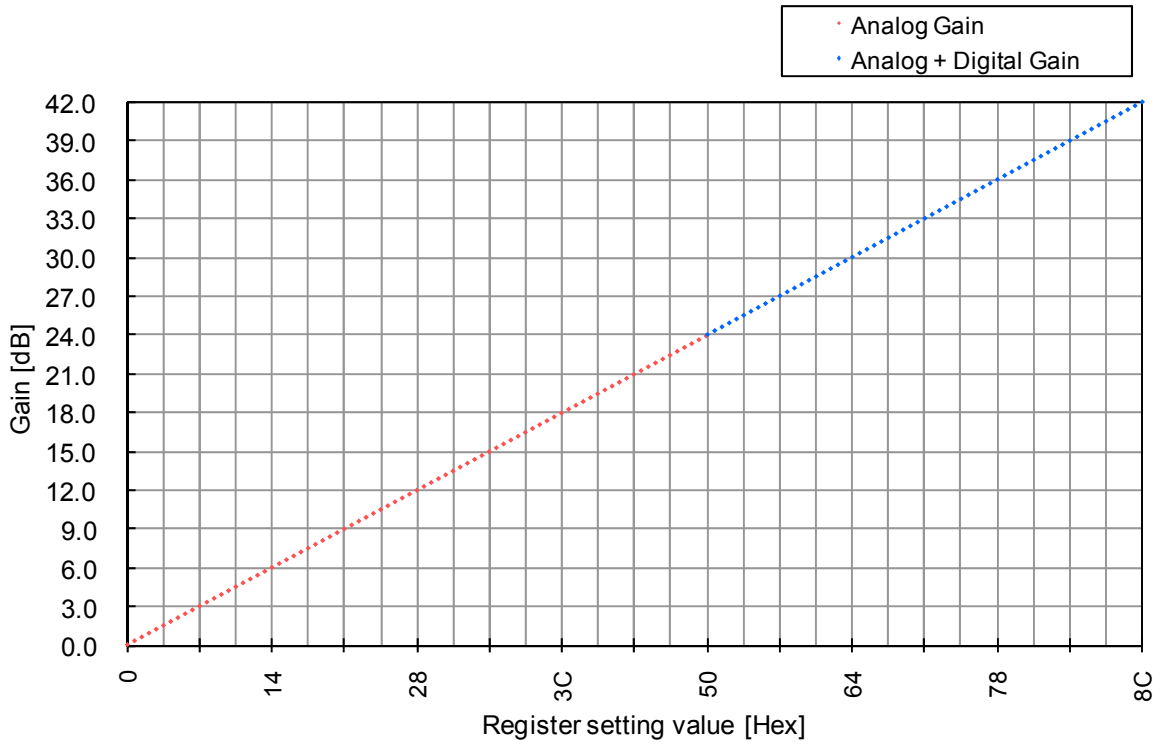


List of XVS Pulse Width Setting

Gain Adjustment Function

The Programmable Gain Control (PGC) of this device consists of the analog block and digital block.
The total of analog gain and digital gain can be set up to 42 dB by the GAIN register (address 1Eh [7:0]) setting.

See the List of Gain Setting Register Value for Each Register.



List of PGC Register

Register details			Initial value	Setting value		Remarks
Register name	Address	Bit		Min.	Max.	
GAIN	1Eh	[7:0]	00h	00h	8Ch	See the next page.

List of Gain Setting Register Value

Gain [dB]	GAIN [7:0]	Gain [dB]	GAIN [7:0]	Gain [dB]	GAIN [7:0]
0.0	0h	14.1	2Fh	28.2	5Eh
0.3	1h	14.4	30h	28.5	5Fh
0.6	2h	14.7	31h	28.8	60h
0.9	3h	15.0	32h	29.1	61h
1.2	4h	15.3	33h	29.4	62h
1.5	5h	15.6	34h	29.7	63h
1.8	6h	15.9	35h	30.0	64h
2.1	7h	16.2	36h	30.3	65h
2.4	8h	16.5	37h	30.6	66h
2.7	9h	16.8	38h	30.9	67h
3.0	Ah	17.1	39h	31.2	68h
3.3	Bh	17.4	3Ah	31.5	69h
3.6	Ch	17.7	3Bh	31.8	6Ah
3.9	Dh	18.0	3Ch	32.1	6Bh
4.2	Eh	18.3	3Dh	32.4	6Ch
4.5	Fh	18.6	3Eh	32.7	6Dh
4.8	10h	18.9	3Fh	33.0	6Eh
5.1	11h	19.2	40h	33.3	6Fh
5.4	12h	19.5	41h	33.6	70h
5.7	13h	19.8	42h	33.9	71h
6.0	14h	20.1	43h	34.2	72h
6.3	15h	20.4	44h	34.5	73h
6.6	16h	20.7	45h	34.8	74h
6.9	17h	21.0	46h	35.1	75h
7.2	18h	21.3	47h	35.4	76h
7.5	19h	21.6	48h	35.7	77h
7.8	1Ah	21.9	49h	36.0	78h
8.1	1Bh	22.2	4Ah	36.3	79h
8.4	1Ch	22.5	4Bh	36.6	7Ah
8.7	1Dh	22.8	4Ch	36.9	7Bh
9.0	1Eh	23.1	4Dh	37.2	7Ch
9.3	1Fh	23.4	4Eh	37.5	7Dh
9.6	20h	23.7	4Fh	37.8	7Eh
9.9	21h	24.0	50h	38.1	7Fh
10.2	22h	24.3	51h	38.4	80h
10.5	23h	24.6	52h	38.7	81h
10.8	24h	24.9	53h	39.0	82h
11.1	25h	25.2	54h	39.3	83h
11.4	26h	25.5	55h	39.6	84h
11.7	27h	25.8	56h	39.9	85h
12.0	28h	26.1	57h	40.2	86h
12.3	29h	26.4	58h	40.5	87h
12.6	2Ah	26.7	59h	40.8	88h
12.9	2Bh	27.0	5Ah	41.1	89h
13.2	2Ch	27.3	5Bh	41.4	8Ah
13.5	2Dh	27.6	5Ch	41.7	8Bh
13.8	2Eh	27.9	5Dh	42.0	8Ch

Black Level Adjustment Function

The black level offset (offset variable range: 03Ch to 1FFh) can be added relative to the data in which the digital gain modulation was performed by the BLKLEVEL register (address: 20h [7:0], 21h [0]). When the BLKLEVEL setting is increased by 1 LSB, the black level is increased by 1 LSB.

Use with values shown below is recommended.
10-bit output: 3Ch (60d)
12-bit output: F0h (240d)

List of Black Level Adjustment Register

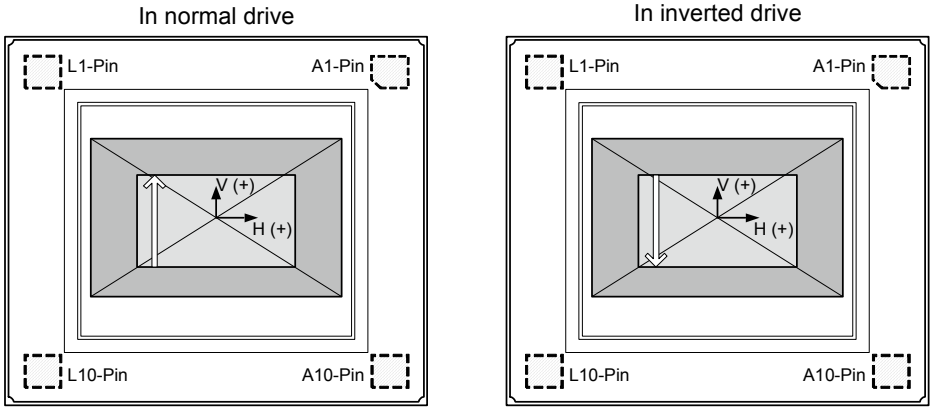
Register details			Initial value	Setting value	
Register name	Address	Bit		Min.	Max.
BLKLEVEL	20h	[7:0]	03Ch	03Ch	1FFh
	21h	[0]			

Vertical Normal Operation and Inverted Drive

The sensor readout direction (normal/inverted) in vertical direction can be switched by the VREVERSE (address 01h [0]) register setting. See the item of “Drive mode” for the order of readout lines in normal and inverted modes. One invalid frame is generated when reading immediately after the readout direction change in order to switch the normal operation and inversion between frames.

List of Vertical Drive Direction Setting Register

Register details			Initial value	Setting value	
Register name	Address	Bit		Normal	Inverted
VREVERSE	01h	[0]	0	0	1



Normal and Inverted Drive Outline in Vertical Direction

Shutter and Integration Time Settings

This sensor has a variable electronic shutter function that can control the integration time in line units. In addition, this sensor performs rolling shutter operation in which electronic shutter and readout operation are performed sequentially for each line.

Note) For integration time control, an image which reflects the setting is output from the frame after the setting changes.

Example of Integration Time Setting

The sensor's integration time is obtained by the following formula.

Integration time = 1 frame period × (SVS + 1 - SPL) - (SHS1) × (1H period) - t_{OFFSET} (However, SVS > SPL)

Note) 1. The frame period is determined by the input XVS when the sensor is operating in slave mode, or the register VMAX value in master mode. The frame period is designated in 1H units, so the time is determined by (Number of lines × 1H period).
2. See “Drive Modes” for the 1H period.
3. t_{OFFSET} is the integration time error. Substitute the value below in the formula of integration time.

Operation mode	t_{OFFSET} [H]
All-pixel scan mode HD1080 p mode (10 bit-15 frame/s, 10 bit-30 frame/s, 12 bit-15 frame/s) Window cropping mode Vertical 1/2 subsampling mode	0.3
HD1080 p mode (12 bit 30 frame/s) 2 x 2 binning mode	0.1

In this item, the shutter operation and integration time are shown as in the figure below with the time sequence on the horizontal axis and the vertical address on the vertical axis. For simplification, shutter and readout operation are noted in line units.

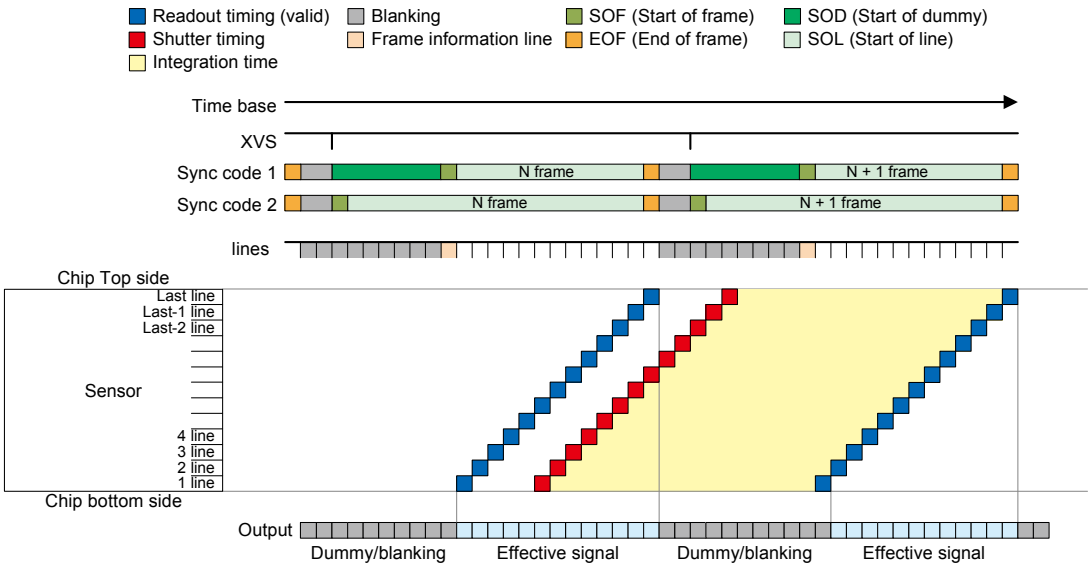


Image Drawing of Shutter Operation

Normal Exposure Operation (Controlling the Integration Time in 1H Units)

The integration time can be controlled by varying the electronic shutter timing. In the electronic shutter settings, the integration time is controlled by the SHS1 register (address: 08h [7:0], 09h [7:0]).

Set SHS1 to a value between 0 and (Number of lines per frame - 1). When the sensor is operating in slave mode, the number of lines per frame is determined by the XVS interval (number of lines), using the input XHS interval as the line unit.
When the sensor is operating in master mode, the number of lines per frame is determined by the VMAX register (address: 05h [7:0], 06h [7:0]).
The number of lines per frame varies according to the drive mode.

Registers Used to Set the Integration Time in 1H Units

Register details			Initial value	Description
Register name	Address	Bit		
SHS1	08h	[7:0]	0000h	Sets the shutter sweep time.
	09h	[7:0]		
VMAX	05h	[7:0]	04E2h	Sets the number of lines per frame (only in master mode). See “Operating Modes” for the setting value in each mode.
	06h	[7:0]		

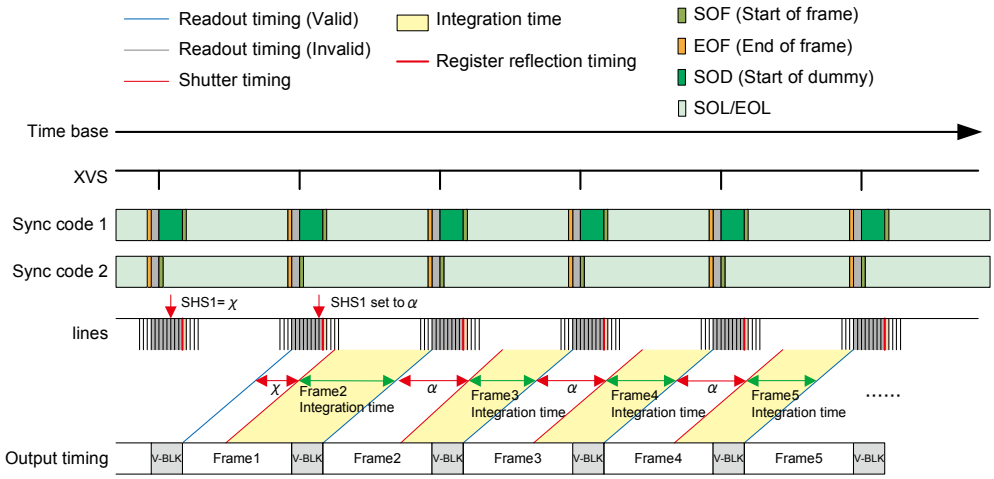


Image Drawing of Integration Time Control within a Frame

Long Exposure Operation (Control by Expanding the Number of Lines per Frame)

Long exposure operation can be performed by lengthening the frame period.
When the sensor is operating in slave mode, this is done by lengthening the input vertical sync signal (XVS) pulse interval.
When the sensor is operating in master mode, it is done by designating a larger register VMAX (address: 05h [7:0], 06h [7:0]) value compared to normal operation.
Likewise, in slave mode the integration time can be increased by lengthening the input XVS signal pulse interval.
When the integration time is extended by increasing the number of lines, the rear V blanking increases by an equivalent amount.

The maximum VMAX and SHS1 values are 65535d. When the number of lines per frame is set to the maximum value, the integration time in all-pixel scan mode at 19.64 frame/s is approximately 2.7 s.
When set to a number of V lines or more than that noted for each readout drive mode, the imaging characteristics are not guaranteed during long exposure operation.

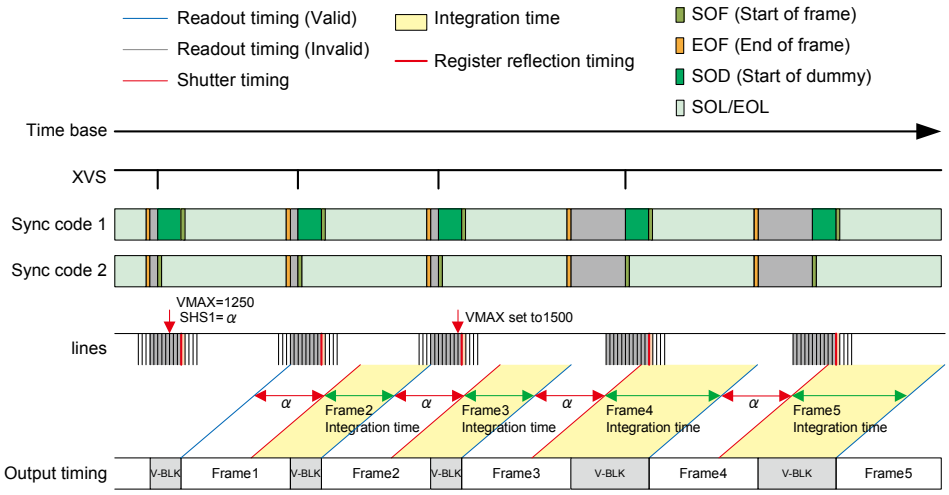


Image Drawing of Long Exposure Time Control by Adjusting the Frame Period

Long Exposure Operation (Controlling the Integration Time in Frame Units)

When setting a long exposure that extends the integration time to one frame or more, set the SVS register (address: 06h [7:0], 07h [1:0]) to the value of (Number of integration frames - 1). In addition, the frame in which the shutter operates is designated by the SPL register (address: 0Dh [7:0], 0Eh [1:0]). To further adjust the integration time in 1H units within the frame set by SPL, set the SHS1 register. However, note that performing long integration causes the readout timing and the setting reflection timing to be eliminated according to the value set by SVS, so the frame rate drops. The blanking signal is output in data corresponding to the drop in the frame rate.

- ◆This description is for the settings in master mode. In slave mode, long integration is set by eliminating the input vertical sync signal (XVS) pulse.
- ◆When set so that SVS < SPL, the SPL setting value is ignored, and the signal is stored for the number of frames designated by SVS.
- ◆Set SHS1 to a value between 0 and (Number of lines per frame - 7).
- ◆During long exposure operation, register communication is also reflected at the eliminated timing. To forcibly end operation partway, use the shutter break function.
- ◆The imaging characteristics are not guaranteed during long exposure operation that performs integration for two frames or more.

Registers Used to Set the Integration Time in Frame Units

Register details			Initial value	Description
Register name	Address	Bit		
SSBRK	1Bh	[0]	1h	Shutter break function Set both SVS and SPL to “0” simultaneously with this setting.
SVS	07h	[7:0]	000h	Designates the number of integration frames. Integration time = Setting value + 1 frame
	08h	[1:0]		
SPL	0Dh	[7:0]	000h	Designates the number of sweep frames.
	0Eh	[1:0]		
SHS1	08h	[7:0]	0000h	Sets the shutter sweep time. Note) When SVS is set to more than 1h, SHS1 is limited to less than VMAX-7.
	09h	[7:0]		

* Integration time control is reflected to the next readout frame after the frame during which the setting was made.

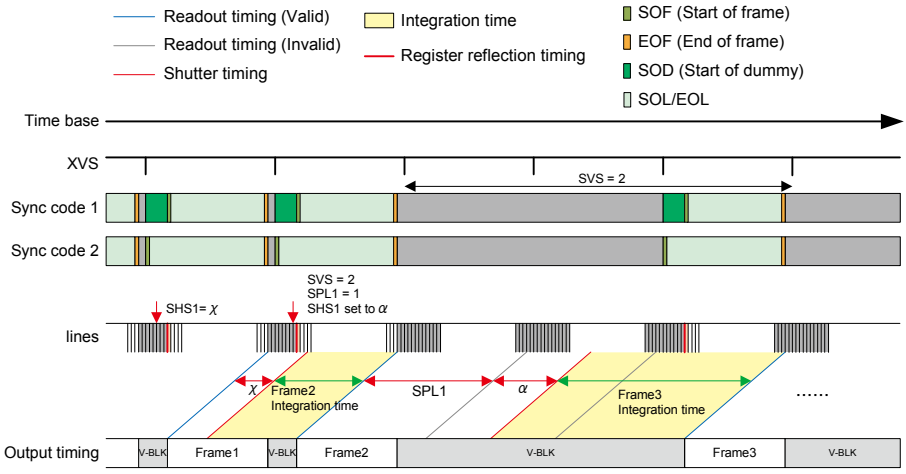


Image Drawing of Long Exposure Control in Frame Units

Example of Integration Time Setting

The example of register setting for controlling the integration time is shown below.

Example of Integration Time Setting (in all-pixel mode, t_{OFFSET}=0.3H)

Operation	Sensor setting (Register)				Integration time
	VMAX*	SVS	SPL	SHS1	
Normal frame rate	1250	0	0	1249	0.7H period
				1248	1.7H period
				:	:
				N	(1250 – N – 0.3) H period
				:	:
				1	1248.7H period
				0	1249.7H period
Long-time exposure operation (control by expanding the number of lines per frame)	1251	0	0	0	1250.7H period
	1252				1251.7H period
	:				:
	M			N	(M – N – 0.3) H period
	:			:	:
Long-time exposure operation (integration time control in frame units)	1250	1	0	N	(2499.7 – N) H period
		2			(3269.7 – N) H period
		:			:
		V			{(V + 1) × VMAX – N – 0.3} H period
		:			:
		9			(12499.7 – N) H period
			1		(11249.7 – N) H period
			2		(9999.7 – N) H period
			:		:
			L		{VMAX × (10 – L) – N – 0.3} H period
			:		:
		V	L		{VMAX × (V + 1 – L) – N – 0.3} H period

* In sensor master mode. XHS interval to be input in slave mode.

* The SHS1 setting value (N) is set to the VMAX value (M) of -7 to 0.

Shutter Break Function

When changing the integration time setting before the next reflection timing (readout timing) during long integration operation, the setting can be reflected at the normal XVS timing (when the register SVS is set to “0h”) by setting the SSBRK register (address: 12h [0]) to “01h”. The timing at which the SSBRK register is reflected conforms to the frame sequence before SVS is set.

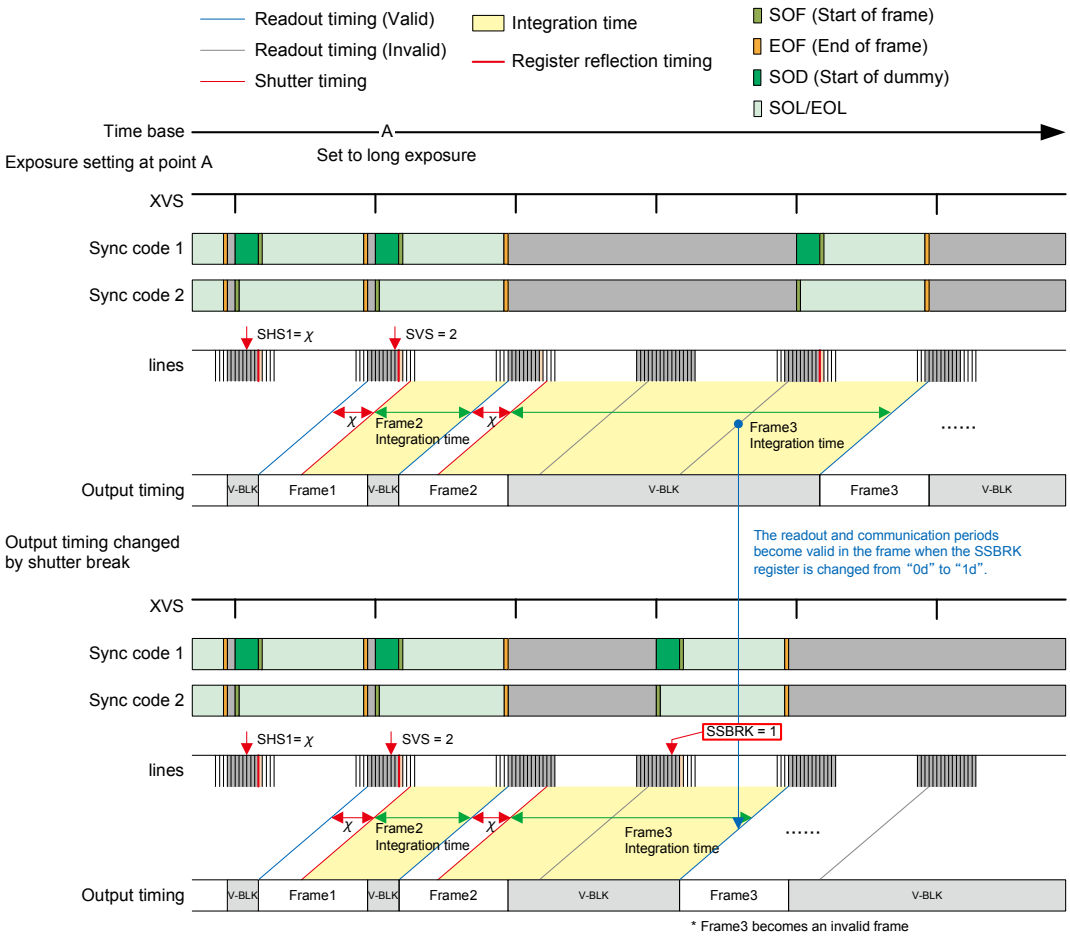
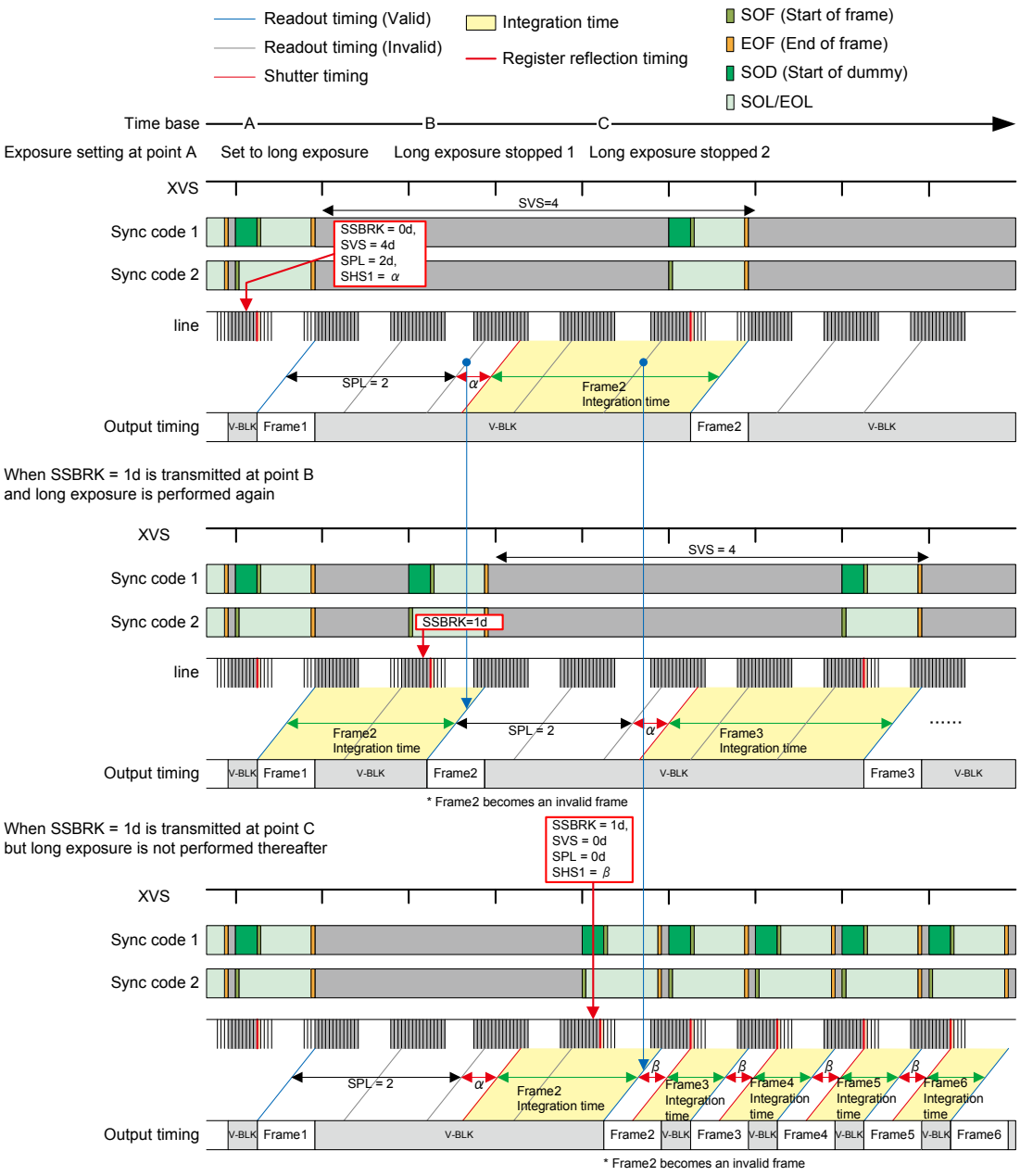


Image Drawing of Shutter Break Function

Depending on the value set when long integration operation starts (point “A” on the time base), the scheduled output can be stopped partway and settings can be changed as shown in the figure above. In this case, readout occurs in the frame when the SSBRK register is transmitted, and the signal stored up to that point is output. In this case the signal output in the frame when SSBRK is set becomes an invalid signal. In addition, perform communication at the next communication timing to return the SSBRK register to “0d”.



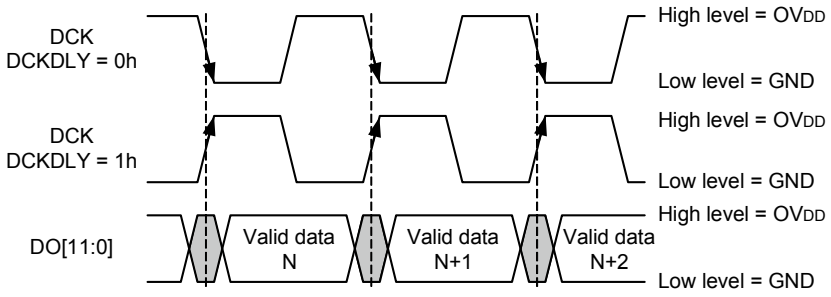
Example Showing Application of the Shutter Break Function

When the SVS and SPL register values are left unchanged after the shutter break, readout is performed and then long integration starts again. To stop long integration with shutter break, the SVS and SPL register values must both be set to “0d” during the communication period of the frame during which shutter break is performed.

Output Signal Interface Control

This sensor supports the following output formats. See “Image Data Output Format” for the data rate.
Shaded areas in the figure indicate invalid data with regards to the AC characteristics. See “AC Characteristics” for details.

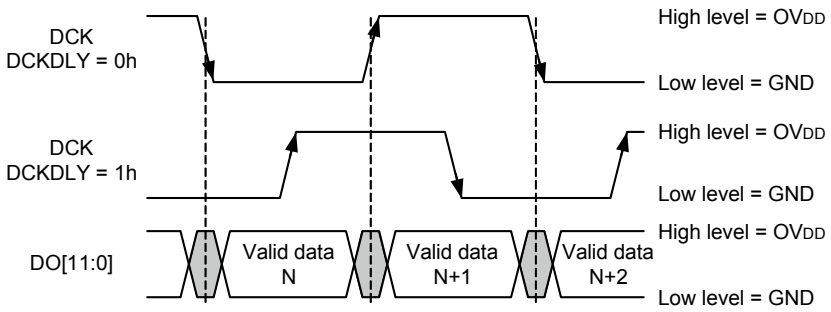
Parallel CMOS SDR Output



Example of Pin Waveform in CMOS 1-port SDR Output Mode

The sensor signal is output in sync with the falling edge of the data clock (DCK). (When DCKDLY is set to “0h”)
Output in sync with the rising edge is possible by setting DCKDLY to “1h”.

Parallel CMOS DDR Output



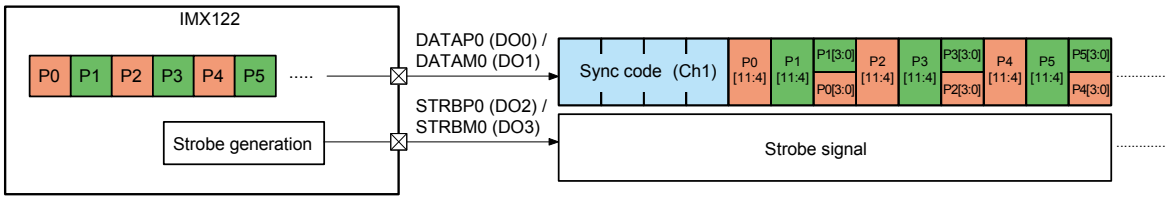
Example of Pin Waveform in CMOS 1-port DDR Output Mode

The sensor signal is output in sync with both rising and falling edges of the data clock (DCK).
(When DCKDLY is set to “0h”)
Output can be performed with the DCK phase shifted by 90 ° relative to the data by setting DCKDLY to “1h”.

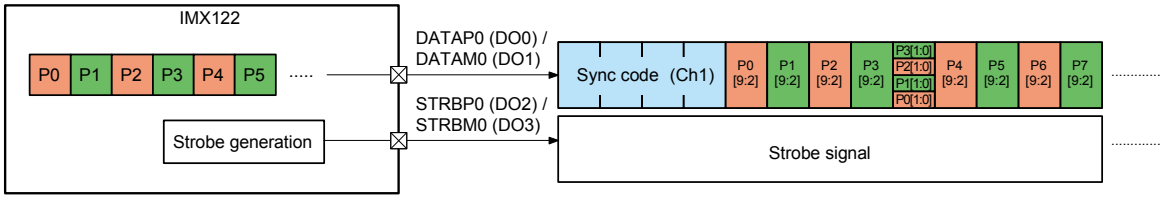
Serial LVDS Output

Serial LVDS uses a different format depending on whether the output gradation is 10 bits or 12 bits.
The data is divided into a DATA line and a STROBE line, and is output on 1 channel or divided into 2 channels.

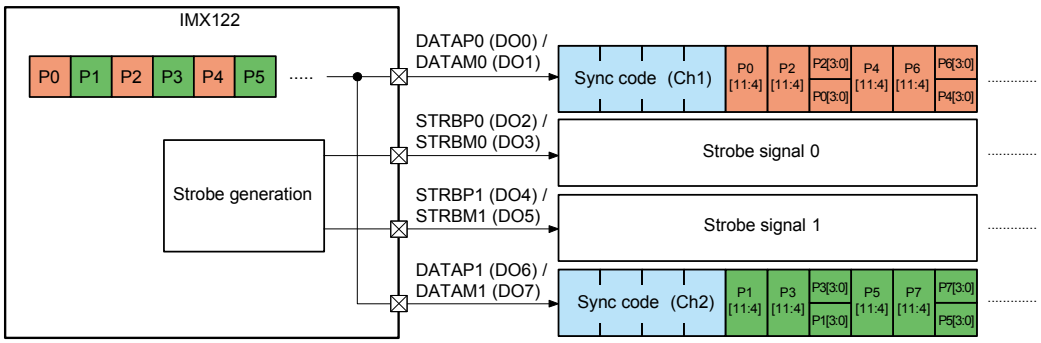
A) 1ch-RAW12 (12 bit)



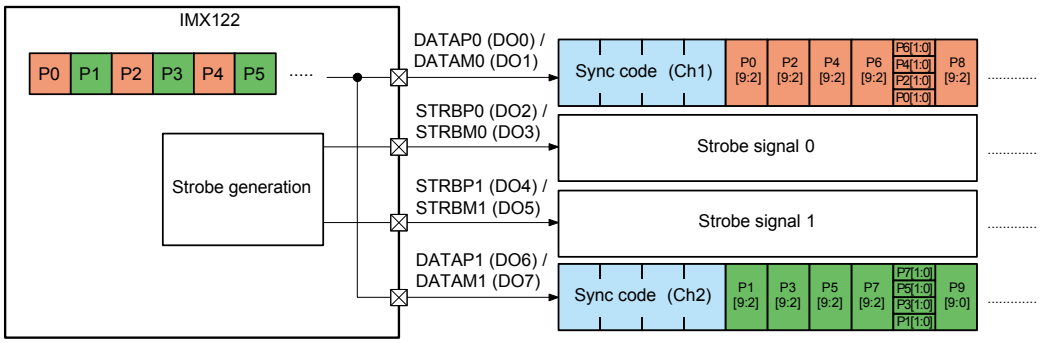
B) 1ch-RAW10 (10 bit)



C) 2ch-RAW12 (12 bit)

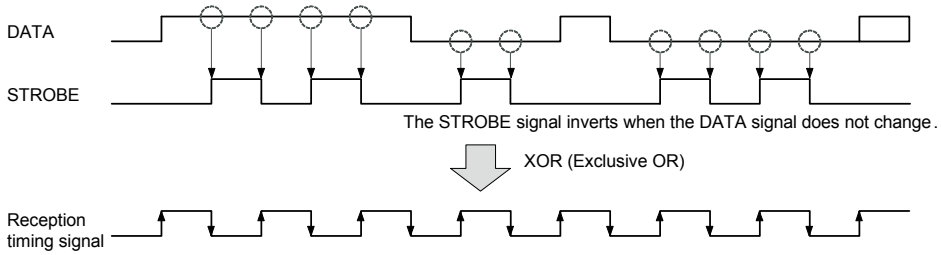


D) 2ch-RAW10 (10 bit)



List of Serial LVDS Output Formats

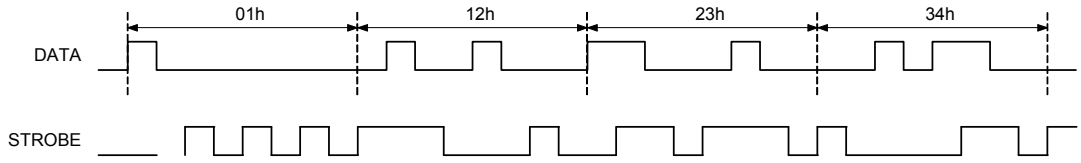
DATA-Strobe Method



DATA-Strobe Method

LVDS output uses the DATA-Strobe method. The DATA signal outputs the output data in binary format, but the STROBE signal performs toggle operation when the DATA signal does not change (0 → 0, 1 → 1).
The signal switching timing is obtained by taking the XOR (exclusive OR) of the DATA and STROBE signals.
Data is output LSB first at both the rising and falling edges of the waveform obtained by the XOR operation.

Example: When outputting 01h, 12h, 23h and 34h in order



Output sequence

Output Formats and Setting Methods

Register details			Initial value	Setting value	Description
Register name	Address	Bit			
OPORTSEL	11h	[4:3]	0	0	Parallel CMOS output, SDR output
				1	Parallel CMOS output, DDR output
				2	Serial LVDS 1ch output
				3	Serial LVDS 2ch output
ADRES	12h	[1]	0	0	In parallel CMOS output mode: 10-bit output In serial LVDS output mode: 10-bit RAW10 output
				1	In parallel CMOS output mode: 12-bit output In serial LVDS output mode: 12-bit RAW12 output
DCKDLY	2Dh	[1]	0	0	In CMOS SDR output mode: Output in sync with the falling edge In CMOS DDR output mode: Output in sync with the edge (0 °) In LVDS output mode: Setting invalid
				1	In CMOS SDR output mode: Output in sync with the rising edge In CMOS DDR output mode: Output with the phase delayed by 90 ° In LVDS output mode: Setting invalid

Output Signal Range

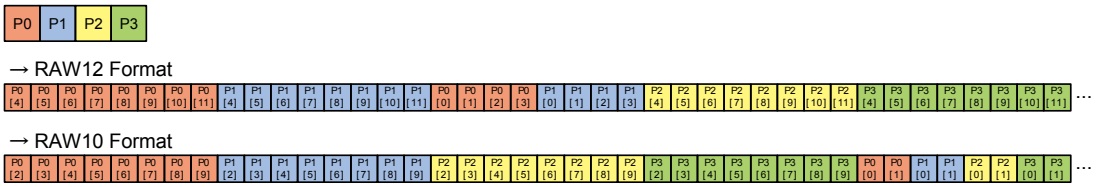
The output gradation of this sensor can be switched to 10 bits or 12 bits. However, the output gradation is fixed for some drive modes.

In parallel CMOS output mode, the output 10 bits or 12 bits are assigned to 10 pins or 12 pins, respectively. When set to 10 bits, the data is output from DO11 to DO2, and the unused pins are fixed Low.

Bit Assignment for Each Output Gradation

DO pin	Output bit assignment	
	10 bit	12 bit
DO [11]	DO [9]	DO [11]
DO [10]	DO [8]	DO [10]
DO [9]	DO [7]	DO [9]
DO [8]	DO [6]	DO [8]
DO [7]	DO [5]	DO [7]
DO [6]	DO [4]	DO [6]
DO [5]	DO [3]	DO [5]
DO [4]	DO [2]	DO [4]
DO [3]	DO [1]	DO [3]
DO [2]	DO [0]	DO [2]
DO [1]	Fixed to “0”	DO [1]
DO [0]	Fixed to “0”	DO [0]

In serial LVDS output mode, output uses the RAW10 format when the sensor gradation is 10 bits, or the RAW12 format when the sensor gradation is 12 bits.



Example of RAW12 and RAW10 Format Output

Output Range

Output method	Output gradation	Output range	
		Minimum value	Maximum value
Parallel CMOS output	10 bit	000h	3FEh
	12 bit	000h	FFEh
Serial LVDS output	10 bit	004h	3FFh
	12 bit	010h	FFFh

The range of the minimum and maximum values of the output data differs in parallel CMOS output mode and serial LVDS output mode. In parallel CMOS output mode, the output pins do not go to “All 1” except for the sync code. In serial LVDS output mode, the sensor signal may go to “All 1”, but not to “All 0”.

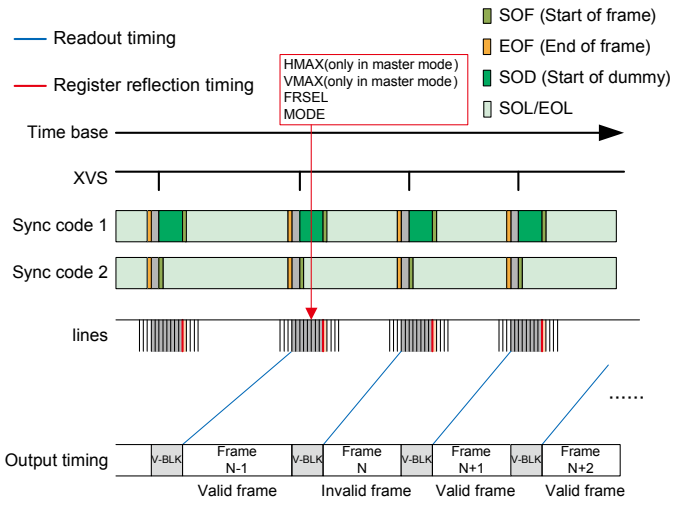
Mode Transitions

When changing the drive mode during sensor drive operation, first set the sensor to all-pixel scan mode, and then set it again to the desired drive mode. The table below shows the number of invalid frames generated by transition between the various modes.
Data is output from sensor during the invalid frame period, but the output values may not reflect the integration time or may not be uniform on the screen, or a partially saturated image may be output.

Number of Invalid Frames Generated during Mode Transitions

Mode transition			Number of invalid frames
All-pixel scan mode	⇒	Window cropping mode	1
All-pixel scan mode	⇒	2 × 2 binning mode	
All-pixel scan mode	⇒	Vertical 1/2 subsampling mode	
All-pixel scan mode	⇒	All-pixel scan mode, vertical value inversion	
Window cropping mode	⇒	All-pixel scan mode	
2 × 2 binning mode	⇒	All-pixel scan mode	
Vertical 1/2 subsampling mode	⇒	All-pixel scan mode	
All-pixel scan mode, vertical value inversion	⇒	All-pixel scan mode	

Note) When transitioning from window cropping mode to all-pixel scan mode, return the cropping range setting registers WINWH and WINWV to the initial values (7C0h, 4C9h).



*When changing the drive mode also changes the frame period, the number of invalid frames is counted according to the frame period after the change.

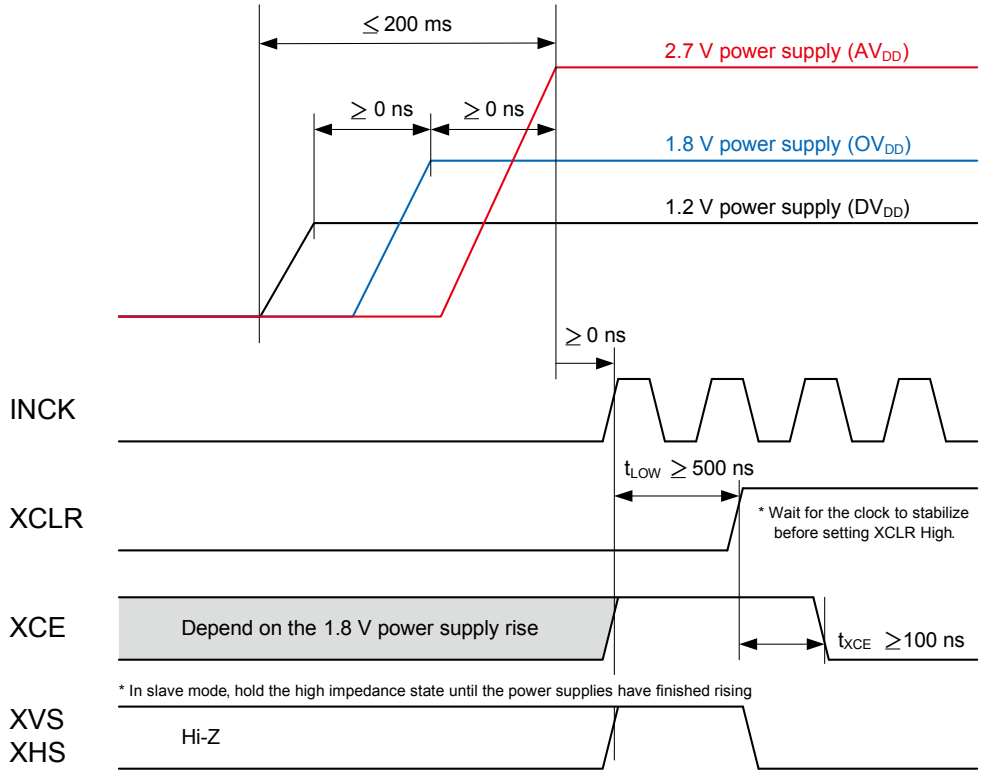
Invalid Frame Generation Timing

Power-on/off Sequence

Power-on Sequence

Follow the sequence below to turn on the power supplies.

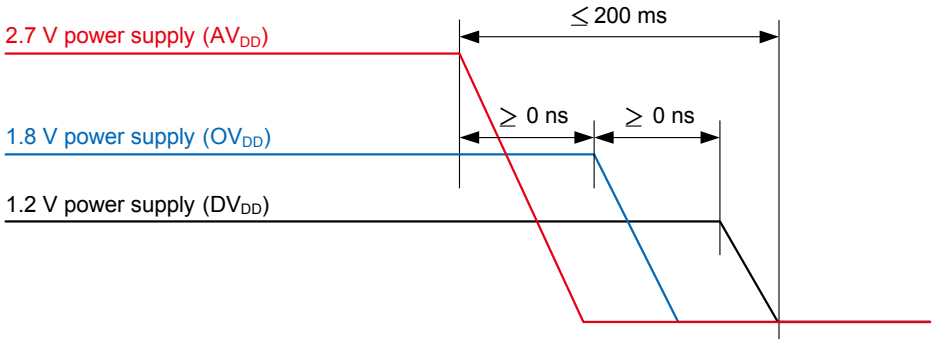
1. Turn on the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) → 1.8 V power supply (OV_{DD}) → 2.7 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
2. Start master clock (INCK) input after turning on the power supplies.
3. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.)
   In addition, hold XCE at High level during this period. The XCE rise timing differs according to the 1.8 V power supply (OV_{DD}), so hold XCE at High level until INCK is input.
   The system clear is applied by setting XCLR to High level. However, the master clock needs to stabilize before setting the XCLR pin to High level.
4. Make the sensor settings by register communication after the system clear. A period of 100 ns or more should be provided after setting XCLR High before inputting the communication enable signal XCE.



Power-on Sequence

Power-off Sequence

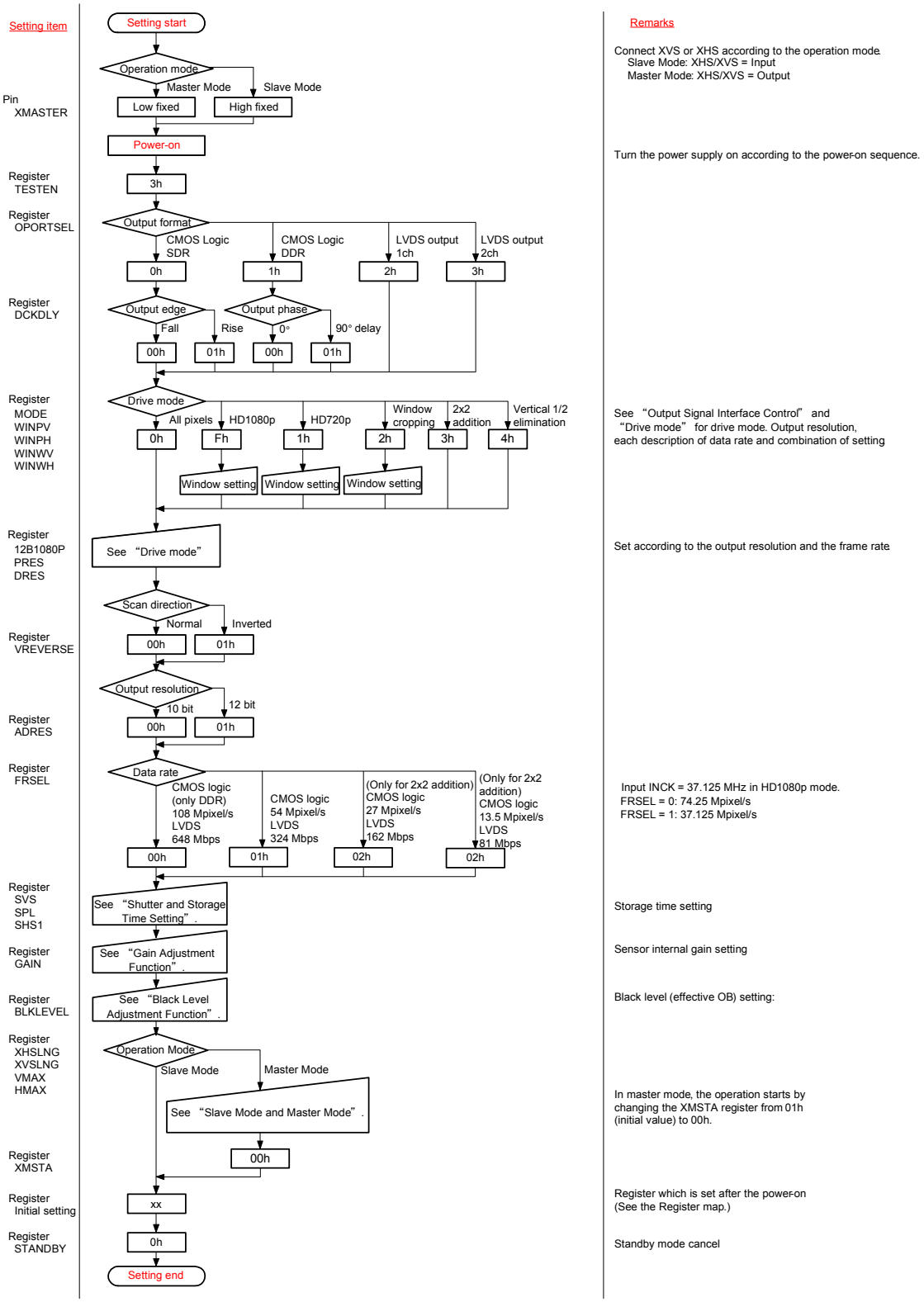
Turn Off the power supplies so that the power supplies fall in order of 2.7 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should finish falling within 200 ms. Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, XVS, XHS) to 0 V or high impedance before the 1.8 V power supply (OV_{DD}) falls.



Power-off Sequence

Sensor Setting Flow Chart

The initial setting flow chart of sensor is shown below. The initial setting should be made after the sensor reset immediately after the power-on.
See the items of the operation description shown in “Remarks” for control method.

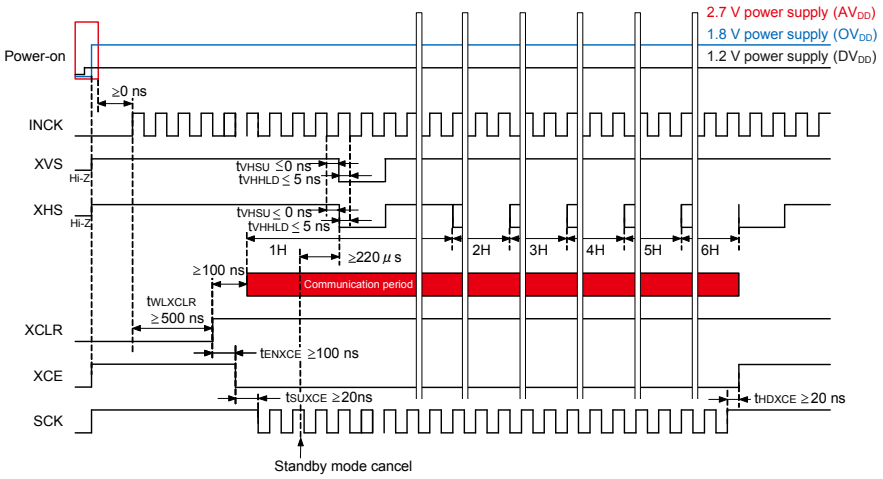


Serial Communication Period after Sensor Reset

Slave mode

The communication period is set at the timing shown below for the sensor initial settings immediately after power-on. In slave mode, the vertical and horizontal sync signals (XVS, XHS) become valid only from the falling edges 100 ns or more after sensor reset (after XCLR is set Low). The 6H serial communication period is from the falling edge of the first valid XVS to the sixth XHS falling edge thereafter.

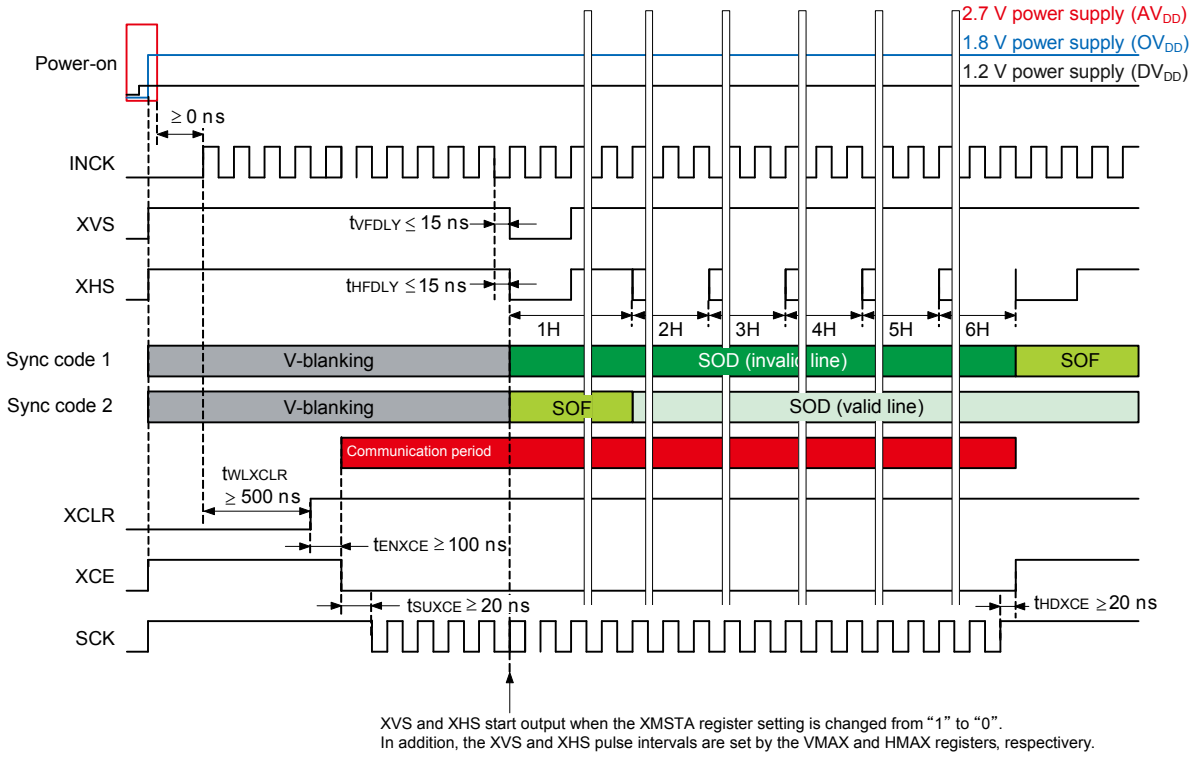
Note) XVS and XHS signals input when XCLR is Low are ignored. At this time the sensor is in standby mode until the next XVS signal. Register communication is possible in standby mode.



Communication Period after Sensor Reset in Slave Mode

Master mode

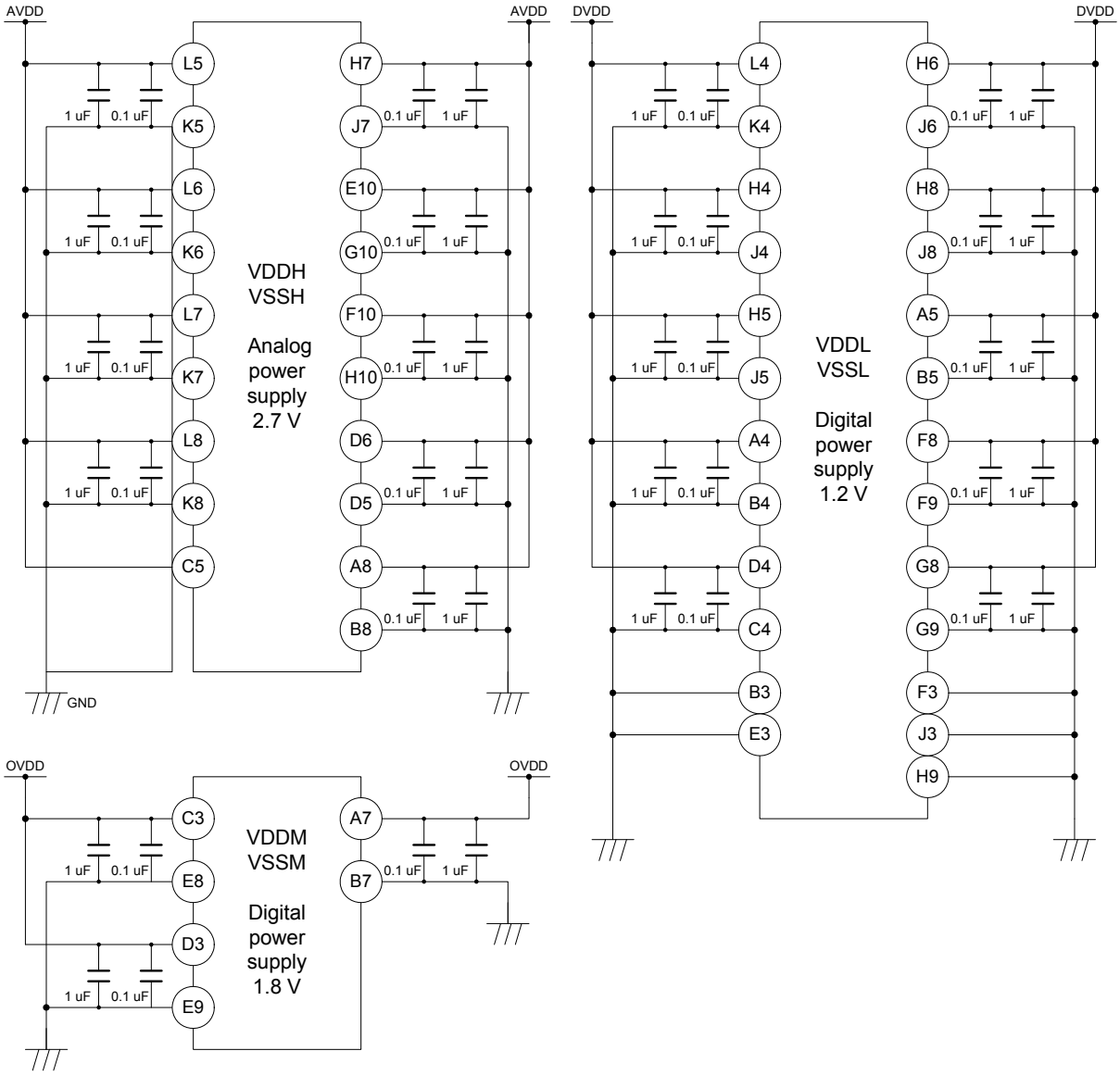
In master mode, the HMAX register (address 03h [7:0], 04h [5:0]) initial value is “44Ch” and the VMAX register (address 05h [7:4], 06h [7:0]) initial value is “4E2h”, so both XVS and XHS are output at these initial setting V and H widths until the setting values are reflected 6H later. When the VMAX and HMAX registers are set to arbitrary values by serial communication at the initial setting, and the master mode start register XMSTA (address 26h [0]) setting is changed from “1” to “0”, XVS and XHS start output according to the set values from the 7th H after the register settings are reflected. However, when VMAX and HMAX are set during the standby period, XVS and XHS are output according to the set values after standby is canceled.



Communication Period after Sensor Reset in Master Mode

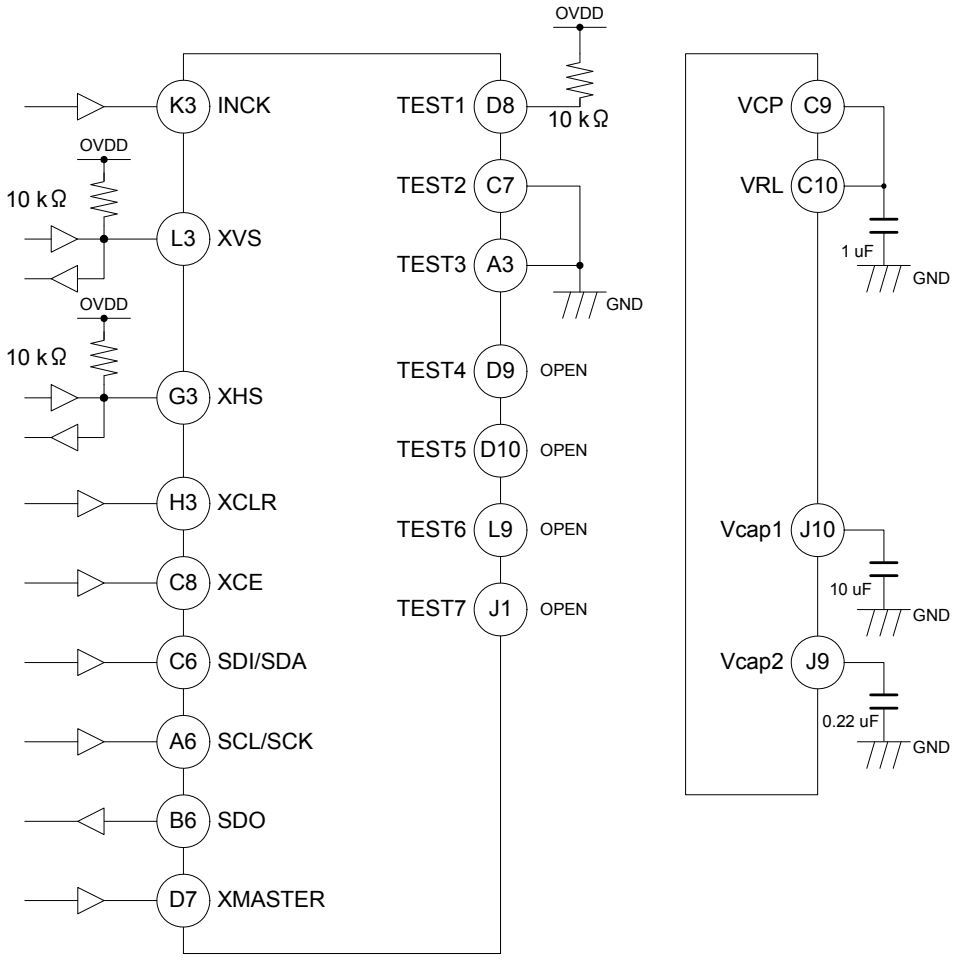
Peripheral Circuit

Power pins



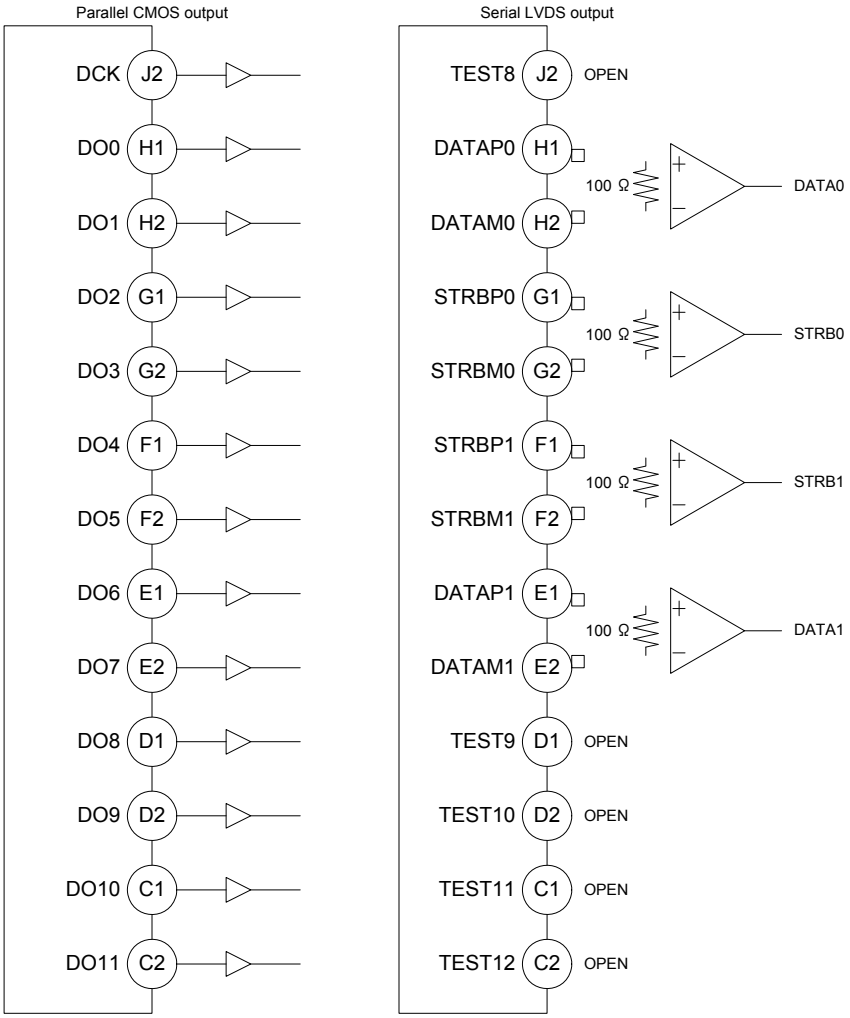
Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Signal pins



Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Data out pins



Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same

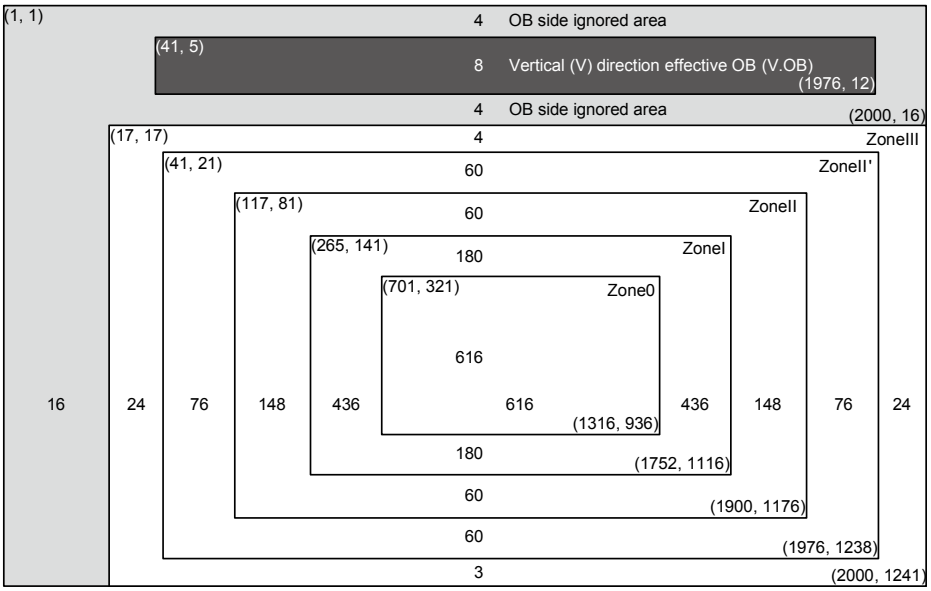
Spot Pixel Specifications

(VA_{DD} = 2.7 V, OV_{DD} = 1.8 V, DV_{DD} = 1.2 V, Ta = 60 °C, 30 frame/s, Gain: 0 dB)

Type of distortion	Level	Maximum distorted pixels in each zone				Measurement method	Remarks
		0 to II'	Effective OB	III	Ineffective OB		
Black or white pixels at high light	30 % ≤ D	17	No evaluation criteria applied			1	
White pixels in the dark	5.6 mV ≤ D	200		No evaluation criteria applied		2	Ta = 60 °C 1/30 s integration
Black pixels at signal saturated	D ≤ 649 mV	0	No evaluation criteria applied			3	

Note) 1. Zone is specified based on all-pixel drive mode.
2. D...Spot pixel level.
3. See the Spot Pixel Pattern Specifications for the specifications in which white pixel and black pixel are close.

Zone Definition



Notice on White Pixels Specifications

After delivery inspection of CMOS image sensors, cosmic radiation may distort pixels of CMOS image sensors, and then distorted pixels may cause white point effects in dark signals in picture images. (Such white point effects shall be hereinafter referred to as "White Pixels".) Unfortunately, it is not possible with current scientific technology for CMOS image sensors to prevent such White Pixels. It is recommended that when you use CMOS image sensors, you should consider taking measures against such White Pixels, such as adoption of automatic compensation systems for White Pixels in dark signals and establishment of quality assurance standards.
Unless the Seller's liability for White Pixels is otherwise set forth in an agreement between you and the Seller, Sony Corporation or its distributors (hereinafter collectively referred to as the "Seller") will, at the Seller's expense, replace such CMOS image sensors, in the event the CMOS image sensors delivered by the Seller are found to be to the Seller's satisfaction, to have over the allowable range of White Pixels as set forth as set forth above under the heading "Spot Pixels Specifications", within the period of three months after the delivery date of such CMOS image sensors from the Seller to you; provided that the Seller disclaims and will not assume any liability after if you have incorporated such CMOS image sensors into other products.
Please be aware that Seller disclaims and will not assume any liability for (1) CMOS image sensors fabricated, altered or modified after delivery to you, (2) CMOS image sensors incorporated into other products, (3) CMOS image sensors shipped to a third party in any form whatsoever, or (4) CMOS image sensors delivered to you over three months ago. Except the above mentioned replacement by Seller, neither Sony Corporation nor its distributors will assume any liability for White Pixels. Please resolve any problem or trouble arising from or in connection with White Pixels at your costs and expenses.

[For Your Reference] The Annual Number of White Pixels Occurrence

The chart below shows the predictable data on the annual number of white pixels occurrence in a single-story building in Tokyo at an altitude of 0 meters. It is recommended that you should consider taking measures against the annual White Pixels, such as adoption of automatic compensation systems appropriate for each annual number of White Pixels occurrence.
The data in the chart is based on records of past field tests, and signifies estimated number of White Pixels calculated according to structures and electrical properties of each device. Moreover, the data in the chart is for your reference purpose only, and is not to be used as part of any CMOS image sensor specifications.

Example of Annual Number of Occurrence

White Pixel Level (in case of integration time = 1/30 s) (Ta = 60 °C)	Annual number of occurrence
5.6 mV or higher	2.4 p.c.s
10.0 mV or higher	1.6 p.c.s
24.0 mV or higher	0.8 p.c.s
50.0 mV or higher	0.5 p.c.s
72.0 mV or higher	0.4 p.c.s

Note 1) The above data indicates the number of White Pixels occurrence when a CMOS image sensor is left for a year.

Note 2) The annual number of White Pixels occurrence fluctuates depending on the CMOS image sensor storage environment (such as altitude, geomagnetic latitude and building structure), time (solar activity effects) and so on. Moreover, there may be statistic errors. Please take notice and understand that this is an example of test data with experiments that have being conducted over a specific time period and in a specific environment.

Note 3) This data does not guarantee the upper limits of the number of White Pixels occurrence.

For Your Reference:

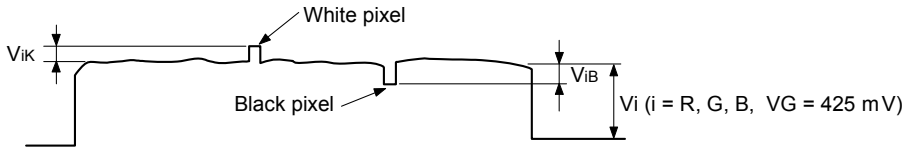
The annual number of White Pixels occurrence at an altitude of 3,000 meters is from 5 to 10 times more than that at an altitude of 0 meters because of the density of the cosmic rays. In addition, in high latitude geographical areas such as London and New York, the density of cosmic rays increases due to a difference in the geomagnetic density, so the annual number of White Pixels occurrence in such areas approximately doubles when compared with that in Tokyo.

Measurement Method for Spot Pixels

After setting the measurement condition to the standard imaging condition II, and the device drive conditions are within the bias and clock voltage conditions. Configure the drive circuit according to the example and measure.

1. Black or white pixels at high light
   After adjusting the average value of the Gr/Gb signal output to 425 mV, measure the local dip point (black pixel at high light, ViB) and the peak point (white pixel at high light, ViK) in the Gr/Gb/R/B signal output Vi (i = Gr/Gb/R/B), and substitute the values into the following formula.

   Spot pixel level D = {(Vi_B or Vi_K)/Vi average value} × 100 [%]



Signal output waveform of R/G/B channel

2. White pixels in the dark
   Set the device to a dark setting and measure the local peak point of the signal output waveform using the average value of the dark signal output as a reference.

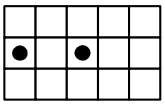
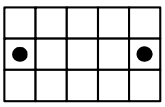
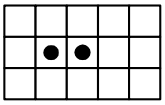
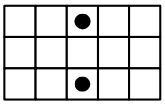
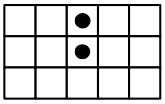
3. Black pixels at signal saturated
   Set the device to operate in saturation and measure the local dip point using the OB output as a reference.

Signal output waveform of R/G/B channel

Spot Pixel Pattern Specifications

Spot pixel patterns are counted as shown below.

List of Spot Pixel Patterns

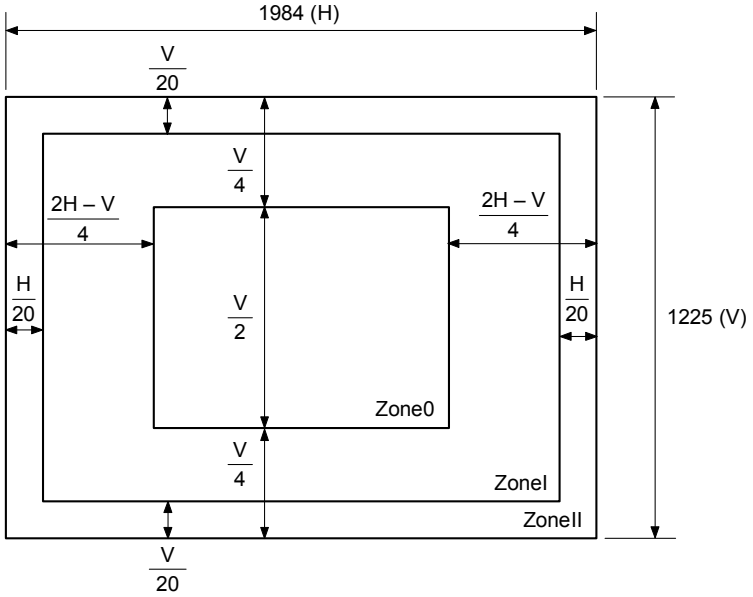
No.	Pattern	White pixel	Black pixel	Bright spot
1		Rejected	Rejected	Rejected
2		Rejected	Rejected	Rejected
3		Allowed	Allowed	Allowed
4		Rejected	Allowed	Allowed
4		Allowed	Allowed	Allowed

Note) 1. ●: Black circles indicate the positions of spot pixels. The patterns are specified separately for white pixels, black pixels and bright spots.
(Example: Even when a black pixel and a white pixel are arranged as shown by pattern No. 1, this is not judged as a defect (Allowed).)
2. Sensors exhibiting one or more patterns indicated as “Rejected” are sorted and removed.
3. Sensors exhibiting patterns indicated as “Allowed” are not subject to sorting and removal, and these pixels are instead counted in the number of allowable spot pixels by zone.
4. White pixels and black pixels other than the patterns noted in the table above are all counted in the number of allowable spot pixels by zone.

Stain Specifications

Zone	Allowable pixels	Size	Level	Lens aperture
0 to II	0	L ≥ 3	R ≥ 8 %	F = 16
Means no stain over three lines or more.				

Stain Zone Definition



Stain Measurement Method

In the following measurement, set the measurement condition to the standard imaging condition II, set the lens diaphragm to F16, and adjust the luminous intensity so that the average value of the G channel signal output is 150 mV. Measure the local dip in the average value of the R/G/B channel signal output (ViBL), and then calculate the stain level (R) as the ratio of ViBL to the average value of the R/G/B channel signal output (Vi).

Stain level $R = (Vi_{BL}/Vi) \times 100$ [%] (i = R, G, B)

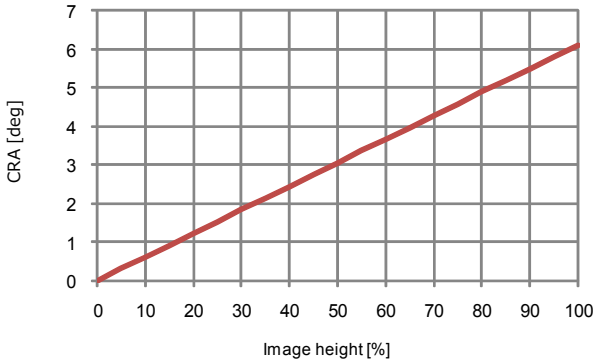
At the same time, the size (L) of the area where the stain level is 8 % or more is determined by line number conversion.
The distance from one center of a stain to another is the stain interval, and is also determined in the same way by line number conversion.

Signal output waveform of R/G/B channel

CRA Characteristics

(Exit pupil distance: -30 mm)

The recommended CRA characteristics is 0.0 degrees all over the image height (0 – 100 %), because the target E.P.D. is infinite.
We assume that the worst case of E.P.D. is -30 mm. The CRA characteristics of -30 mm E.P.D. is described below. The real CRA should be smaller than the table below.



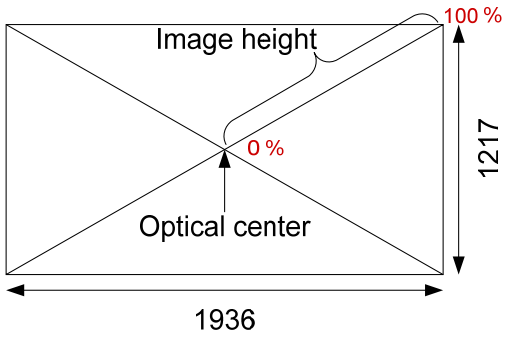
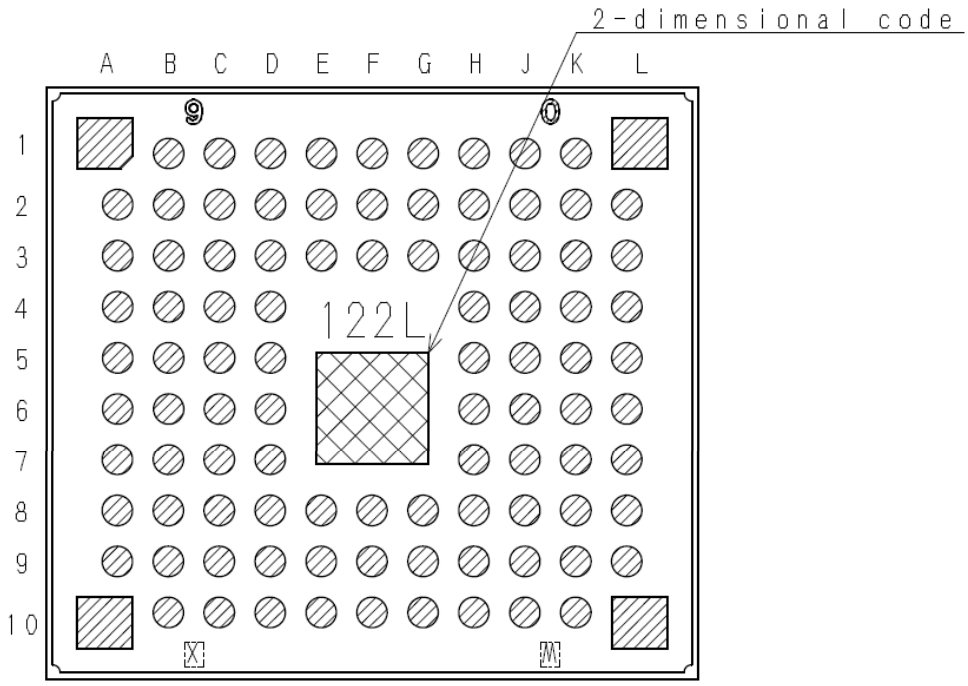


Image height		CRA
(%)	(mm)	(deg)
0	0.00	0.00
5	0.16	0.31
10	0.32	0.61
15	0.48	0.92
20	0.64	1.22
25	0.80	1.53
30	0.96	1.83
35	1.12	2.14
40	1.28	2.44
45	1.44	2.75
50	1.60	3.05
55	1.76	3.36
60	1.92	3.66
65	2.08	3.97
70	2.24	4.27
75	2.40	4.57
80	2.56	4.88
85	2.72	5.18
90	2.88	5.48
95	3.04	5.79
100	3.20	6.09

Marking



Note:Following characters enter into "W", and"X".

W:In English upper case character,One character
X:Number,single number

Notes On Handling

1. Static charge prevention

Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

(1) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.

(2) Use a wrist strap when handling directly.

(3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.

(4) Ionized air is recommended for discharge when handling image sensors.

(5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Protection from dust and dirt

Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.

(1) Perform all lens assembly and other work in a clean environment (class 1000 or less).

(2) Do not touch the glass surface with hand and make any object contact with it.
If dust or other is stuck to a glass surface, blow it off with an air blower.
(For dust stuck through static electricity, ionized air is recommended.)

(3) Clean with a cotton swab with ethyl alcohol if grease stained. Be careful not to scratch the glass.

(4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

(5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

3. Installing (attaching)

(1) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

(2) The adhesive may cause the marking on the rear surface to disappear.

(3) If metal, etc., clash or rub against the package surface, the package may chip or fragment and generate dust.

(4) Acrylate anaerobic adhesives are generally used to attach this product. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the product in place until the adhesive completely hardens. (reference)

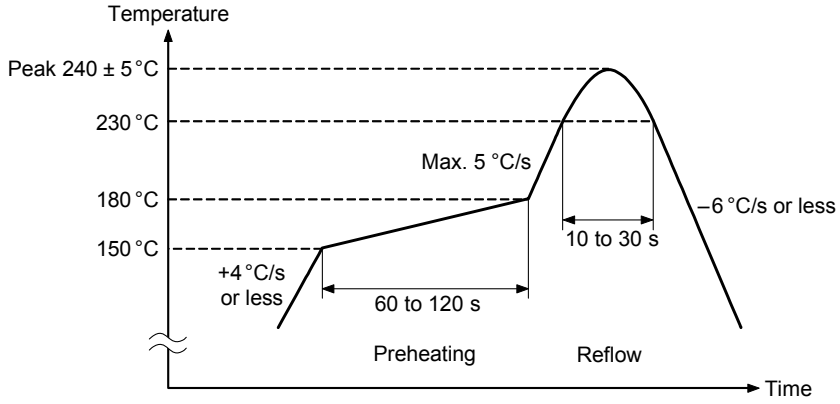
(5) Note that the sensor may be damaged when using ultraviolet ray and infrared ray on mounting it.

4. Recommended reflow soldering conditions

The following items should be observed for reflow soldering.

(1) Temperature profile for reflow soldering

Control item	Profile (at part side surface)
1. Preheating	150 to 180 °C 60 to 120 s
2. Temperature up (down)	+4 °C/s or less (–6 °C/s or less)
3. Reflow temperature	Over 230 °C 10 to 30 s Max. 5 °C/s
4. Peak temperature	Max. 240 ± 5 °C



(2) Reflow conditions

(a) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 245 °C.

(b) Perform the reflow soldering only one time.

(c) Finish reflow soldering within 72 h after unsealing the degassed packing.
Store the products under the condition of temperature of 30 °C or less and humidity of 70 % RH or less after unsealing the package.

(d) Perform re-baking only one time under the condition at 125 °C for 24 h

(3) Others

(a) Carry out evaluation for the solder joint reliability in your company.

(b) After the reflow, the paste residue of protective tape may remain around the seal glass.
(The paste residue of protective tape should be ignored except remarkable one.)

(c) Note that X-ray inspection may damage characteristics of the sensor.

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as the color filters of color devices will be discolored.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

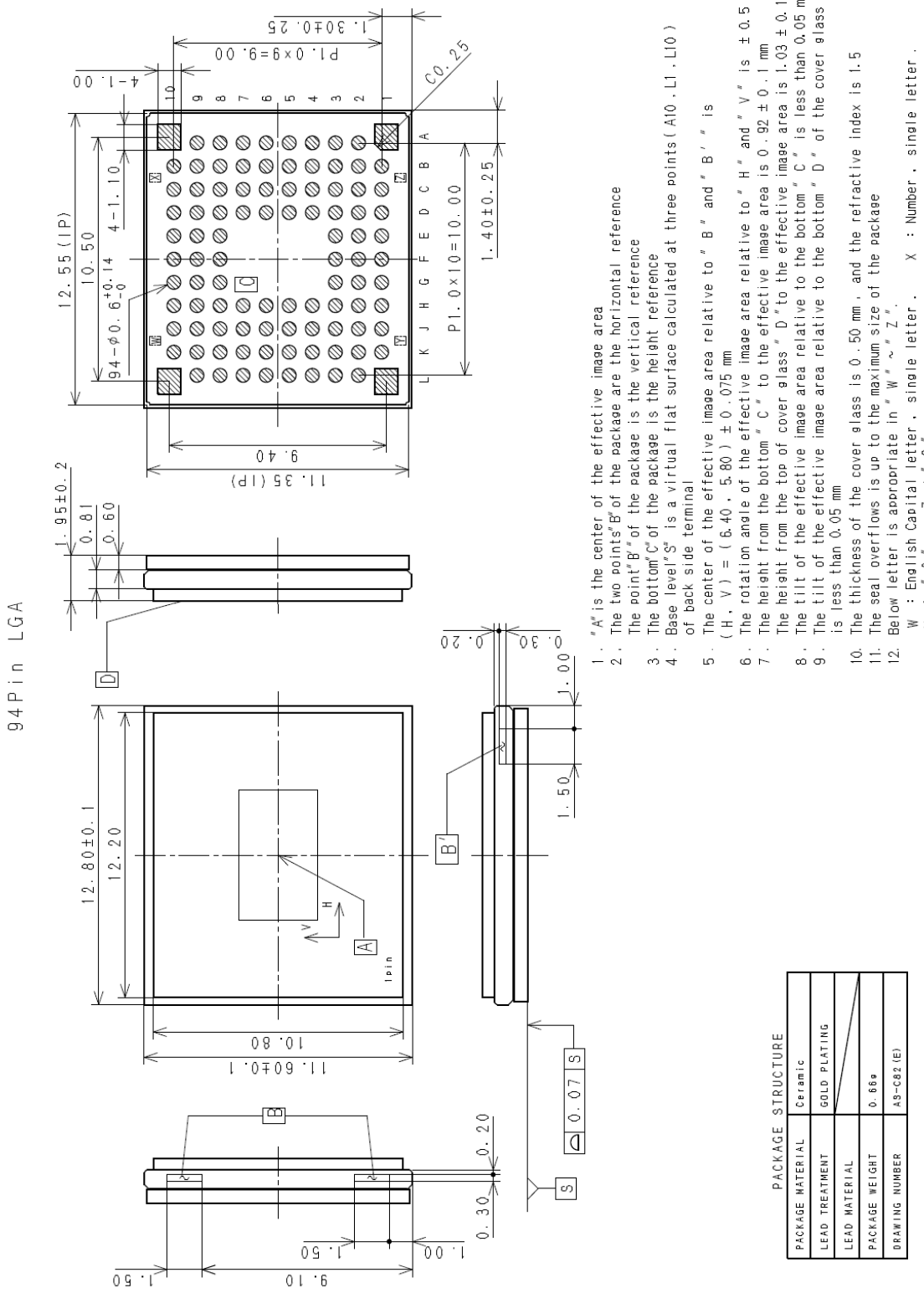
(3) This product is precision optical parts, so care should be taken not to apply excessive mechanical shocks or force.

(4) Note that imaging characteristics of the sensor may be affected when approaching strong electromagnetic wave or magnetic field during operation.

(5) Note that image may be affected by the light leaked to optical black when using an infrared cut filter that has transparency in near infrared ray area during shooting subjects with high luminance.

Package Outline

(Unit: mm)



1. "A" is the center of the effective image area
2. The two points"B" of the package are the horizontal reference
   The point"B" of the package is the vertical reference
3. The bottom"C" of the package is the height reference
4. Base level"S" is a virtual flat surface calculated at three points(A10,L1,L10)
   of back side terminal
5. The center of the effective image area relative to " B " and " B ' " is
   (H, V) = (6.40, 5.80) ± 0.075 mm
6. The rotation angle of the effective image area relative to " H " and " V " is ± 0.5°
7. The height from the bottom " C " to the effective image area is 0.92 ± 0.1 mm
   The height from the top of cover glass " D "to the effective image area is 1.03 ± 0.1 mm
8. The tilt of the effective image area relative to the bottom " C " is less than 0.05 mm
9. The tilt of the effective image area relative to the bottom " D " of the cover glass
   is less than 0.05 mm
10. The thickness of the cover glass is 0.50 mm, and the refractive index is 1.5
11. The seal overflows is up to the maximum size of the package
12. Below letter is appropriate in " W " ~ " Z ".
    W : English Capital letter, single letter. X : Number, single letter.
    Y : " 0 ". Z : " 6 ".

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	
PACKAGE WEIGHT	0.66g
DRAWING NUMBER	AS-C82(E)

Note

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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.