CLC001 Evaluation Board User Guide

SD001EVK

Rev 1.1

Interface Products

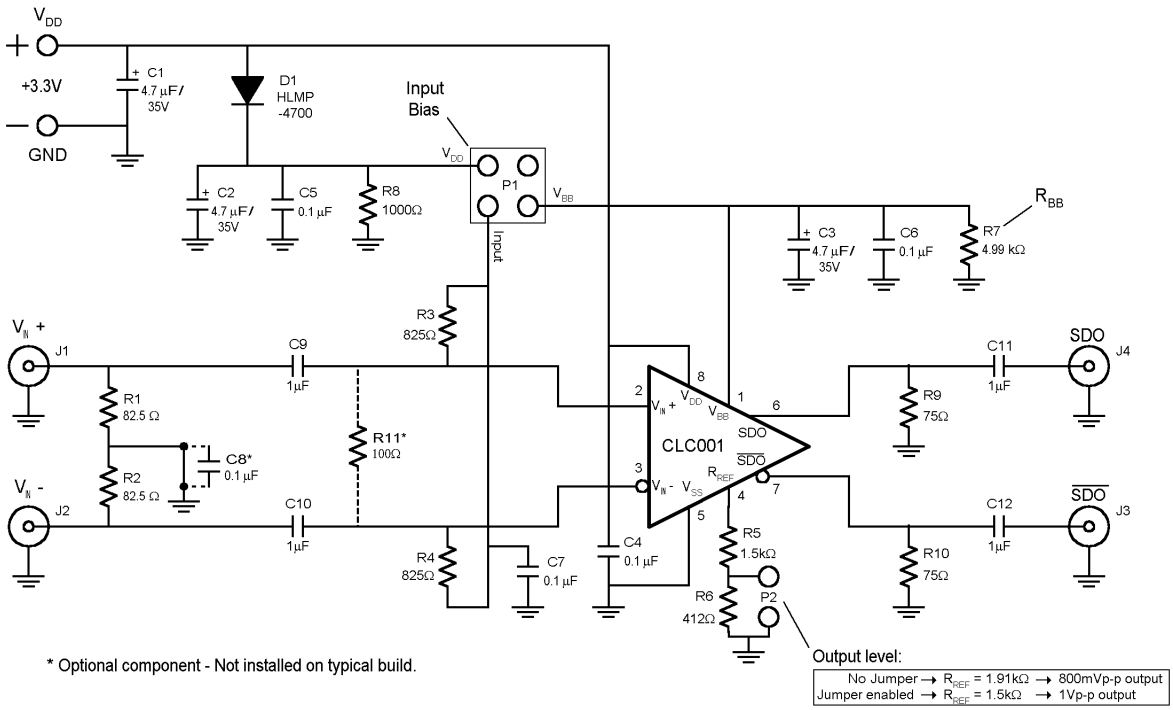

Figure 1. CLC001 Evaluation Board Schematic

Power Connection

The CLC001 evaluation board is powered by externally supplying 3.3V ±10% (4V Max) to VDD with respect to GND.

Input Interfacing

The CLC001 evaluation board schematic is shown above in Figure 1. The board is initially set up for 75Ω, AC-coupled, single-ended input. It may be configured for DC-coupled LVDS or twisted pair cable by removing R1 and R2, shorting across C9 and C10, and inserting the correct termination resistor for R11 (typically between 100 and 120Ω). No jumper should be used on P1 for DC-coupled applications. A center tap capacitance termination may be implemented by removing the short on C8 and inserting a 0.1uF capacitor.

DC Bias is applied to the inputs with the proper placement of jumpers on P1. With no jumpers installed, no bias voltage is supplied and the part must be DC-coupled. The CLC001 Evaluation Board allows for two methods of applying DC bias to the input:

1. VBB
The CLC001 provides a bias voltage through its VBB pin. Place a jumper on P1 connecting the pins labeled “Vbb” and “Input” to bias the inputs in this manner. RBB (R7) set at 4.99 kΩ should provide around 1.25V at 800 mV_{p-p} output, and 1.5V at 1.0 V_{p-p} output.

2. VDD
The CLC001 may be biased with the VDD supply by placing a jumper connecting the pins labeled “Vdd” and “Input”. This will bias the inputs at 1.5-1.7V, or roughly half of the VDD voltage.

Please refer to the datasheet for more details on input interfacing.

Adjusting the Output Level

Output level is determined by the value of $R_{REF,}$ which is set by P2. R_{REF} is 1.91 kΩ with no jumper in place, which sets the output at 800 mV_{p-p}. With the jumper enabled at P2, R_{REF} becomes 1.5 kΩ and the output is 1.0 V_{p-p}. The output level may be set to various values up to 1.0 V_{p-p} by replacing R5 and/or R6 to get the desired value of R_{REF}. Refer to Figure 10 of the datasheet for the output level’s sensitivity to R_{REF}. A typical output waveform at 622 Mbps and 1.0 V_{p-p} output level is shown in Figure 2 below.

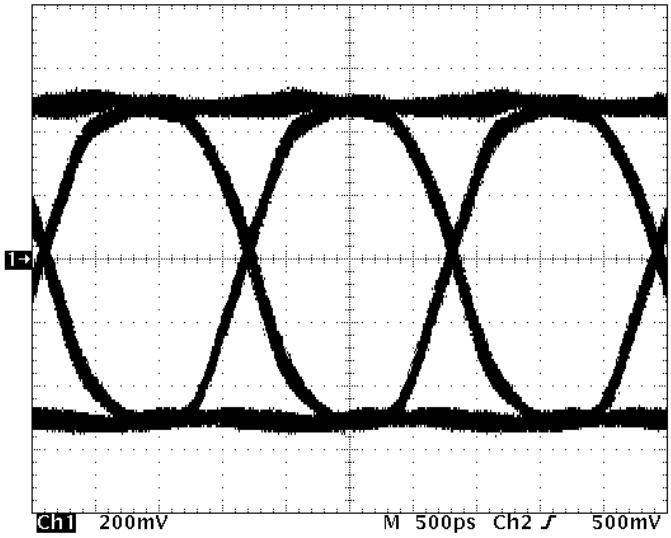

Figure 2. Typical Waveform at 622 Mbps and 1.0 V_{p-p} Output Level

BOM (Bill of Materials)

Qty	Ref. Des.	Part No.	Mfr.	Description
1	U1	CLC001AJE	NSC	IC, Ampl.
3	C1, C2, C3	ECS-T1CY475R	Pana.	4.7uF/16V SM Tant.
4	C4, C5, C6, C7	06032R104K7B20D	Philips	0.1uF/16V X7R SM0603
1	C8 (optional)	ECJ-1VB0J105K	Pana.	1uF/6.3V X7R SM0603
4	C9, C10, C11, C12	ECJ-1VB0J105K	Pana.	1uF/6.3V X7R SM0603
2	R1, R2	ERJ-3EKF82R5	Pana.	82.5/1% SM0603
2	R3, R4	ERJ-3EKF8250	Pana.	825/1% SM0603
1	R5	ERJ-3EKF1501	Pana.	1.5K/1% SM0603
1	R6	ERJ-3EKF4120	Pana.	412/1% SM0603
1	R7	ERJ-3EKF4991	Pana.	4.99K/1% SM0603
1	R8	ERJ-3EKF1001	Pana.	1K/1% SM0603
2	R9, R10	ERJ-3EKF75R0	Pana.	75/1% SM0603
1	R11 (optional)	ERJ-3EKF1000	Pana.	100/1% SM0603
1	D1	HLMP-4700	H-P	LED, Red, GP
4	J1, J2, J3, J4	560-471-00	A/D Elect.	75-Ohm R/A BNC
1	P1	TSW-102-07-T-D	Samtec	2x2 Pin header
1	P2	TSW-101-07-T-D	Samtec	1x2 Pin header