NOTES:

1. PLACE NET NAMES ON ALL JUMPERS AND HEADERS.
2. PLACE ALL PARTS OTHER THAN SMP CONNECTORS ON A 0 OR 90 DEGREE ORIENTATION.
3. SERIAL DATA SHOULD BE ROUTED AS SINGLE-ENDED 50 OHM TRANSMISSION LINES ON OUTSIDE LAYERS. ROUTING DISTANCE SHOULD BE 3 INCHES OR LESS.
4. USE ROGERS MATERIAL FOR OUTSIDE LAYERS AND FR4-370 MATERIAL FOR INSIDE LAYERS.
5. SERIAL AND REFCLK NETS MUST MATCH WITHIN +/- 0.5 MILS
6. MATCH DIFFERENTIAL TRACE WIDTHS OF SERIAL AND REFCLK LINES WITH SMP/SMA PADS.
7. PLACE TI LOGO IN TOP SIDE METAL

REVISIONS		
ECR	ECR NUMBER	DATE
	-------	xx/xx/xx

SCHEMATIC SHEET INDEX:

TLK10XXX DATA SHEET REVISION: x.x.x
DATA SHEET LAST UPDATED ON: xx/xx/xx

TEXAS INSTRUMENTS

ENGINEER	J. NERGER	DATE	04/12/13
LAYOUT	DFW TEST	DATE	04/12/13
RELEASED	J. NERGER	DATE	04/12/13

SCHEMATIC TITLE: TLK10XXX EVM MOTHER BOARD

PAGE TITLE: COVER PAGE AND NOTES

SIZE	DOCUMENT NUMBER	REV	SHEET
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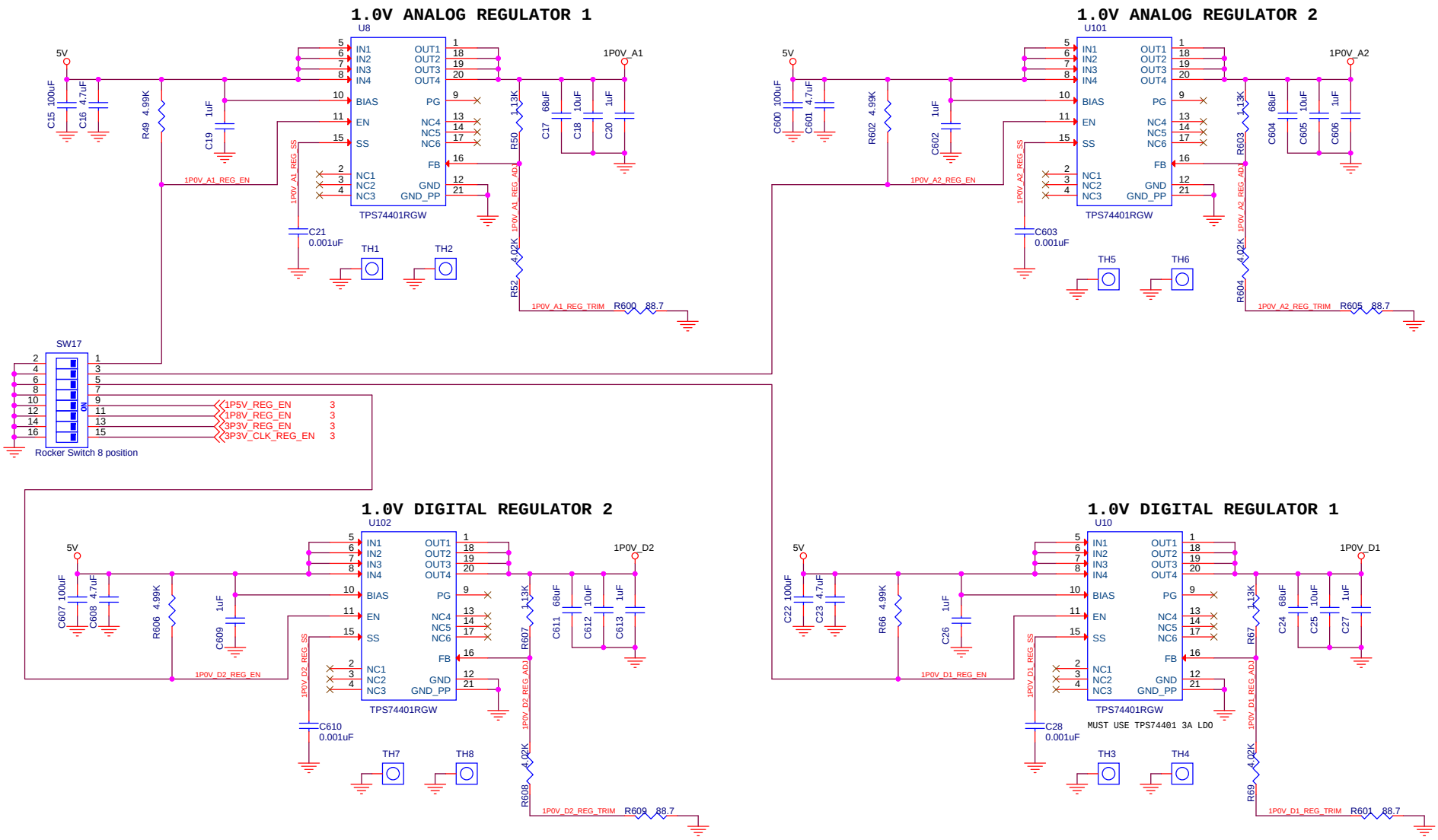

TEXAS INSTRUMENTS

PAGE TITLE			
1P0V REGULATORS			
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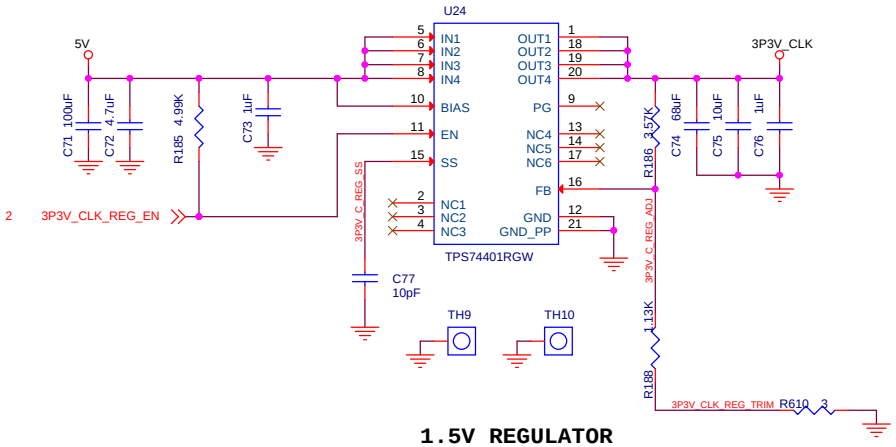
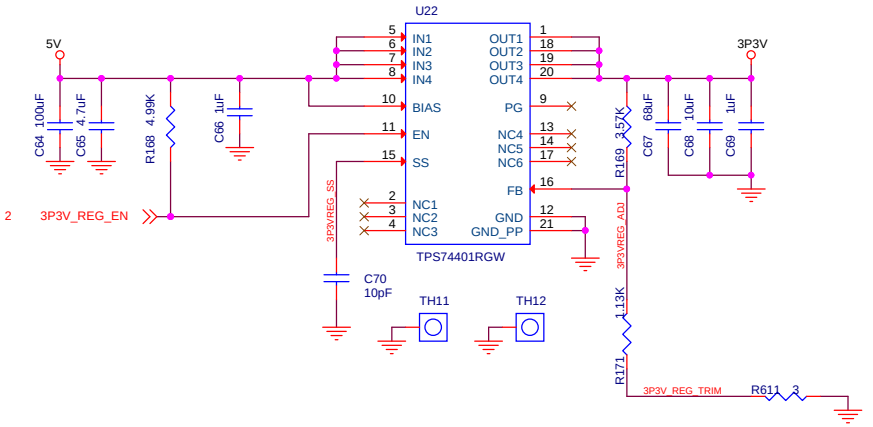
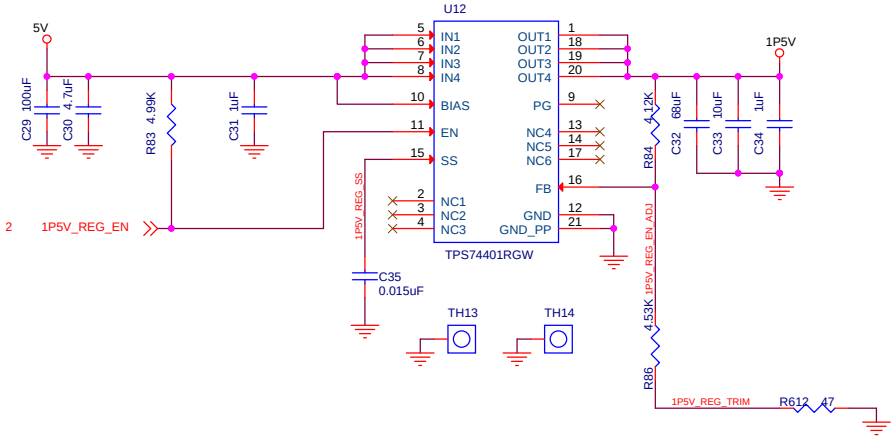
3.3V CLK REGULATOR



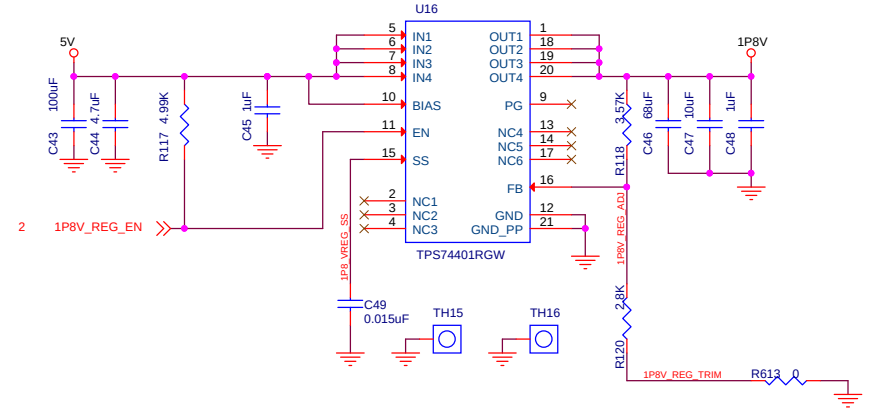
3.3V REGULATOR

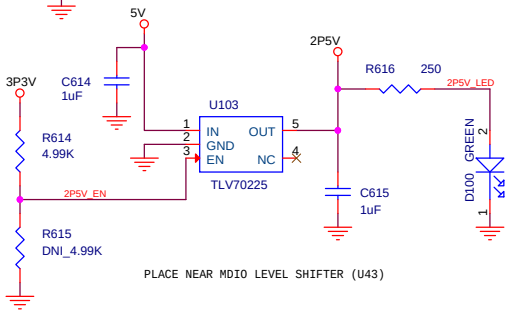


1.5V REGULATOR



1.8V REGULATOR





TEXAS INSTRUMENTS

PAGE TITLE			
1P5V, 1P8V, 2P5V, 3P3V REGULATORS			
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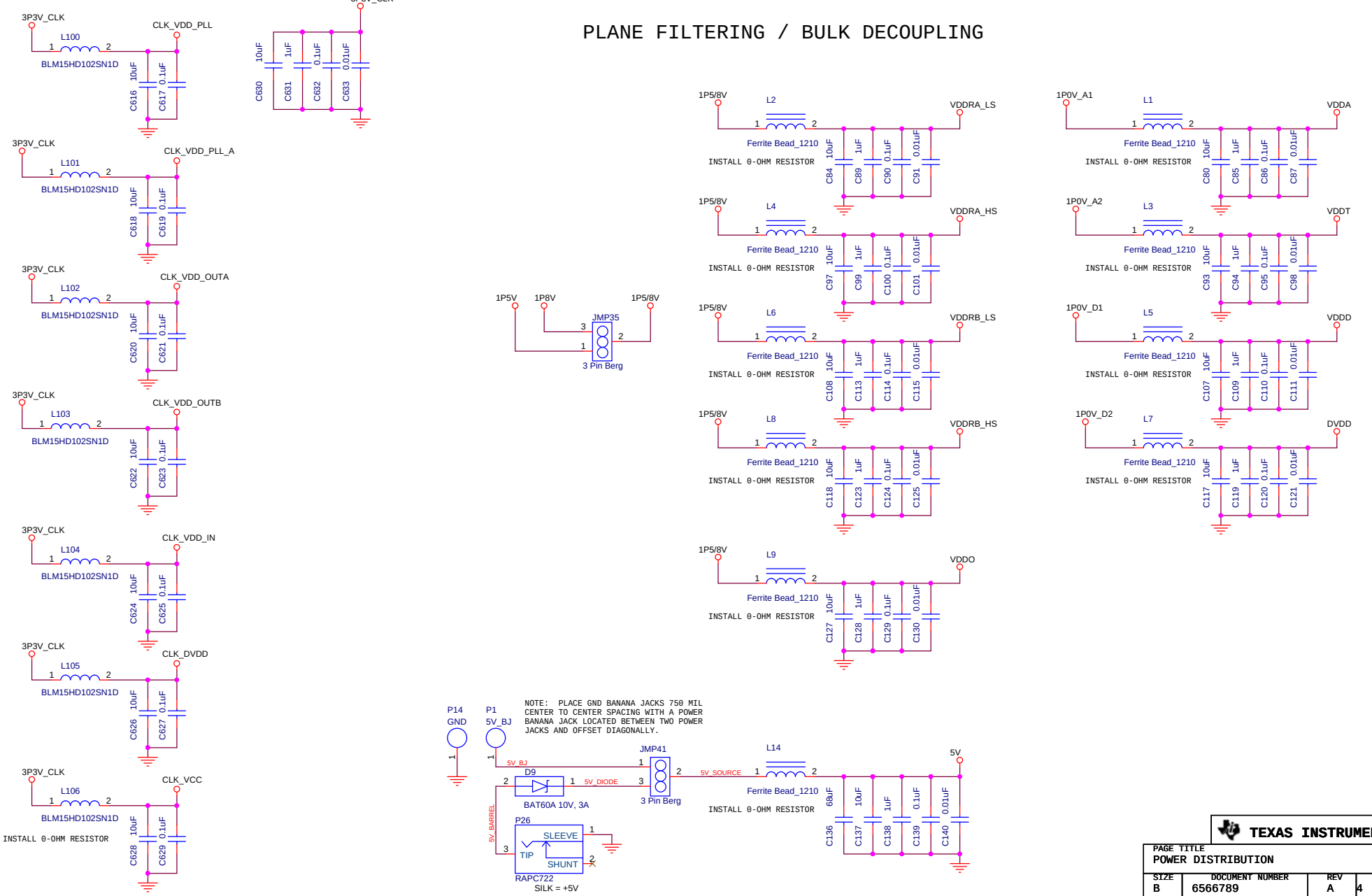
PLANE FILTERING / BULK DECOUPLING



TEXAS INSTRUMENTS

PAGE TITLE			
POWER DISTRIBUTION			
SIZE	DOCUMENT NUMBER	REV	PAGE
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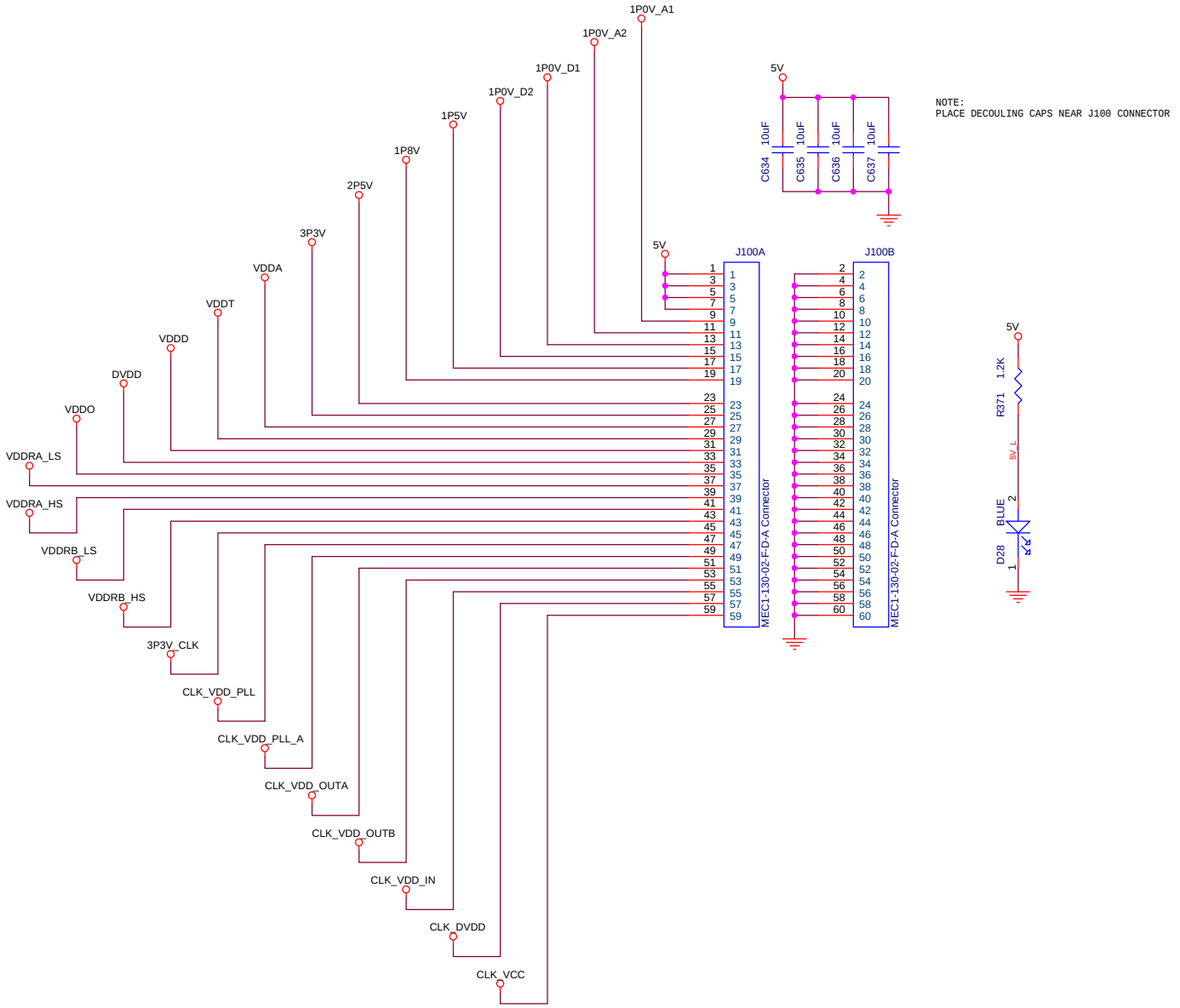
NOTE:



NOTE:
PLACE DECOULING CAPS NEAR J100 CONNECTOR

TEXAS INSTRUMENTS

PAGE TITLE			
VOLTAGE MONITORING			
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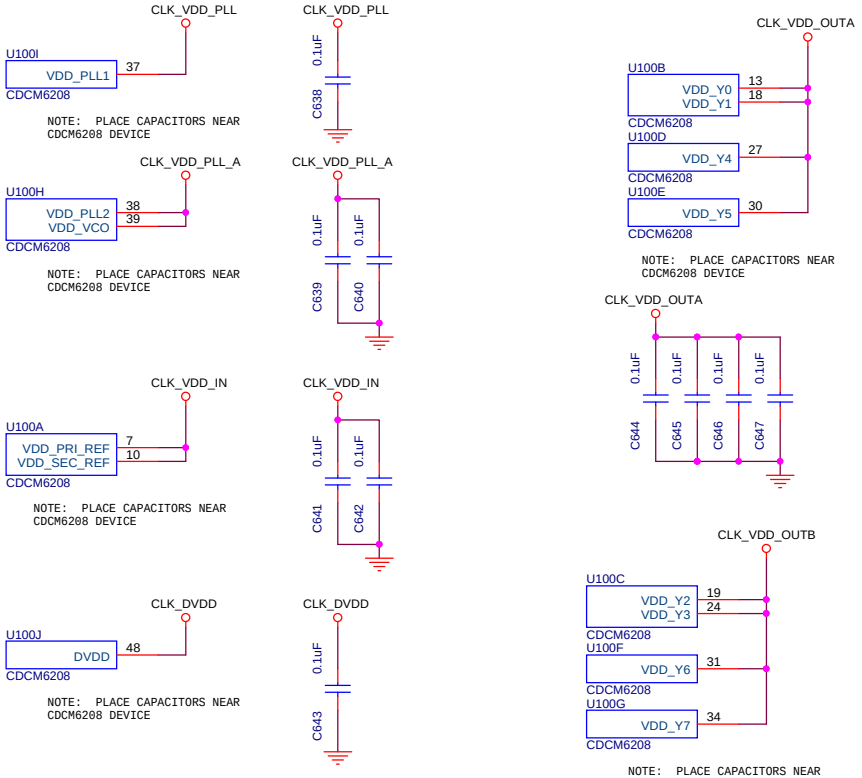
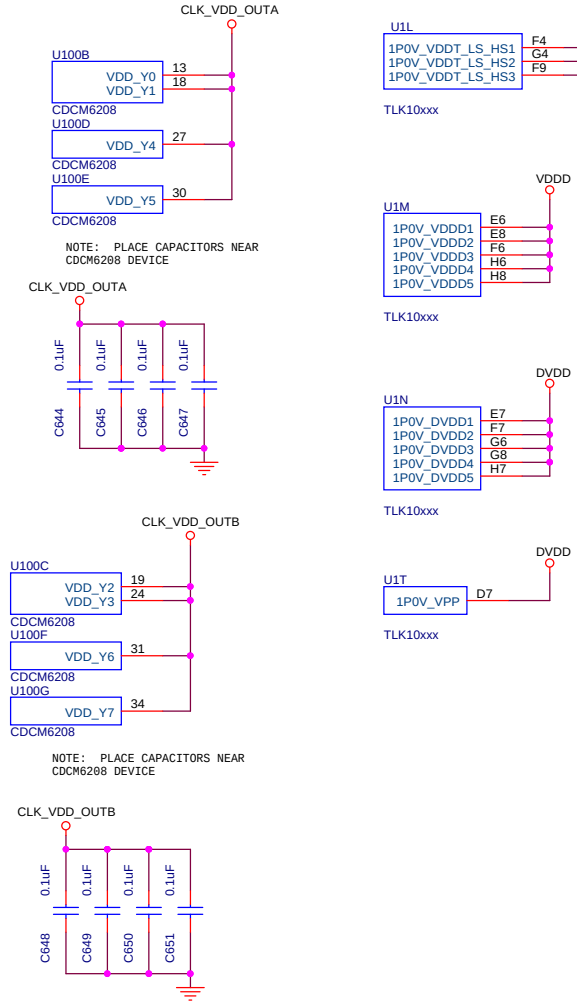
NOTES:

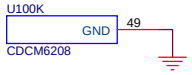
DECOUPLLING GENERAL GUIDELINES:
1. PLACE CAPACITORS SUCH THAT SMALLER VALUE CAPACITORS ARE NEARER THE DUT AND THEN SUCCESSIVELY PLACE LARGER VALUE CAPACITORS AS YOU MOVE AWAY FROM THE DUT.
2. PLACE CAPACITORS NEAR VIAS AND CONNECTORS. THESE CAPACITORS SHOULD DECOUPLE THE DRIVER SUPPLY TO THE GROUND PLANE. IF A SIGNAL IS REFERENCED TO A POWER PLANE AND THIS POWER PLANE IS NOT ASSOCIATED WITH THE DRIVER SUPPLY, THEN THIS PLANE SHOULD ALSO BE DECOUPLED TO GROUND NEAR ALL ASSOCIATED VIAS AND CONNECTORS.

CDCM6208 DEVICE POWER / LOCAL DECOUPLING

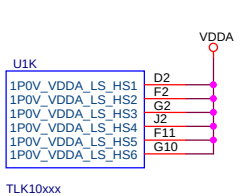


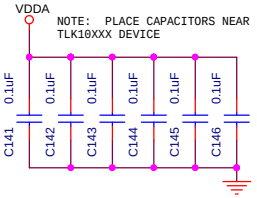


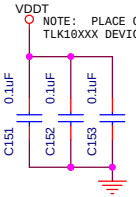
CDCM6208 DEVICE GROUND

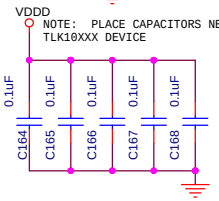


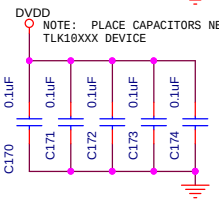
TLK10XXX DEVICE POWER / LOCAL DECOUPLING

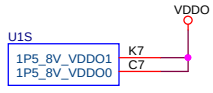


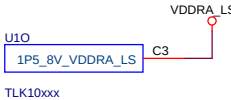


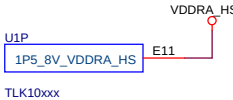


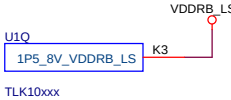


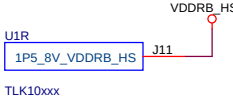


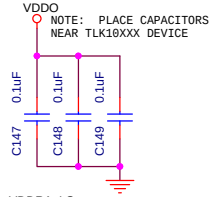


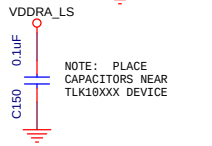


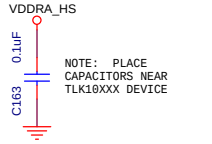


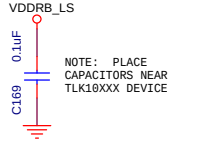


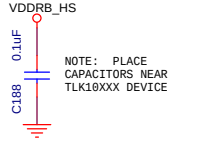




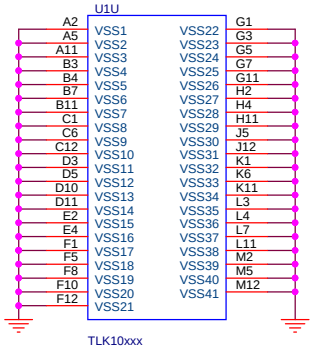








TLK10XXX DEVICE GROUND



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DEVICE POWER, GROUND, LOCAL DECOUPLING			
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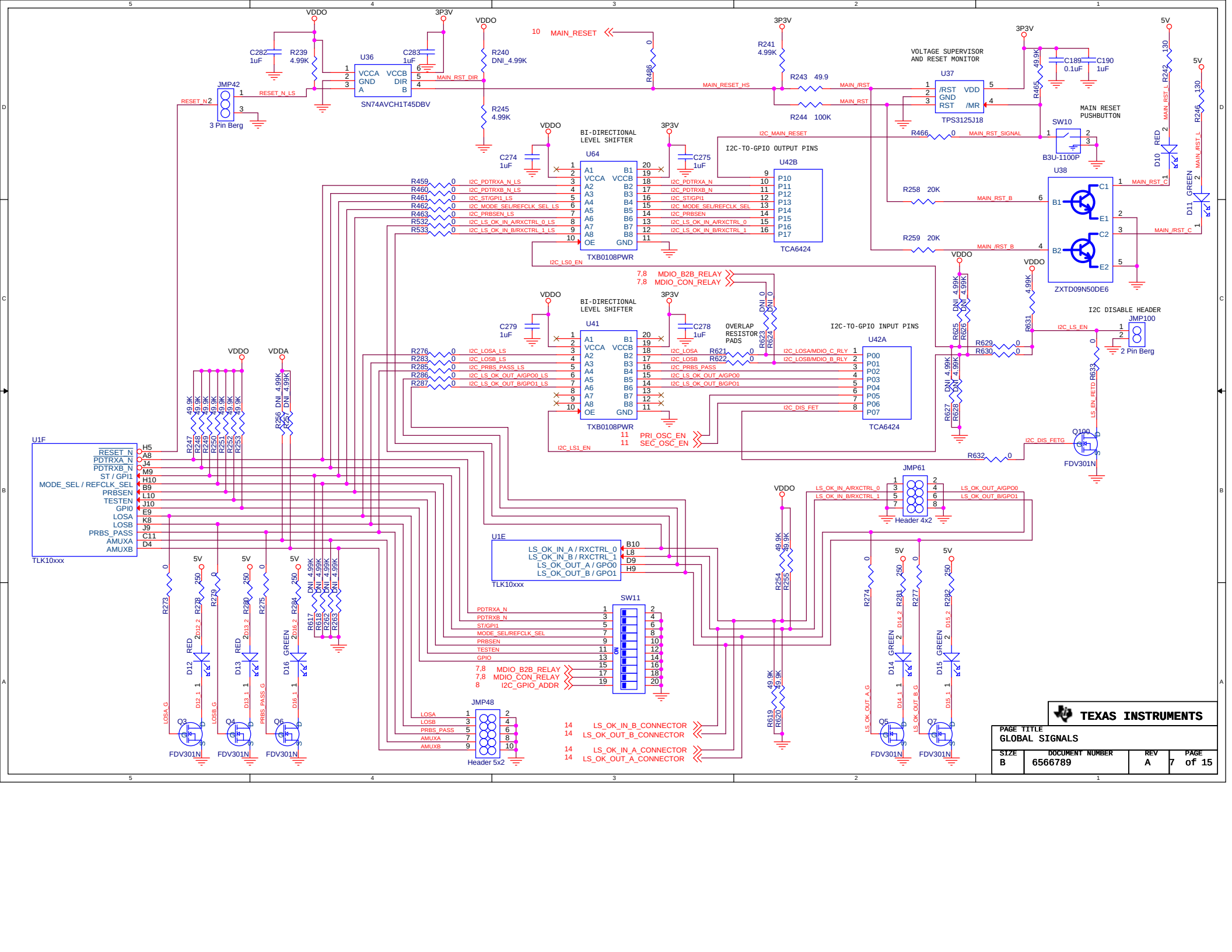
VDDO
3P3V
VDDA
5V
U36
SN74AVCH1T45DBV
JMP42
3 Pin Berg
MAIN_RESET
MAIN_RST_DIR
MAIN_RESET_HS
VOLTAGE SUPERVISOR
AND RESET MONITOR
U37
TPS3125J18
MAIN RESET
PUSHBUTTON
SW10
B3U-1100P
BI-DIRECTIONAL
LEVEL SHIFTER
U64
TXB0108PWR
I2C-TO-GPIO OUTPUT PINS
U42B
TCA6424
U38
ZXTD09N50DE6
U41
OVERLAP
RESISTOR
PADS
I2C-TO-GPIO INPUT PINS
U42A
I2C DISABLE HEADER
JMP100
2 Pin Berg
U1F
TLK10xxx
U1E
JMP61
Header 4x2
SW11
JMP48
Header 5x2
Q100
FDV301N
Q3
Q4
Q6
Q5
Q7
LS_OK_IN_A_CONNECTOR
LS_OK_OUT_A_CONNECTOR
LS_OK_IN_B_CONNECTOR
LS_OK_OUT_B_CONNECTOR
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GLOBAL SIGNALS
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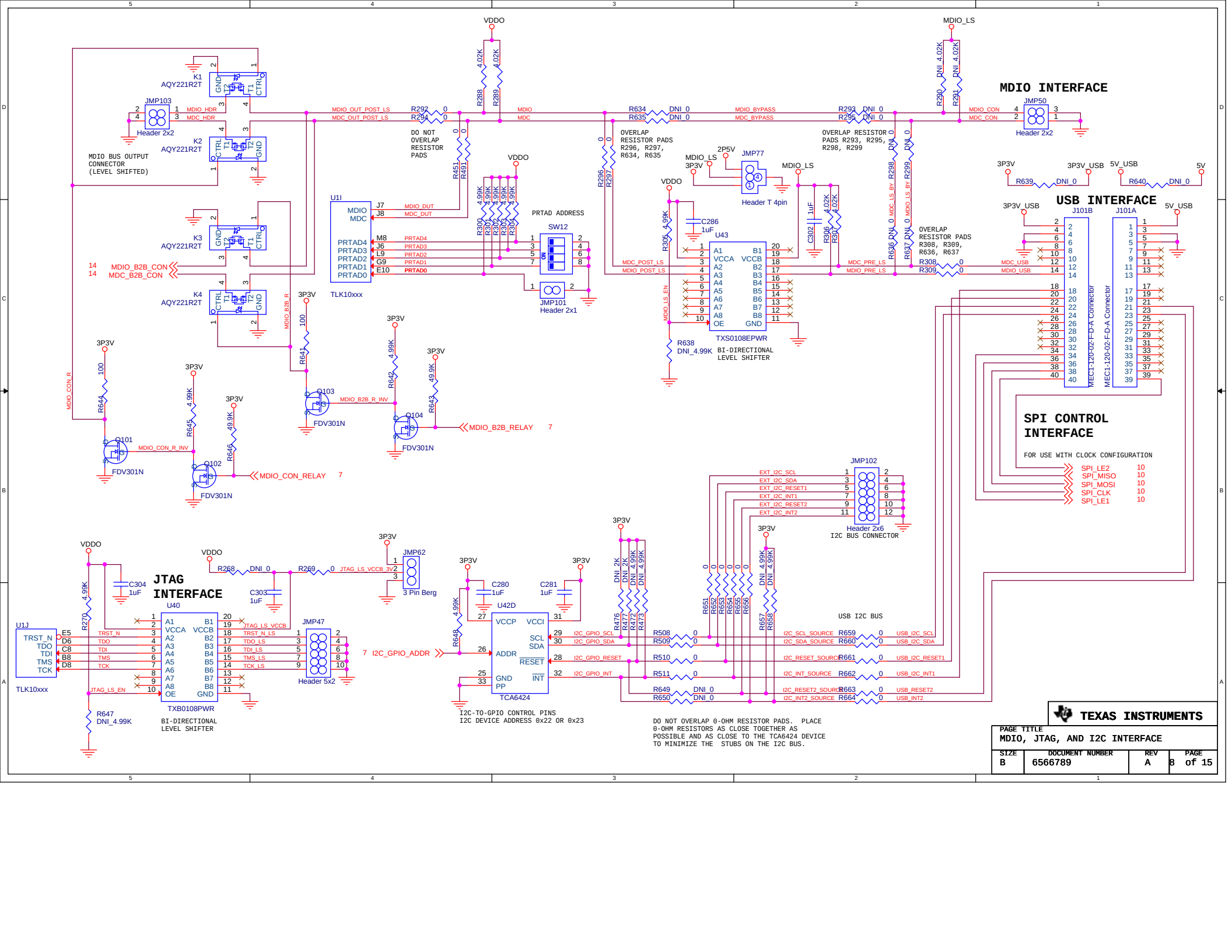
MDIO INTERFACE
USB INTERFACE
SPI CONTROL INTERFACE
FOR USE WITH CLOCK CONFIGURATION
JTAG INTERFACE
MDIO BUS OUTPUT CONNECTOR (LEVEL SHIFTED)
DO NOT OVERLAP RESISTOR PADS
OVERLAP RESISTOR PADS R296, R297, R634, R635
OVERLAP RESISTOR PADS R293, R295, R298, R299
OVERLAP RESISTOR PADS R308, R309, R636, R637
PRTAD ADDRESS
BI-DIRECTIONAL LEVEL SHIFTER
I2C BUS CONNECTOR
USB I2C BUS
I2C-TO-GPIO CONTROL PINS
I2C DEVICE ADDRESS 0x22 OR 0x23
DO NOT OVERLAP 0-OHM RESISTOR PADS. PLACE 0-OHM RESISTORS AS CLOSE TOGETHER AS POSSIBLE AND AS CLOSE TO THE TCA6424 DEVICE TO MINIMIZE THE STUBS ON THE I2C BUS.
TEXAS INSTRUMENTS
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MDIO, JTAG, AND I2C INTERFACE
SIZE B
DOCUMENT NUMBER 6566789
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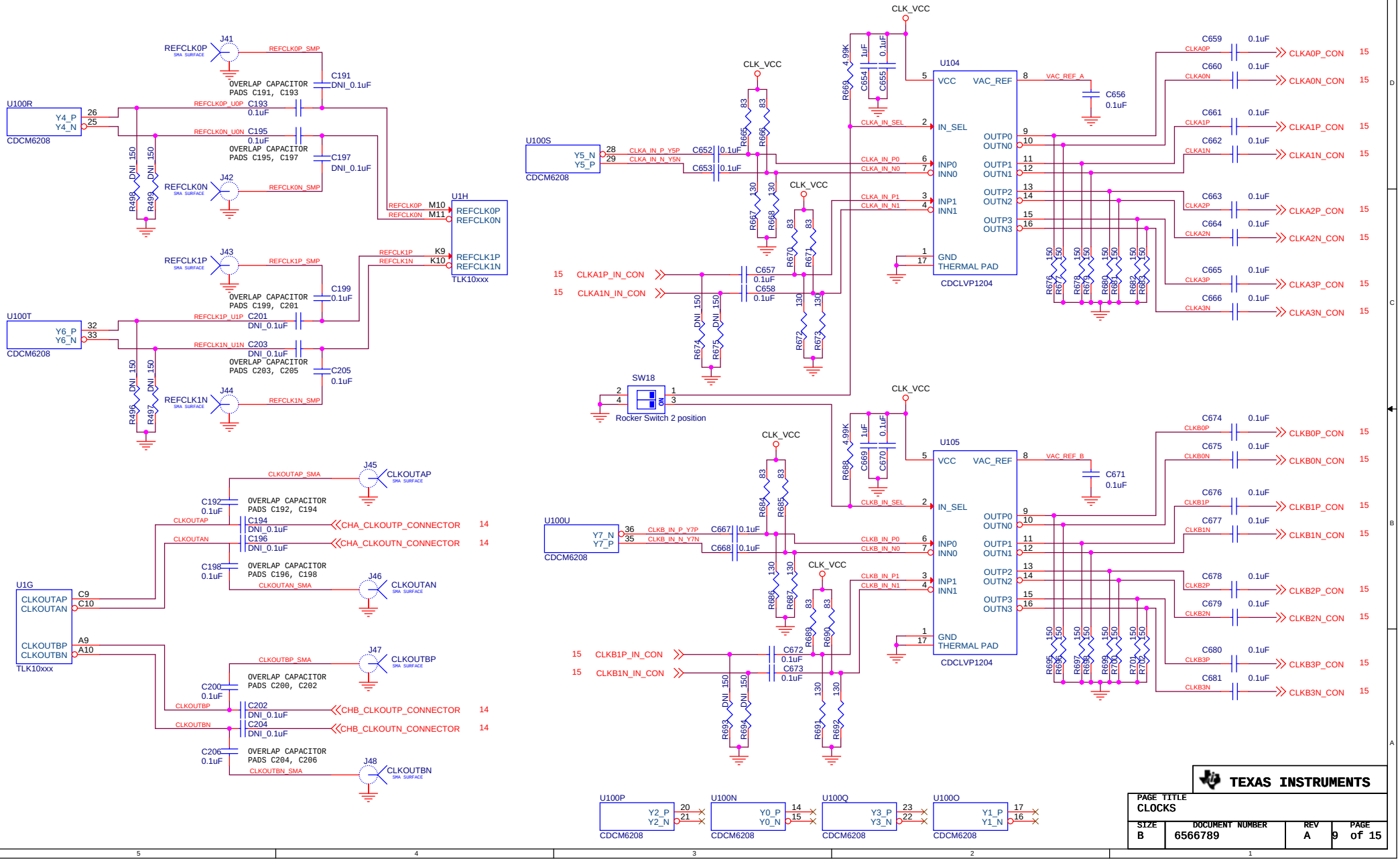
NOTE:
1. MATCH REFCLK0/1_P/N AND CLKOUT0/1_P/N TRACE LENGTHS TO EACHOTHER



TEXAS INSTRUMENTS

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CLOCKS			
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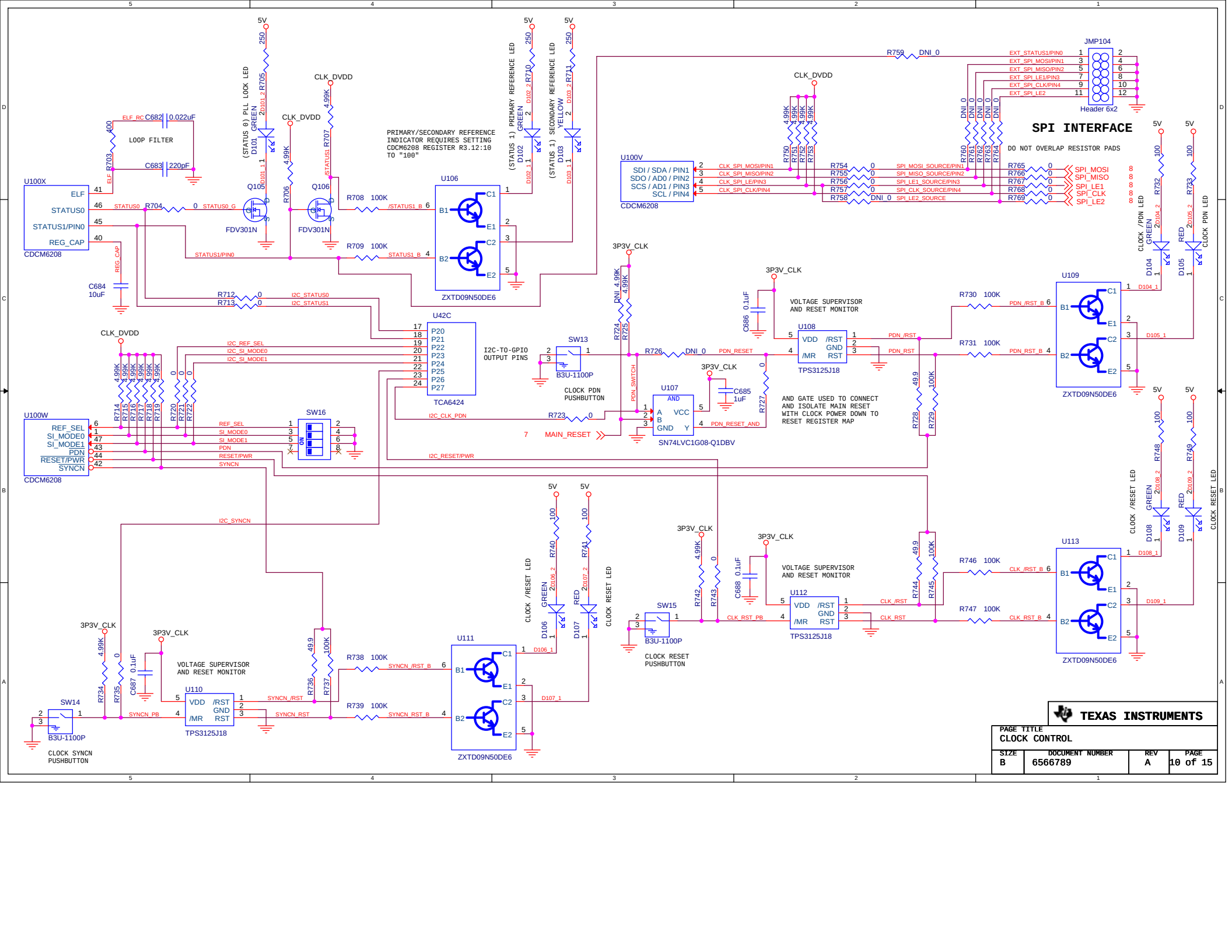
SPI INTERFACE
DO NOT OVERLAP RESISTOR PADS
PRIMARY/SECONDARY REFERENCE INDICATOR REQUIRES SETTING CDCM6208 REGISTER R3.12:10 TO "100"
LOOP FILTER
I2C-TO-GPIO OUTPUT PINS
VOLTAGE SUPERVISOR AND RESET MONITOR
AND GATE USED TO CONNECT AND ISOLATE MAIN RESET WITH CLOCK POWER DOWN TO RESET REGISTER MAP
CLOCK PDN PUSHBUTTON
CLOCK RESET PUSHBUTTON
CLOCK SYNCN PUSHBUTTON
TEXAS INSTRUMENTS
PAGE TITLE
CLOCK CONTROL
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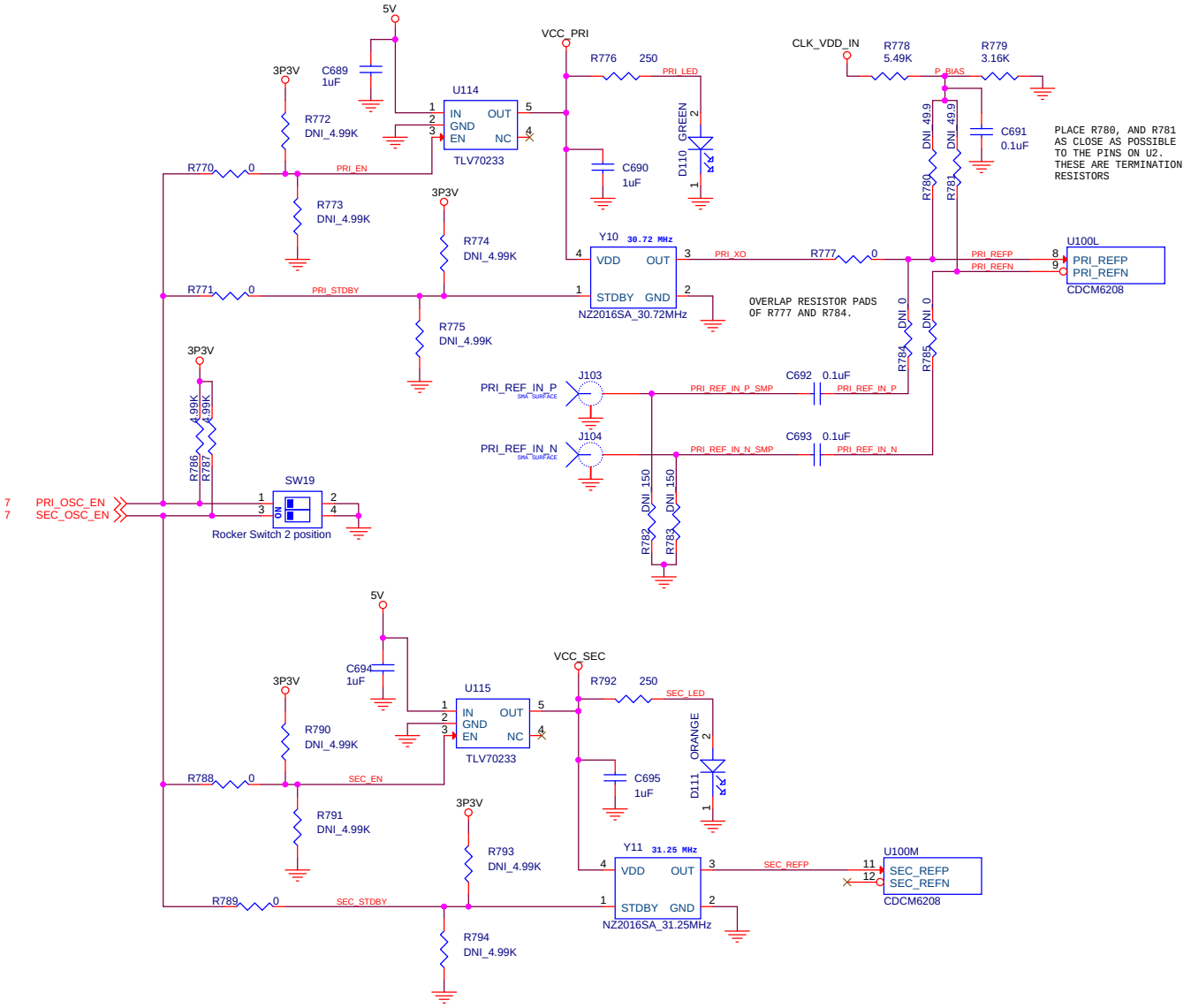
NOTE:



TEXAS INSTRUMENTS

PAGE TITLE			
CRYSTAL OSCILLATORS			
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NOTE:
1. MATCH LOW SPEED INPUT AND OUTPUT TRACE LENGTHS TO EACHOTHER
2. MATCH HIGH SPEED TRANSMIT AND RECEIVE TRACE LENGTHS TO EACHOTHER

TEXAS INSTRUMENTS

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LOW SPEED DATA SIGNALS			
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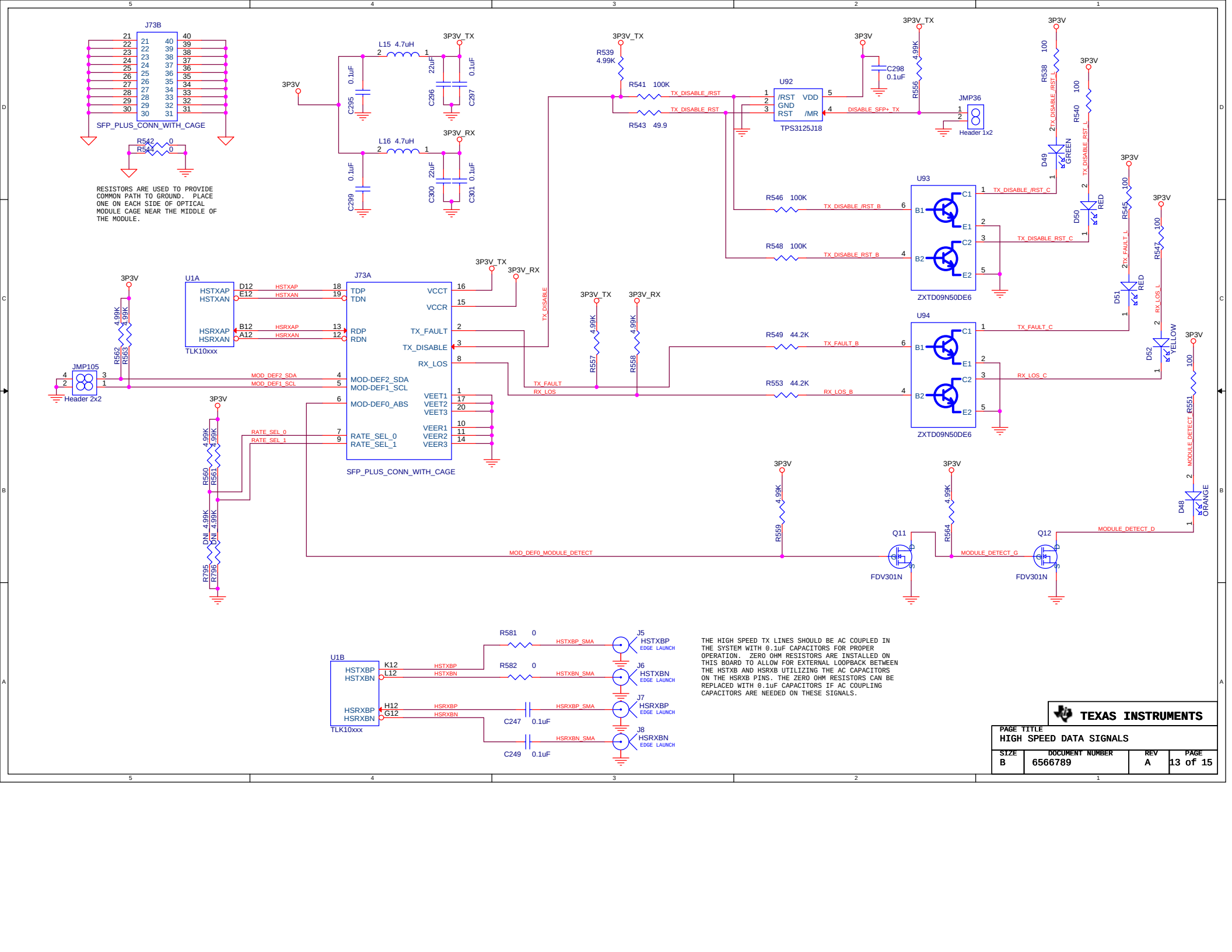
J73B
SFP_PLUS_CONN_WITH_CAGE
R542 0
R544 0
RESISTORS ARE USED TO PROVIDE COMMON PATH TO GROUND. PLACE ONE ON EACH SIDE OF OPTICAL MODULE CAGE NEAR THE MIDDLE OF THE MODULE.
L15 4.7uH
L16 4.7uH
3P3V
3P3V_TX
3P3V_RX
C295 0.1uF
C296 22uF
C297 0.1uF
C299 0.1uF
C300 22uF
C301 0.1uF
R539 4.99K
R541 100K
R543 49.9
TX_DISABLE_/RST
TX_DISABLE_RST
U92
TPS3125J18
/RST VDD
GND
RST /MR
DISABLE_SFP+_TX
C298 0.1uF
R556 4.99K
JMP36
Header 1x2
R538 100
R540 100
D49 GREEN
D50 RED
U93
ZXTD09N50DE6
R546 100K
R548 100K
TX_DISABLE_/RST_C
TX_DISABLE_RST_C
R545 100
R547 100
D51 RED
D52 YELLOW
U94
R549 44.2K
R553 44.2K
TX_FAULT_C
RX_LOS_C
U1A
TLK10xxx
HSTXAP
HSTXAN
HSRXAP
HSRXAN
J73A
SFP_PLUS_CONN_WITH_CAGE
TDP
TDN
RDP
RDN
VCCT
VCCR
TX_FAULT
TX_DISABLE
RX_LOS
MOD-DEF2_SDA
MOD-DEF1_SCL
MOD-DEF0_ABS
RATE_SEL_0
RATE_SEL_1
VEET1
VEET2
VEET3
VEER1
VEER2
VEER3
JMP105
Header 2x2
R562 4.99K
R563 4.99K
R560 4.99K
R561 4.99K
DNI 4.99K
R795
R796
R557 4.99K
R558 4.99K
R559 4.99K
R564 4.99K
Q11 FDV301N
Q12 FDV301N
MOD_DEF0_MODULE_DETECT
MODULE_DETECT_D
MODULE_DETECT_G
R551 100
D48 ORANGE
U1B
TLK10xxx
R581 0
R582 0
C247 0.1uF
C249 0.1uF
J5 HSTXBP EDGE LAUNCH
J6 HSTXBN EDGE LAUNCH
J7 HSRXBP EDGE LAUNCH
J8 HSRXBN EDGE LAUNCH
THE HIGH SPEED TX LINES SHOULD BE AC COUPLED IN THE SYSTEM WITH 0.1uF CAPACITORS FOR PROPER OPERATION. ZERO OHM RESISTORS ARE INSTALLED ON THIS BOARD TO ALLOW FOR EXTERNAL LOOPBACK BETWEEN THE HSTXB AND HSRXB UTILIZING THE AC CAPACITORS ON THE HSRXB PINS. THE ZERO OHM RESISTORS CAN BE REPLACED WITH 0.1uF CAPACITORS IF AC COUPLING CAPACITORS ARE NEEDED ON THESE SIGNALS.
TEXAS INSTRUMENTS
PAGE TITLE
HIGH SPEED DATA SIGNALS
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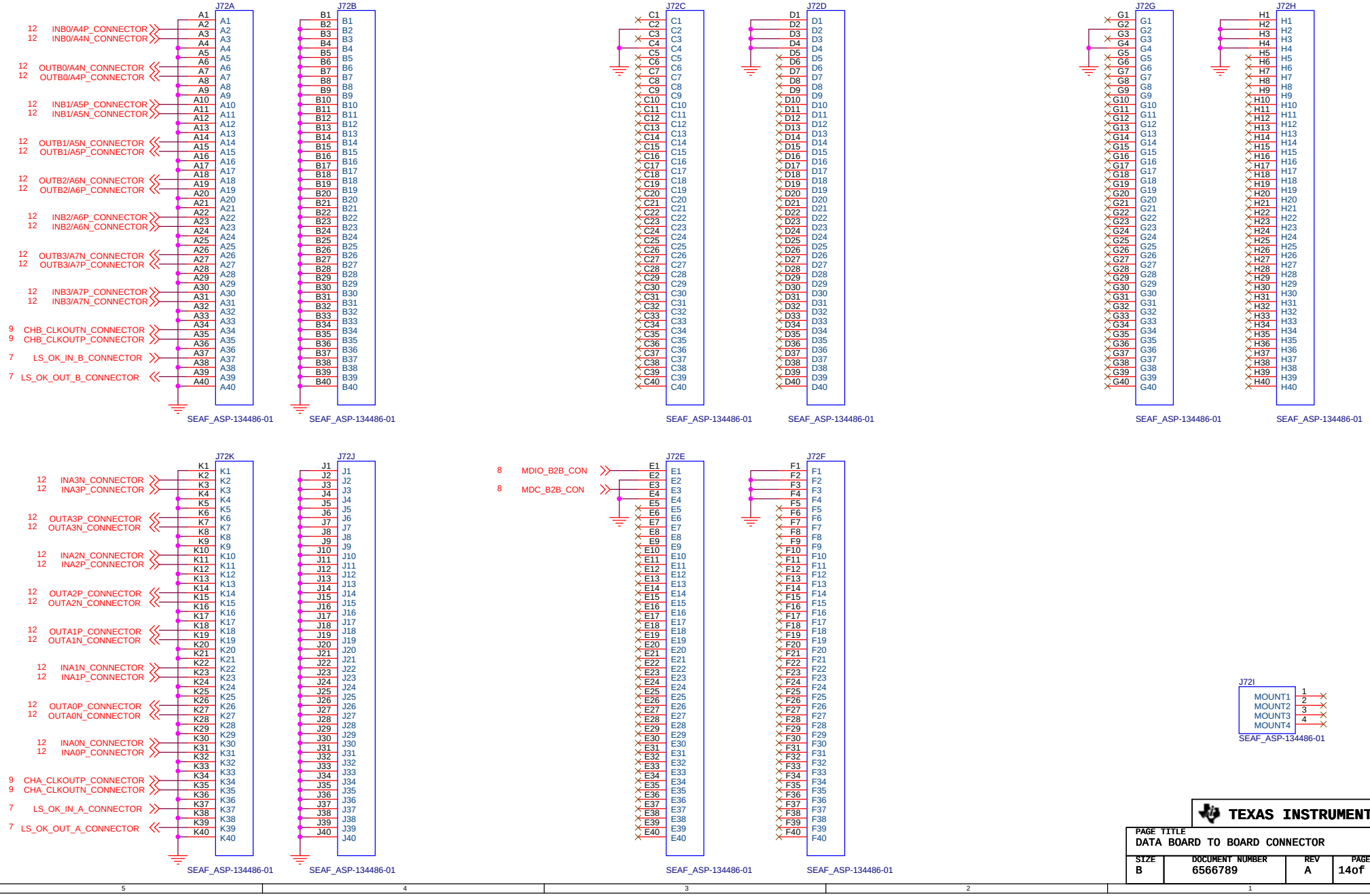

TEXAS INSTRUMENTS

PAGE TITLE			
DATA BOARD TO BOARD CONNECTOR			
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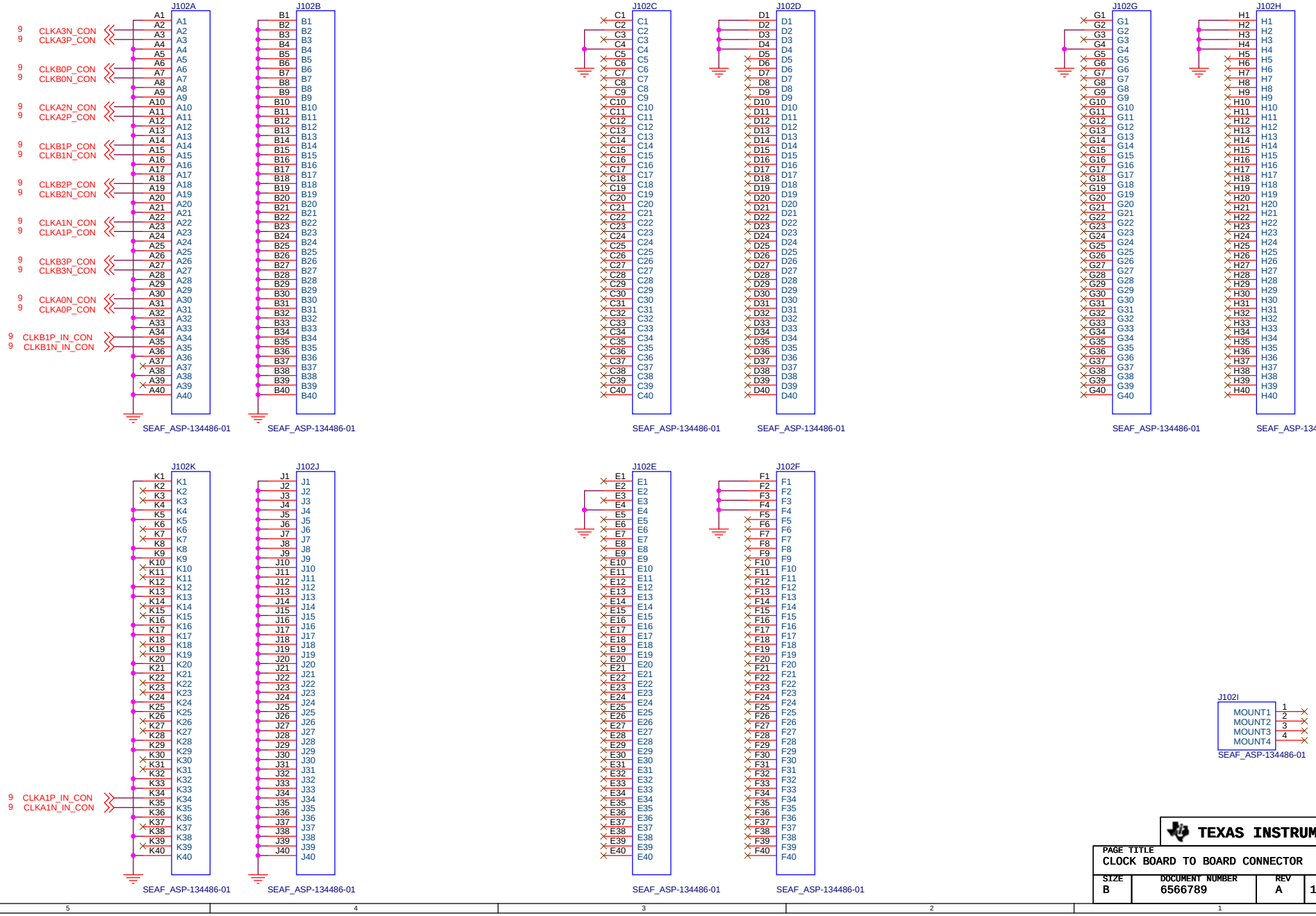

TEXAS INSTRUMENTS

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CLOCK BOARD TO BOARD CONNECTOR			
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