USB_TX_CLK, USB_TX_DATA[15:0], USB_TX_DATAK[1:0], USB_PCLK,
USB_RX_DATA[15:0], USB_RX_DATAK[1:0], USB_RX_VALID
should be matched in length to within 250 mils and kept to less
than 2 inches in length with an impedance of 50 Ω ±10%.

Close to TUSB1310A USB PHY

Close to FPGA

Near U3 Connector

VBUS_5V For OTG Host, if be device then don't use

USB_ULPI_DATA5	USB_ULPI_DATA4	reference clock ON X1
0	0	20 MHz
0	1	25 MHz
1	0	30 MHz
1	1	40 MHz

0	SSC enable
1	SSC disable

0	16-bit PIPE SDR mode
1	ISO_START

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