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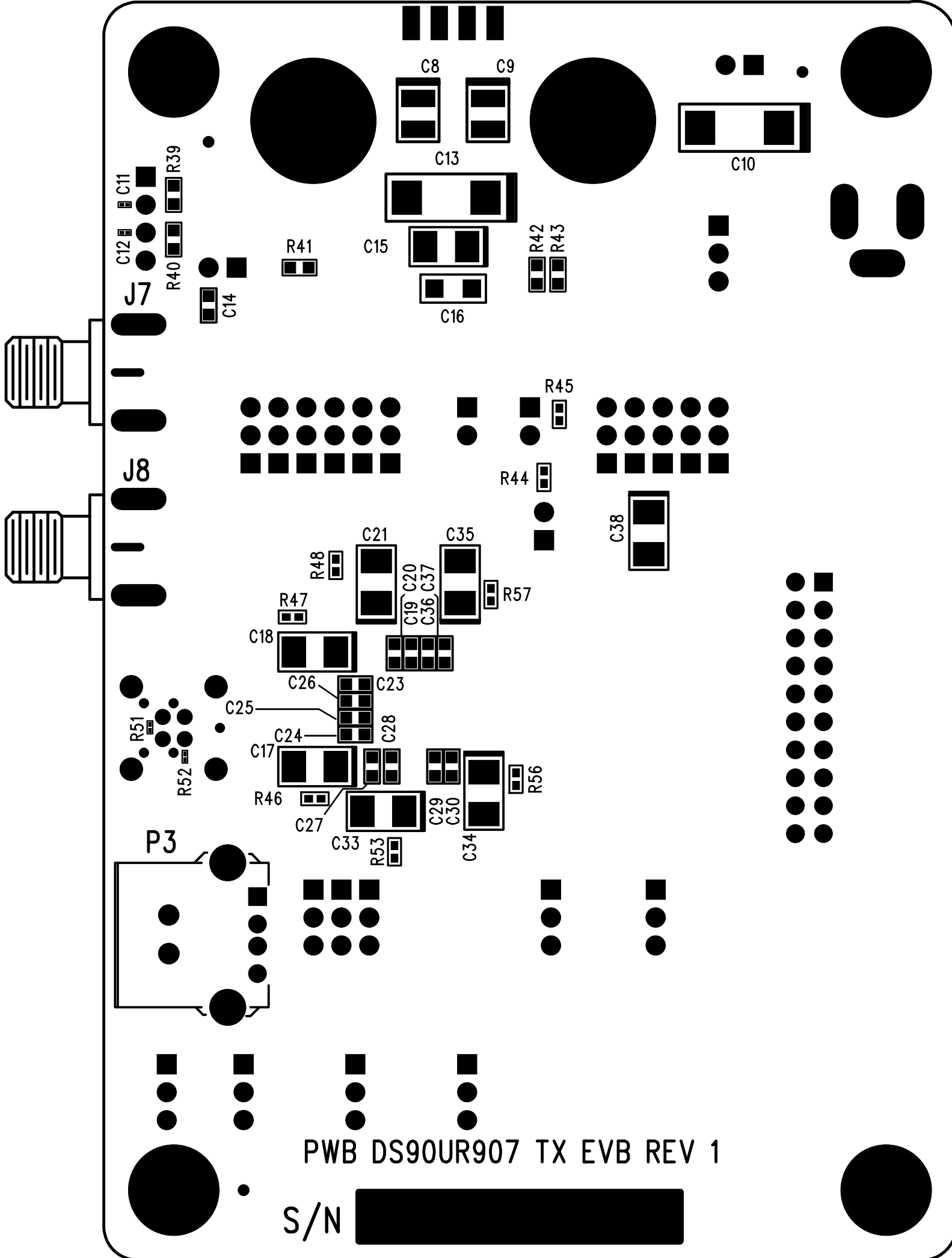
National Semiconductor

NOT FOR EMI TESTING

- JP32: +3.3V, VDDP, +1.8V
- JP31: +3.3V, VDDHS, +1.8V
- JP13: VDD, RED, VSS
- JP14: VDD, BLK, VSS

TX EVB REV

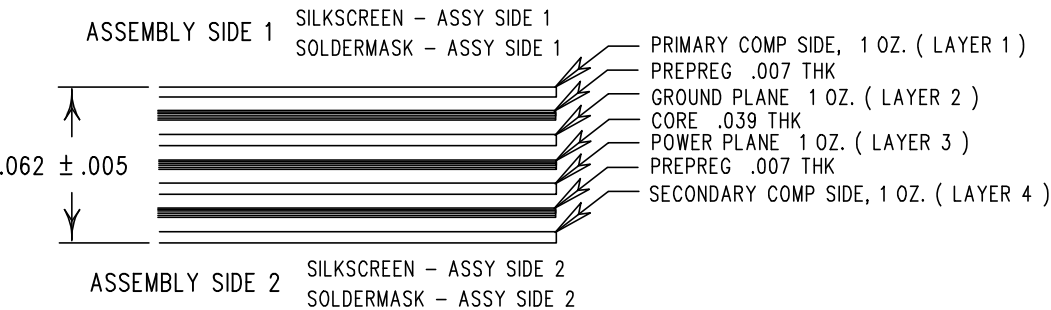
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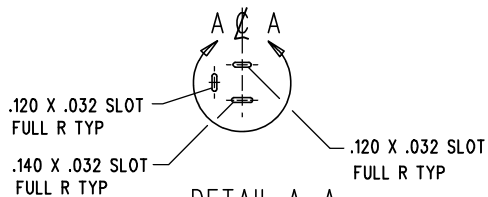
PWB DS90UR907 TX EVB REV 1

S/N





HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.006	20	YES	± .003
×	0.010	26	YES	± .003
□	0.016	50	YES	± .003
◇	0.035	10	YES	± .003
⊗	0.040	30	YES	± .003
⊠	0.043	67	YES	± .003
A	0.065	4	YES	± .003
B	0.091	2	YES	± .003
C	0.156	4	YES	± .004
D	0.265	2	YES	± .005
E	0.032	3	YES	± .003



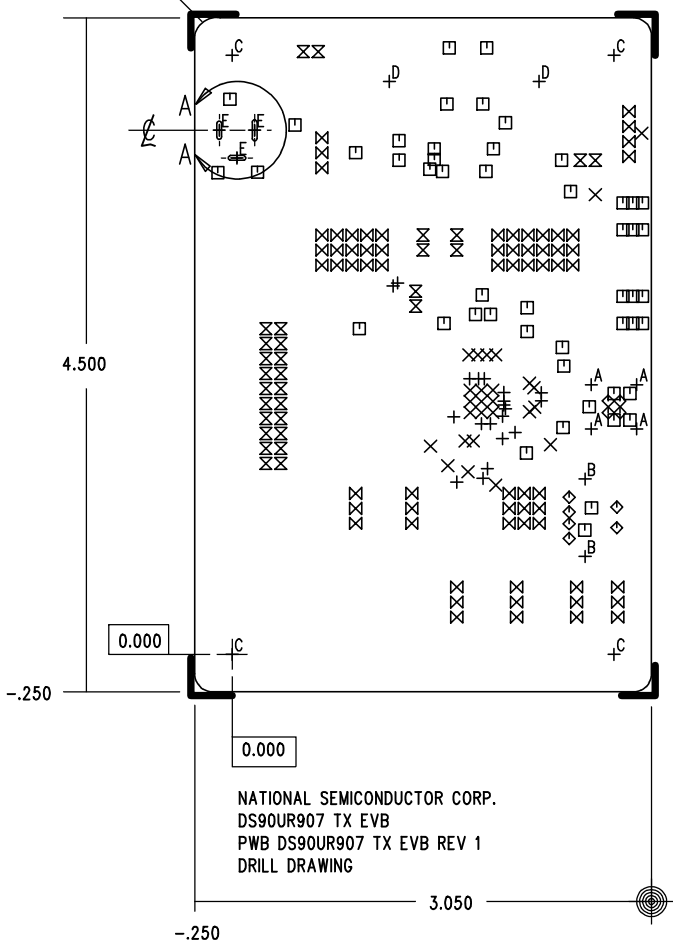
THRU HOLE SLOT - SEE DETAIL A-A

DETAIL A-A

SCALE 1:1 ROT 90° CW

NOTE: .032 DRILL AT SLOT CENTER
PER NC DRILL FILE

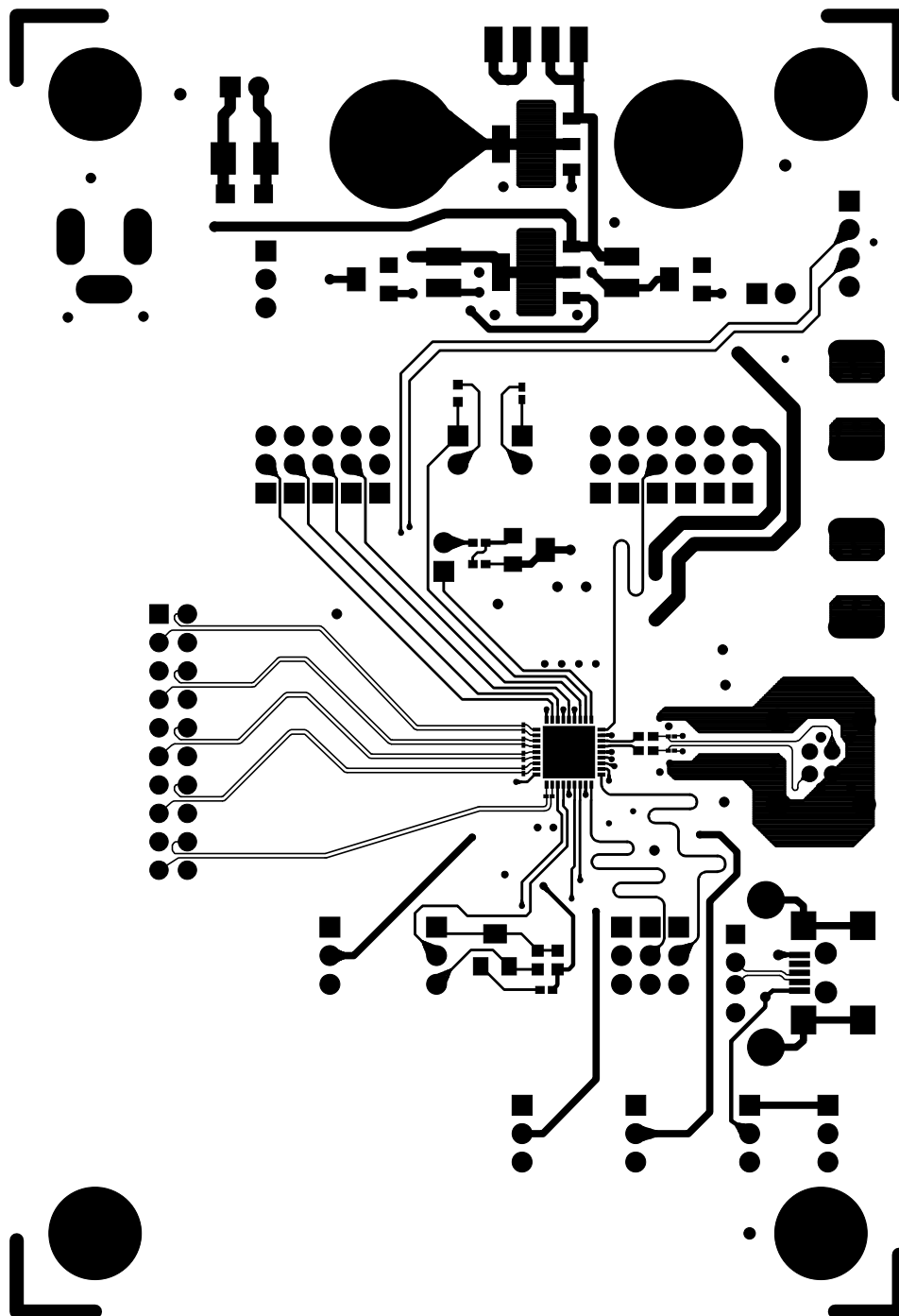
.12 R TYP
4 PLCS



NATIONAL SEMICONDUCTOR CORP.
DS90UR907 TX EVB
PWB DS90UR907 TX EVB REV 1
DRILL DRAWING

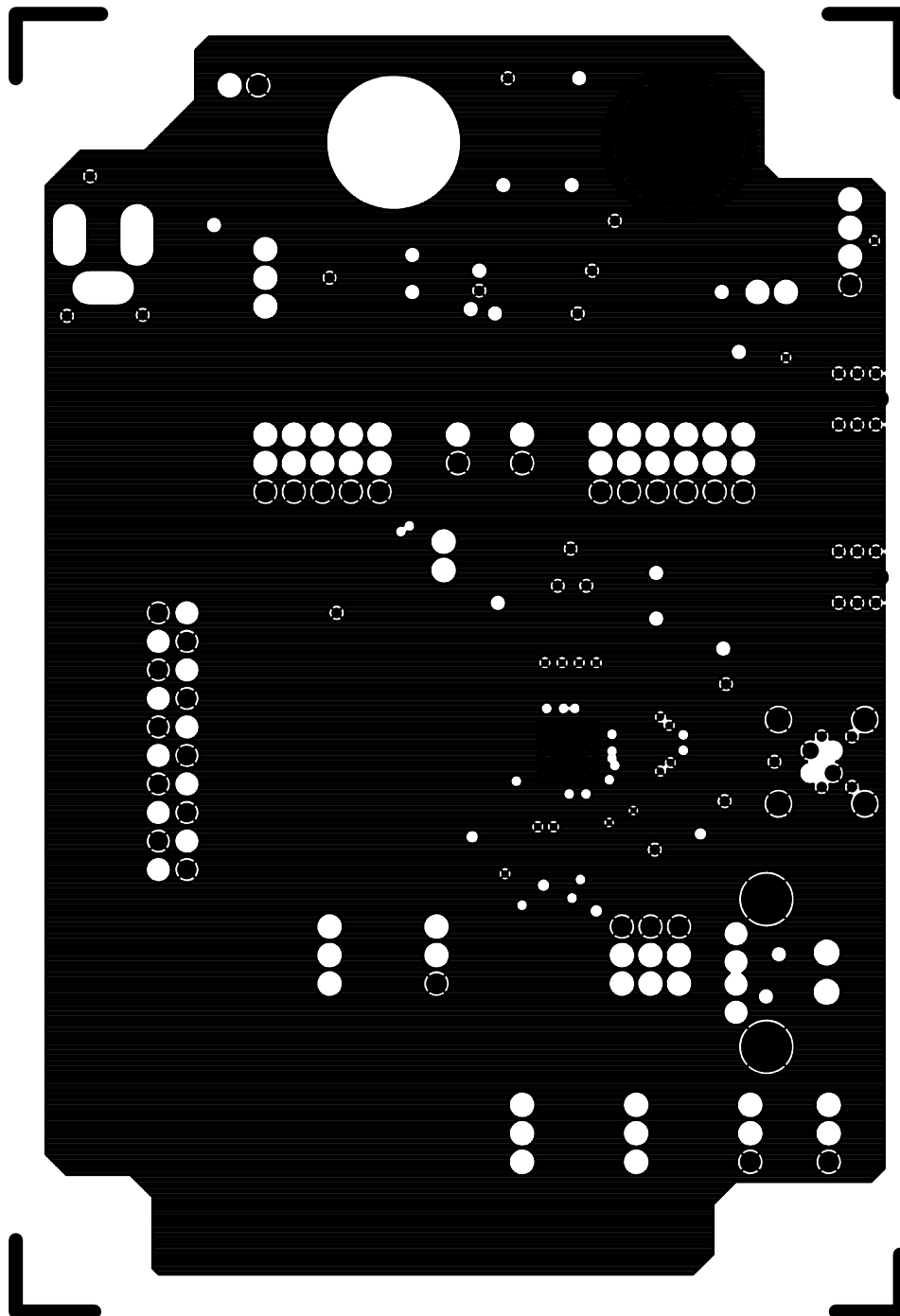
NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. DELETED.
3. FABRICATE USING MASTER FILM PWB DS90UR907 TX EVB REV 1. USE GERBER FILE A678BOA.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC-A-600, CLASS 2
5. MATERIAL: BASE MATERIAL IS ISOLA 410 OR FR-370HR, COLOR GREEN, 0.062 INCH NOM. THICKNESS. COPPER CLADDING SHALL BE 1 OZ.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER. EXPOSED PADS / TRACES SHALL BE PLATED .000030 MIN GOLD OVER NICKEL, .000150 MIN. ENIG.
7. FABRICATION TOLERANCES:
END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .002 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .010 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .010 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC-SM-840, TYPE A, CLASS B. COLOR-GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR-WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .00975 TRACES (LAYER 1 & 4) TO BE 50 OHM SINGLE ENDED IMPEDANCE AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO-MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/- 10%.



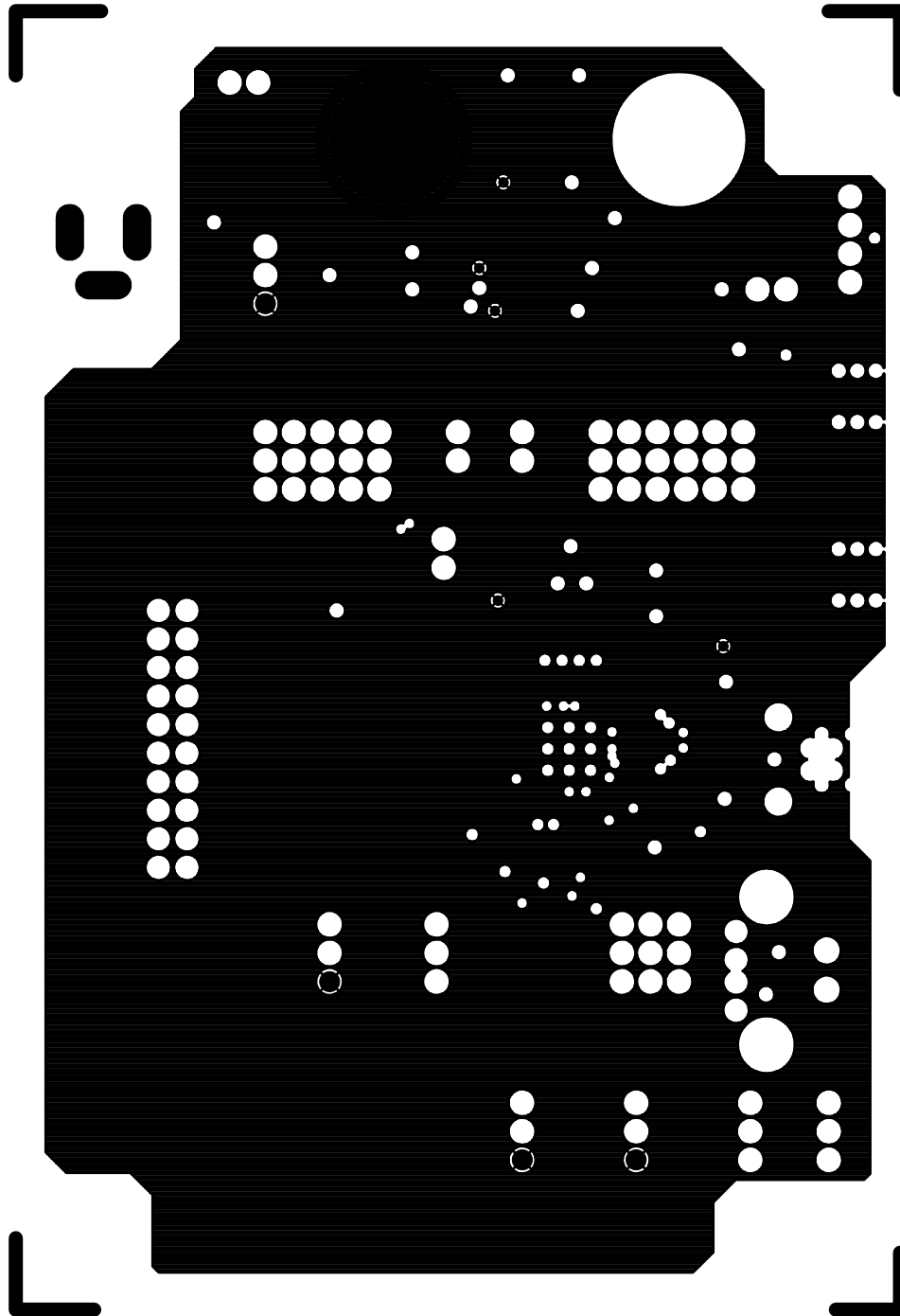
NATIONAL SEMICONDUCTOR CORP.
DS90UR907 TX EVB
PWB DS90UR907 TX EVB REV 1
PRIMARY COMP SIDE - LAYER 1





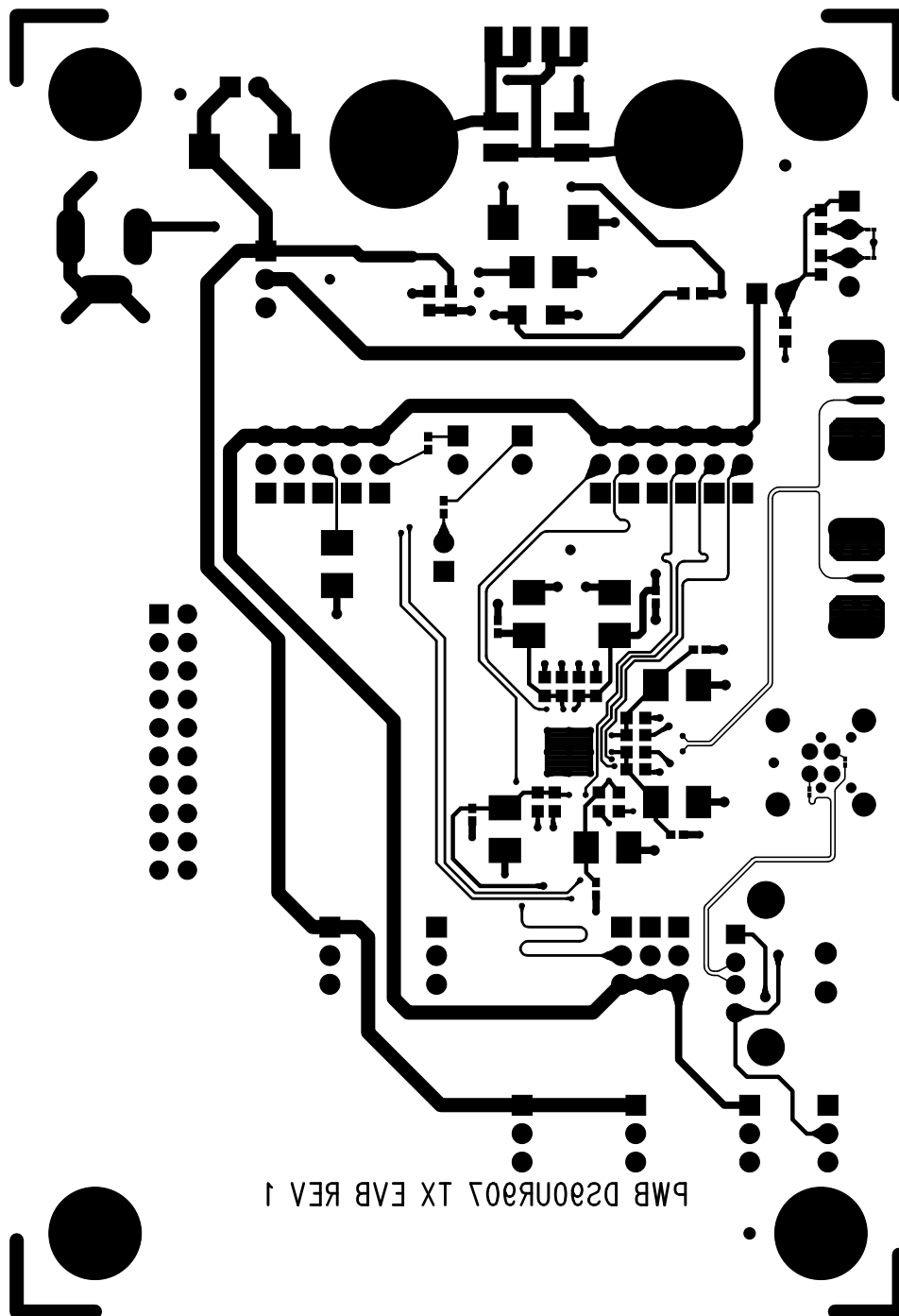
NATIONAL SEMICONDUCTOR CORP.
DS90UR907 TX EVB
PWB DS90UR907 TX EVB REV 1
GROUND PLANE - LAYER 2





NATIONAL SEMICONDUCTOR CORP.
DS90UR907 TX EVB
PWB DS90UR907 TX EVB REV 1
POWER PLANE - LAYER 3

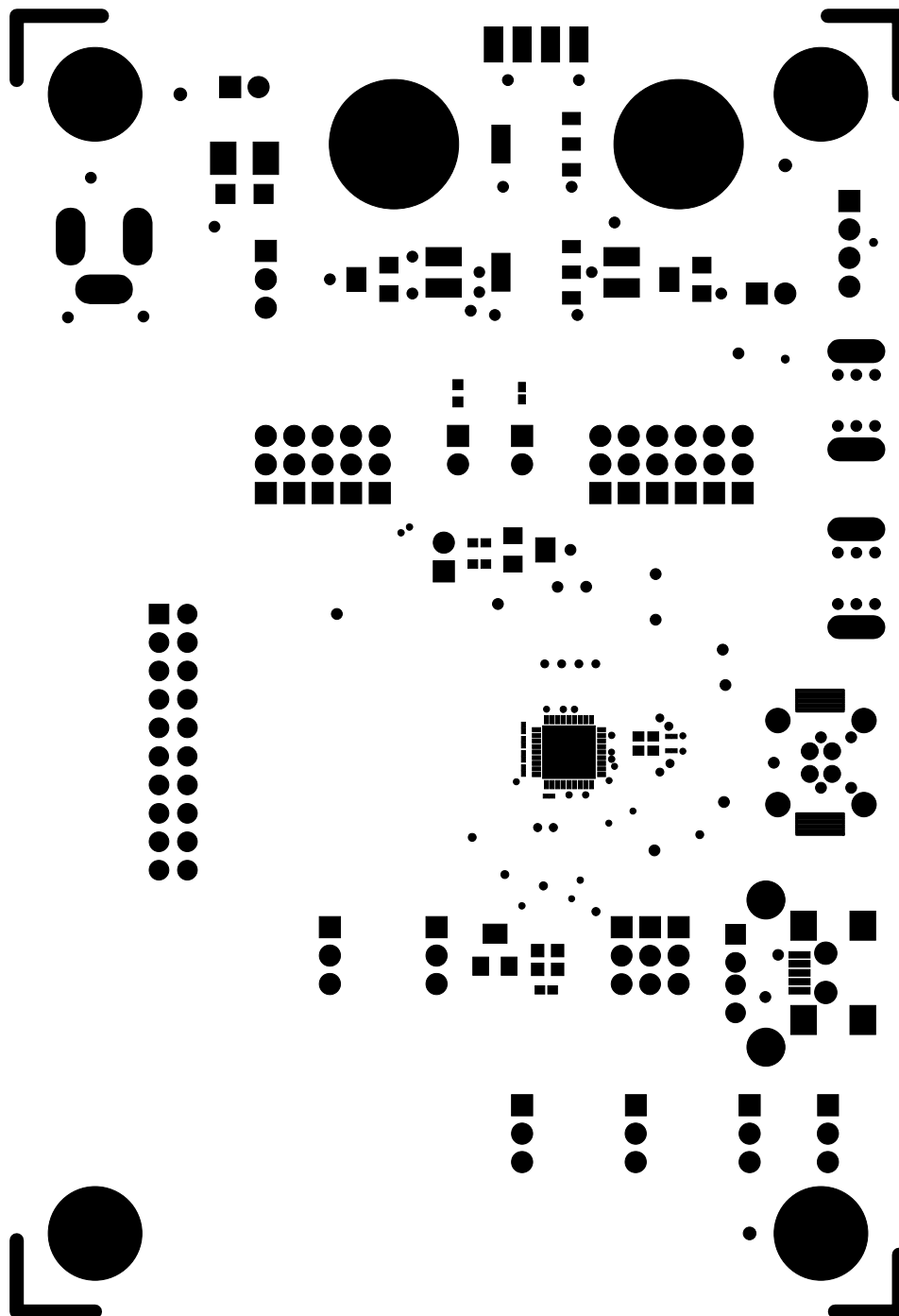




PWB DS90UR907 TX EVB REV 1

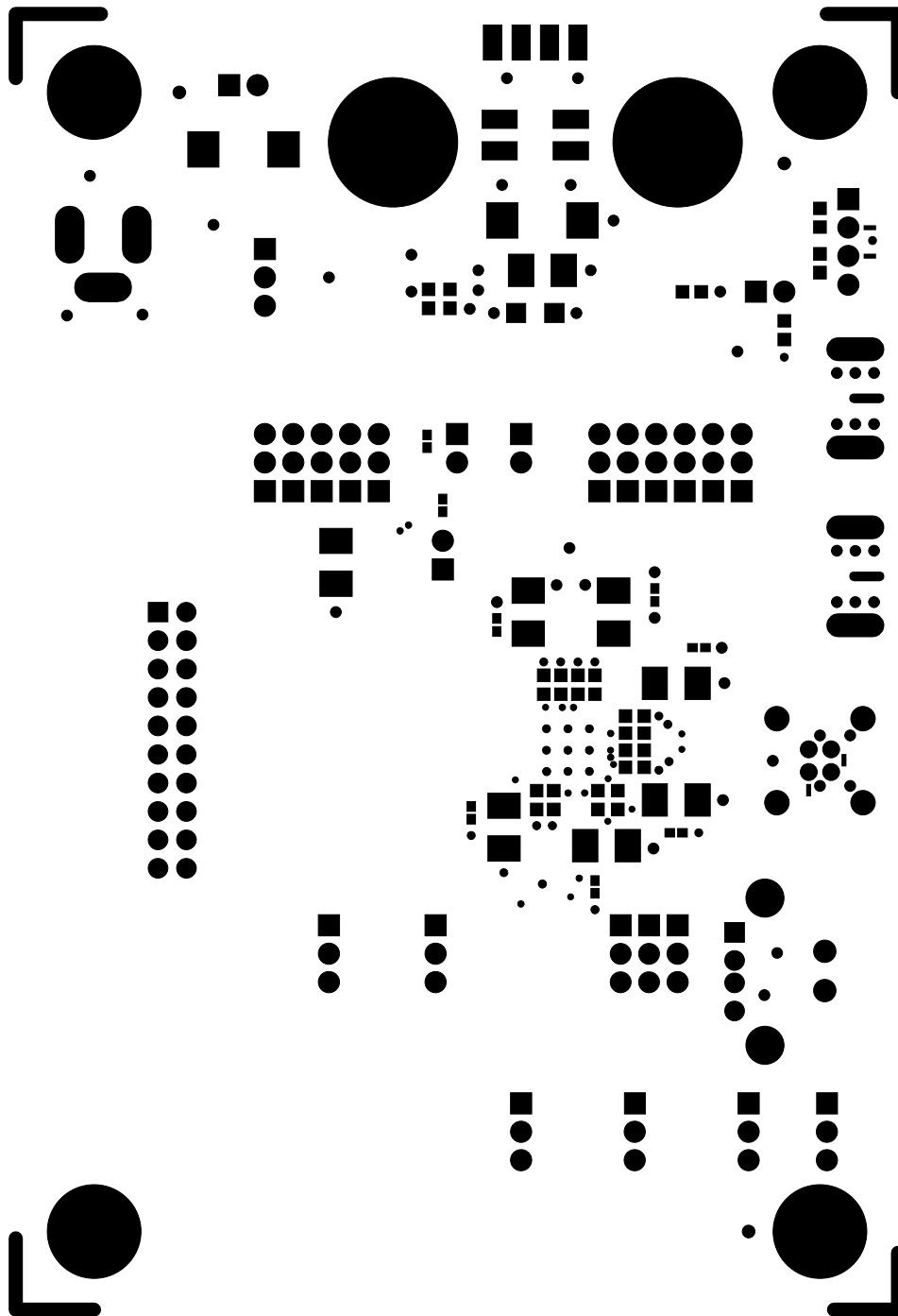
NATIONAL SEMICONDUCTOR CORP.
DS90UR907 TX EVB
PWB DS90UR907 TX EVB REV 1
SECONDARY COMP SIDE - LAYER 4





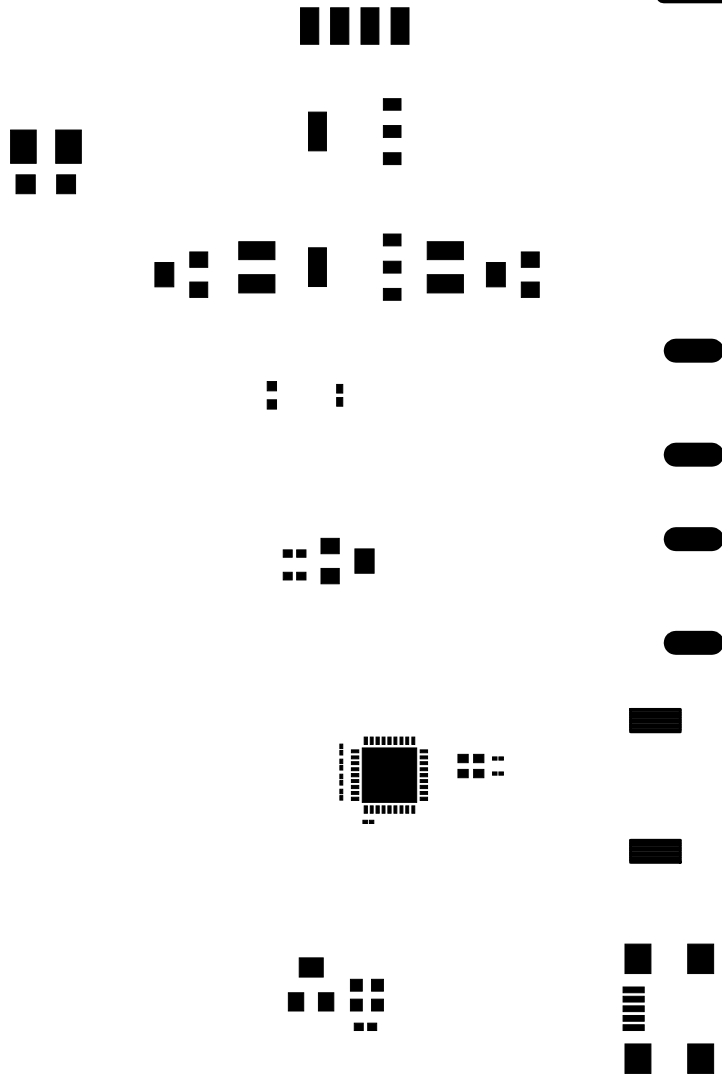
NATIONAL SEMICONDUCTOR CORP.
DS90UR907 TX EVB
PWB DS90UR907 TX EVB REV 1
PRIMARY COMP SIDE - SOLDER MASK (LAYER 1)





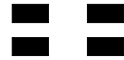
NATIONAL SEMICONDUCTOR CORP.
DS90UR907 TX EVB
PWB DS90UR907 TX EVB REV 1
SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)





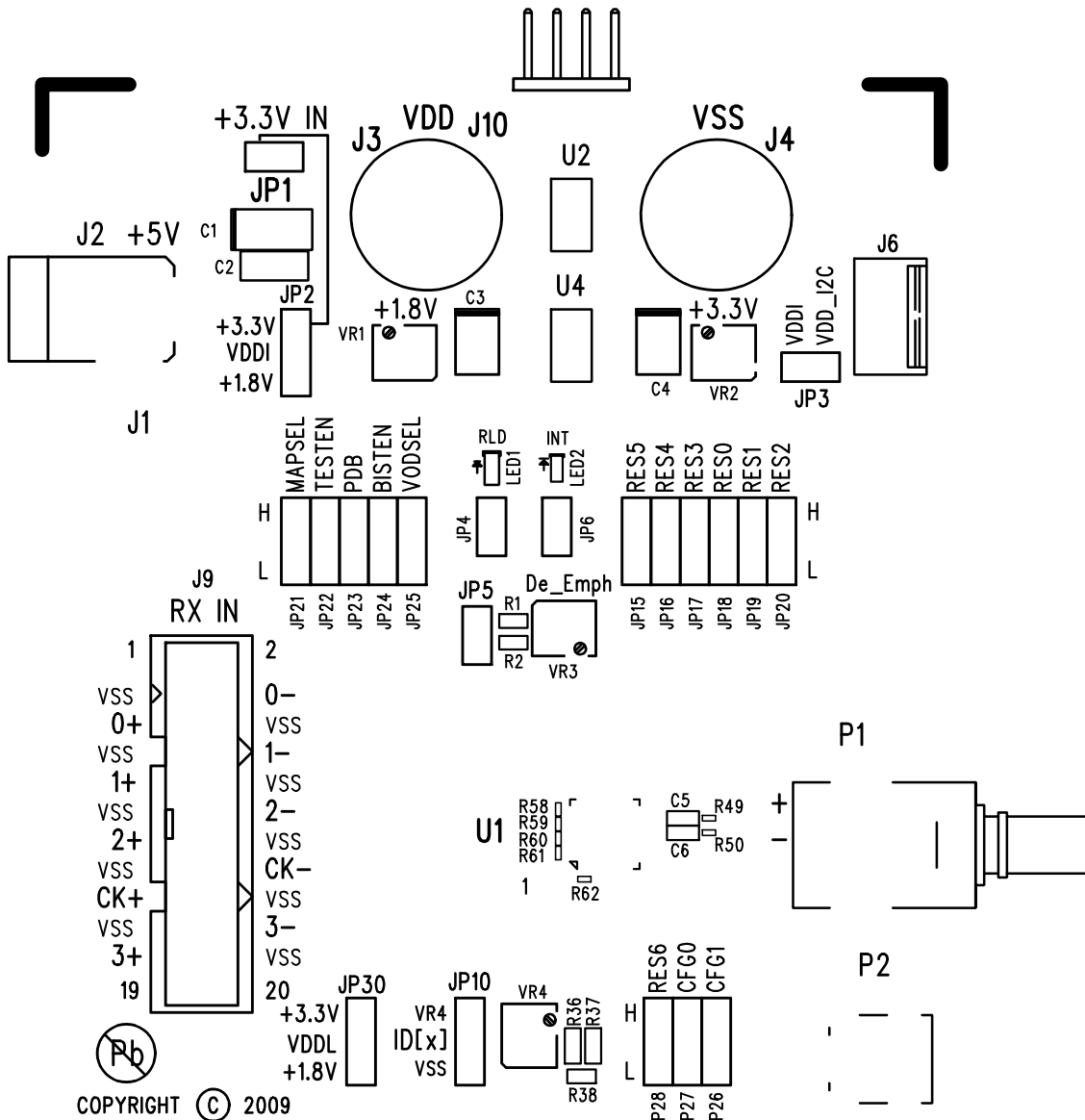
NATIONAL SEMICONDUCTOR CORP.
 DS90UR907 TX EVB
 PWB DS90UR907 TX EVB REV 1
 PRIMARY COMP SIDE - SOLDER PASTE MASK





NATIONAL SEMICONDUCTOR CORP.
DS90UR907 TX EVB
PWB DS90UR907 TX EVB REV 1
SECONDARY COMP SIDE – SOLDER PASTE MASK







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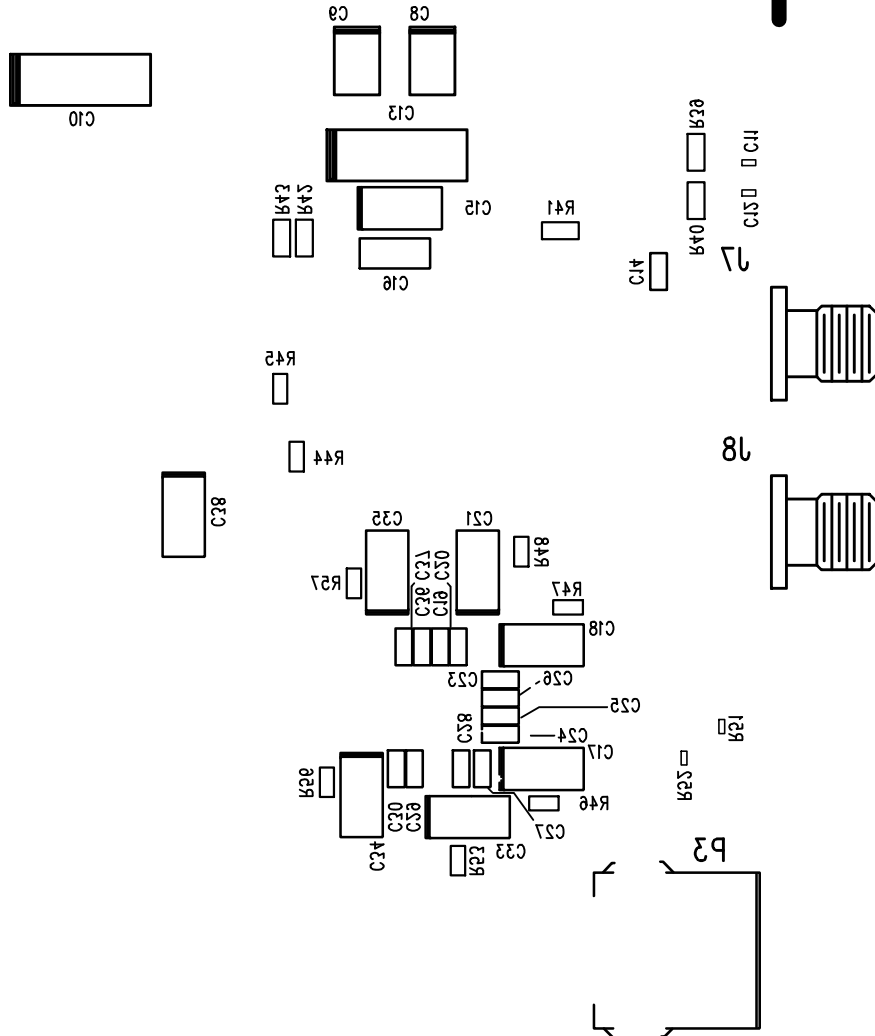
NOT FOR EMI TESTING

MADE IN U.S.A.

TX EVB REV XXXXXXXXXX

NATIONAL SEMICONDUCTOR CORP.
 DS90UR907 TX EVB
 PWB DS90UR907 TX EVB REV 1
 PRIMARY COMP SIDE – SILKSCREEN (LAYER 1)





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NATIONAL SEMICONDUCTOR CORP.
 DS90UR907 TX EVB
 PWB DS90UR907 TX EVB REV 1
 SECONDARY COMP SIDE – SILKSCREEN (LAYER 4)

