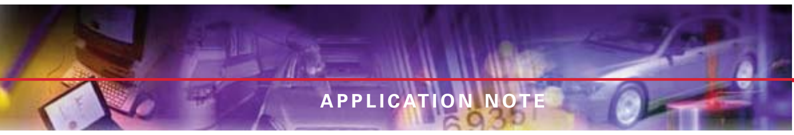

Firecomms EDL300E/D-120 PHY Transceivers Interface Design and Layout Guide

April 2007

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1 GENERAL DESCRIPTION OF DESIGN GUIDE

1.1 Features

The EDL300E-120 and EDL300D-120 Fiber Optic Transceivers (FOT) are 3.3V Ethernet transceivers supporting 100Base-FX and 10Base-FX applications over Plastic Optical Fiber (POF). The EDL300x transceivers incorporate CMOS driver and receiver ICs for high functional integration and low power consumption.

This application note discusses good design practices that apply for the interface between the transceivers and an Ethernet PHY. A description of the PCB layout is provided for typical consumer housings used for these transceivers. Meeting electromagnetic interference (EMI) and electrostatic discharge (ESD) requirements and achieving maximum line performance depends on good design practices. These practices minimize high-speed digital switching noise and common-mode noise, as well as provide shielding for the transceivers from each other and the general environment.

2 GENERAL DESIGN GUIDELINES

2.1 General Recommendations

Follow typical industry guidelines for designing and laying out the differential signals. Provide termination on all high-speed switching signals. Provide impedance matching on long traces to prevent reflections.

3 NETWORK INTERFACES

3.1 General PHY FOT Interface Application Circuit

The EDL300x transceivers have an LVDS-type interface. The DC offset voltage is 1.2V, which is compatible with LVDS. The differential voltage swing across Data+ and Data- is 550mV, which is larger than the typical LVDS differential swing of 300 to 400mV. The larger swing allows the EDL300x part to be used with a wide variety of PHY ICs, while retaining the low power consumption of the CMOS technology. The transceivers can be used with any typical Ethernet PHY interface such as PECL, LVPECL, LVDS and CML once the correct interface network is used.

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The general recommendation for interfacing to any PHY IC is given in Figure 1. It is recommended in general that AC coupling is used to avoid the problem of matching DC offsets between the EDL300x FOTs and the PHY. If DC coupling is preferred, please contact Firecomms Sales for application support.

The circuit of Figure 1 assumes that Vcc for the PHY is 3.3V, the same as for the FOTs. If the PHY is operating from a Vcc of 2.5V, Figure 2 should be used.

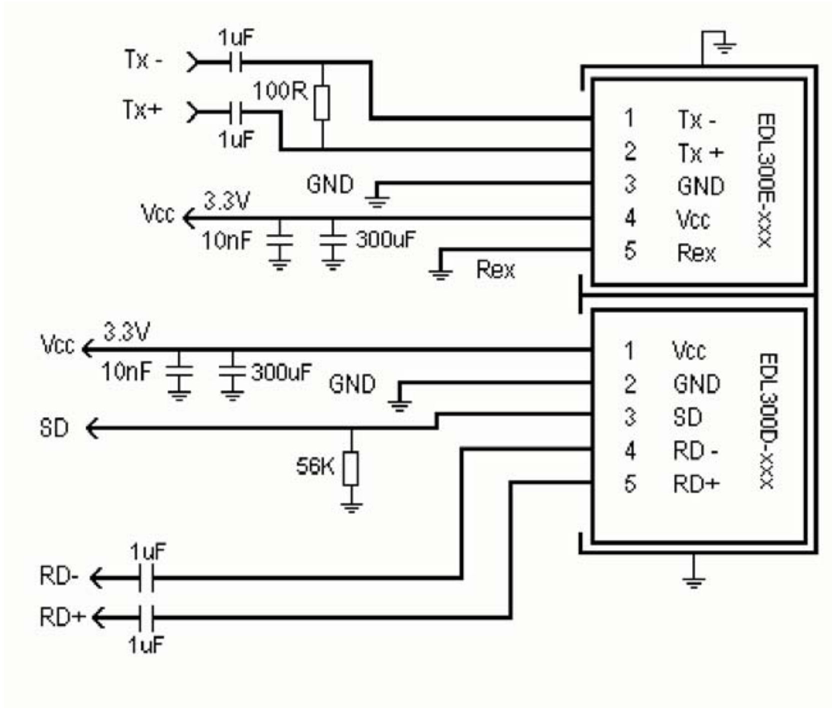

Figure 1.
General interface circuit suitable for Ethernet PHY ICs with an FX port Minimum Receiver Differential Voltage sensitivity of 550mV. This circuit assumes Vcc of 3.3V for both EDL300x and the PHY.

The circuit shown in Figure 1 shows a 100 Ohm resistor on the FOT side of the Transmitter Data+ and Data- signal lines. This resistor is for 50 Ohm differential line impedance matching of the differential signal pair. This resistor should be located as close as possible to the AC coupling capacitors. The coupling capacitors should be located as close as possible to the PHY. Termination for the PHY should be arranged in accordance with the recommended individual PHY application circuit. The receiver FOT EDL300D-120 has a 100 Ohm resistor built into the FOT itself. If the signal line is short, no further impedance matching is required. If, however, the signal line must run for more than 3cm, a 100 Ohm termination resistor should be added across the RD- and RD+ lines as close as possible to the AC coupling capacitors. In turn the AC coupling capacitors should be located as close as possible to the PHY and the termination on the PHY side of the coupling capacitors should be as recommended by the PHY manufacturer.

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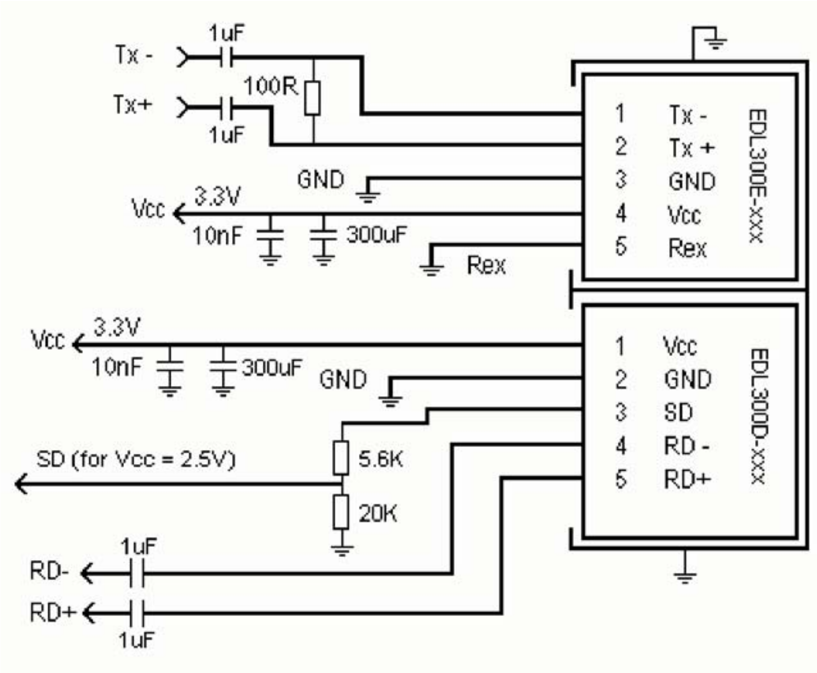

Figure 2.
General interface circuit suitable for an Ethernet PHY ICs operating from 2.5V with an FX port Minimum Receiver Differential Voltage sensitivity of 550mV. This circuit assumes Vcc of 3.3V for both EDL300x and Vcc of 2.5V for the PHY.

3.2 Interfacing to LVDS

Firecomms EDL300x devices are designed to interface directly to an LVDS interface. An LVDS-type device such as a typical SERDES IC or an FPGA can be connected directly to the circuits shown in Figures 1 or 2 as appropriate. Follow the supplier's IC data sheet recommendation for correct termination of the data signals on the IC's side of the AC coupling capacitors.

3.3 Interfacing to LVPECL

When LVPECL (3.3V or 2.5V PECL) is given as the Ethernet PHY 100BaseFX port interface, one of the options listed below should be used to connect to the Firecomms Ethernet Fibre Optic Transceivers. The key parameter required to make a decision on the correct option is the minimum differential swing of the PHY receiver signal pair. It is common in PHY data sheets to quote the single-ended voltage swing. If this is given instead of the differential voltage swing, the differential voltage swing is twice this value. For example, if a minimum single-ended voltage swing of 150mV is quoted in the data sheet, the differential swing is twice this value, i.e. 300mV.

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The differential swing of the Firecomms Ethernet Receiver is 550mV. Therefore, if a selected PHY has a minimum differential receiver sensitivity lower than this value, the relatively simple termination networks illustrated in Figures 3, 4(a) and 4(b) can be used. If, however, the minimum receiver sensitivity is greater than 550mV, a level shifting circuit must be added between the FOT receiver and the PHY receiver input as illustrated in Figure 5.

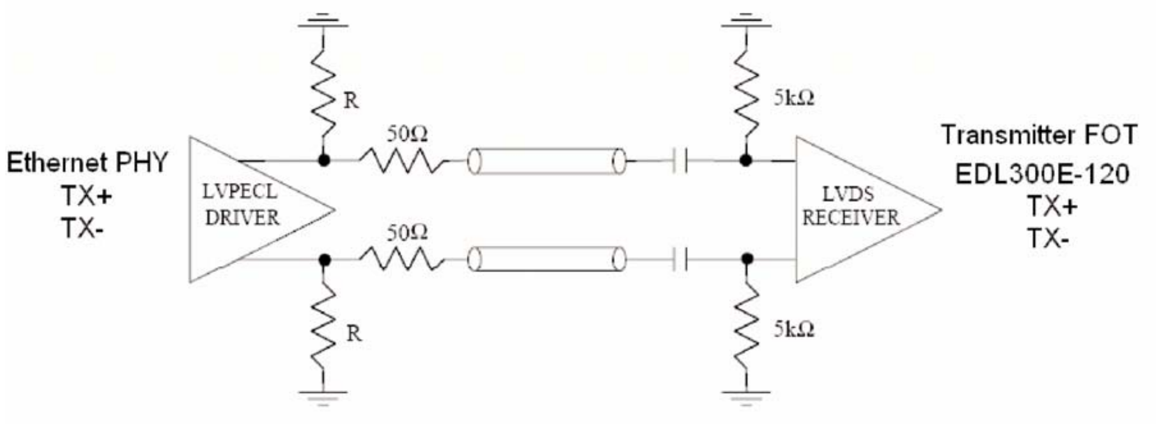

Figure 3.
Interface circuit for the transmit signals from the LVPECL Ethernet PHY to the LVDS Transmit Fiber Optic Transceiver.

The AC-coupling solution between LVPECL (the PHY transmit lines) and LVDS (the FOT transmitter) is shown in Figure 3. The LVPECL output is DC-biased through a resistor R (142 Ohm to 200 Ohm) to ground. Optimum values for R are recommended by the individual PHY IC supplier. A 50 Ohm series resistor is necessary to attenuate the LVPECL output signal to satisfy the LVDS input requirement. At the LVDS input (the transmitter FOT) a 5kΩ resistor to ground on each side is used to bias the common-mode voltage.

Packet loss testing on Ethernet links over POF demonstrates that the optimum value for the AC coupling capacitors is 1uF.

For the connection of the receiver FOT to the Ethernet PHY the schematic shown in Figure 4 applies when the PHY minimum receiver sensitivity is less than 500mV.

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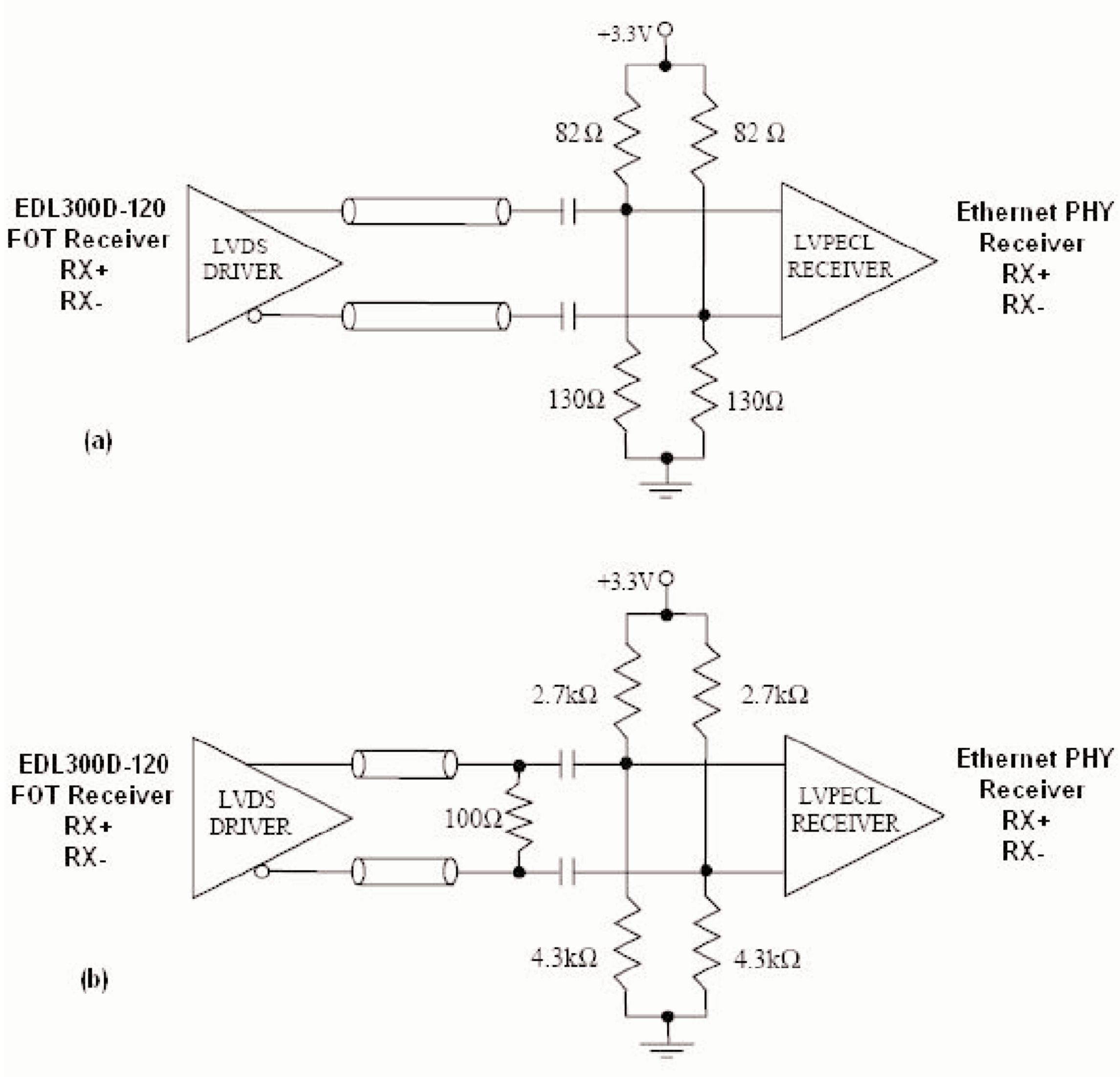

Figure 4 (a) (b).
Interface circuit for the receiver signals from the receiver Fiber Optic Transceiver to the Transmit Ethernet PHY.

The termination networks shown in Figures 4(a) and 4(b) give equal performance but have different current consumption. One or both of these options may be recommended by the PHY supplier. If the PHY has "on board" termination, the resistor network on the PHY side of the coupling capacitors is not necessary and simple direct connection to the PHY can be performed as outlined in Figure 1.

NOTE: When the PHY IC operates from 2.5V, AC coupling must be used and the signal detect line (SD) must be put through a voltage divider as illustrated in Figure 2.

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When the receiver minimum differential voltage swing is greater than 550mV, another IC must be added to the circuit to increase the voltage swing for the PHY receiver. This can be achieved using the either of the circuits shown in Figures 5 or 6.

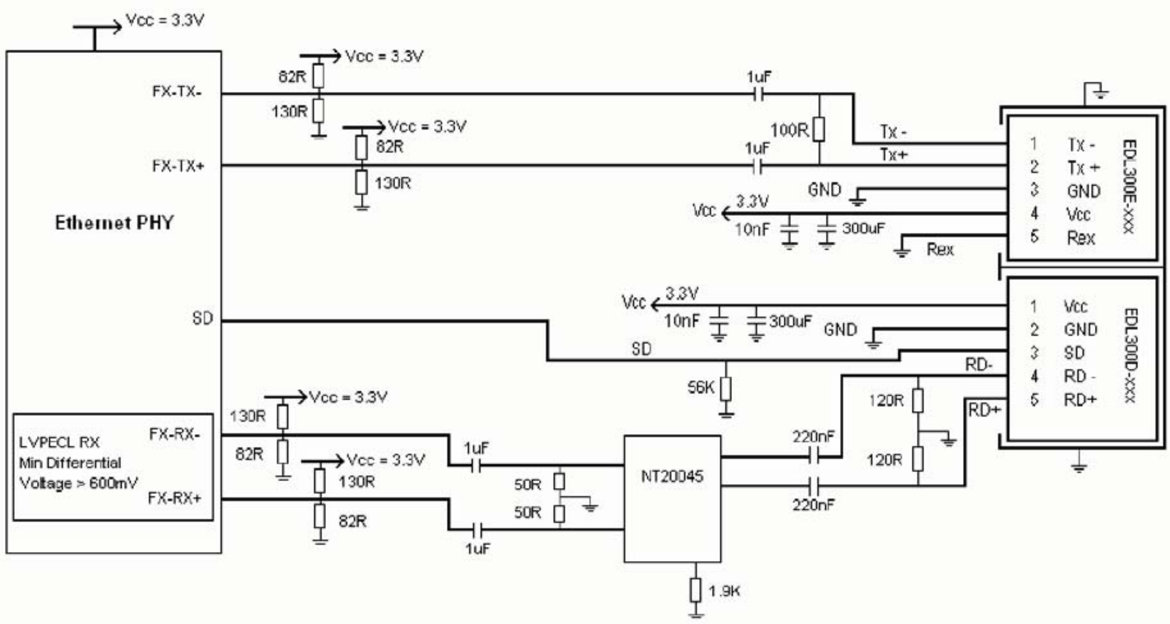

Figure 5.
Interface circuit for LVPECL when the minimum receiver differential voltage sensitivity of the Ethernet PHY is greater than 550mV. This circuit uses a limiting amplifier NT20045 with a minimum differential swing output of 800mV to ensure full compatibility with the PHY. Contact Firecomms sales for availability of the NT20045.

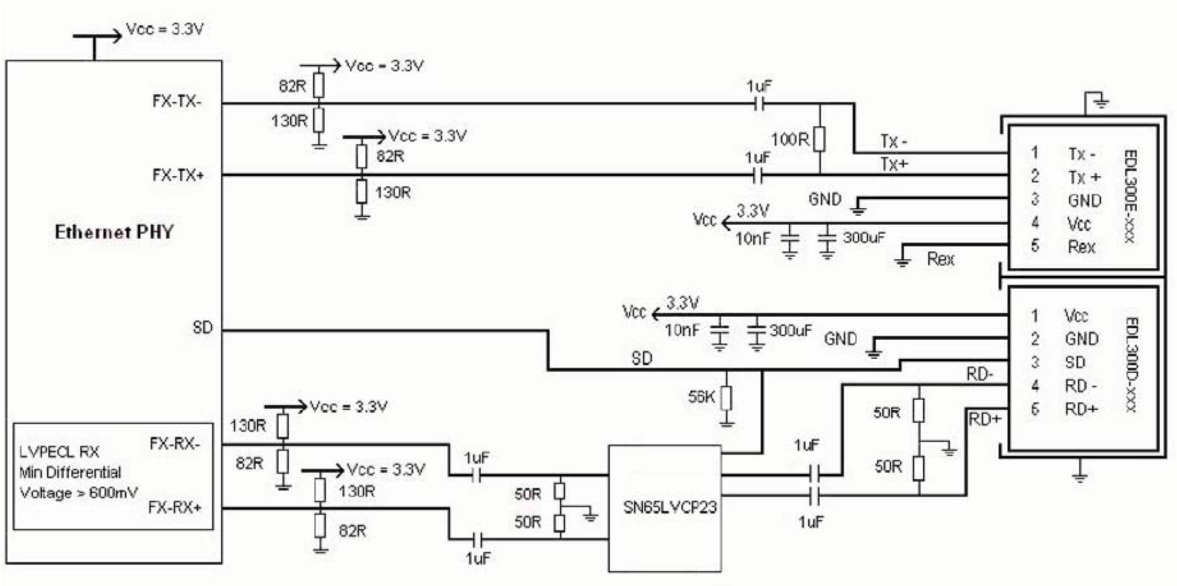

Figure 6.
Interface circuit for LVPECL when the minimum receiver differential voltage sensitivity of the Ethernet PHY is greater than 550mV. This circuit uses an interface converter SN65LVCP23 from TI to convert the LVDS differential swing to the 800mV required for LVPECL.

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3.4 Interfacing to PECL

Interfacing to 5V PECL where the minimum differential swing is 800mV (400mV single-ended swing) requires level shifting of both the differential voltage swing of the data lines and level shifting of the signal detect (SD) voltage level to be compatible with 5V TTL. Please contact Firecomms sales for application support. The 3.3V PECL, which is known as LVPECL, is described in section 3.3.

3.5 Interfacing to CML

The LVDS to CML and CML to LVDS interfaces are relatively simple and follow the convention shown in Figure 1 or Figure 2. Figures 7 and 8 are listed here for completeness. The recommended value for the AC-coupling capacitor is 1uF .

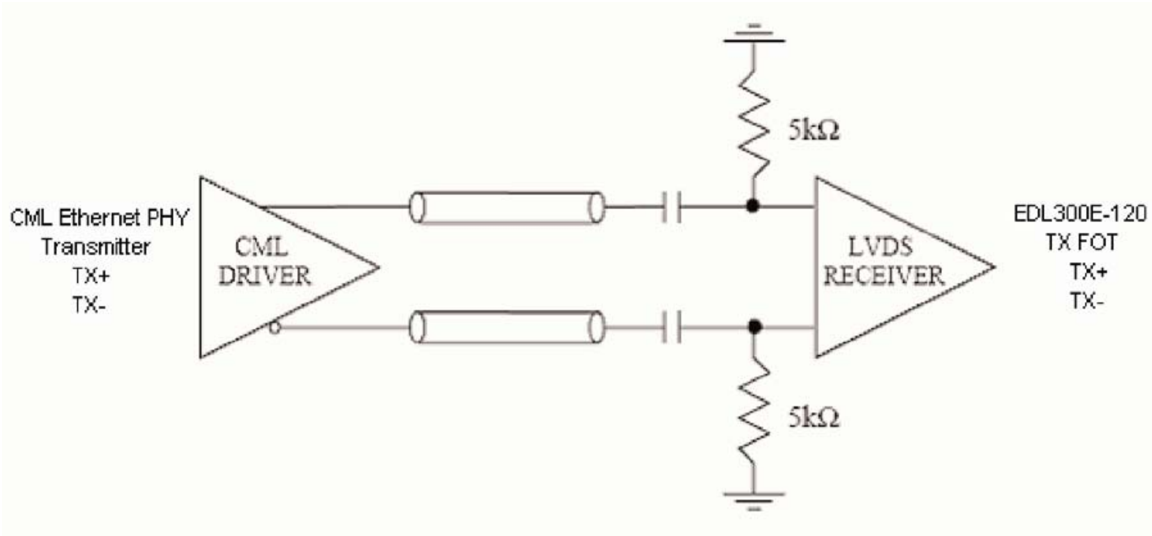

Figure 7.
Interface between the transmitter of a CML Ethernet PHY and Firecomms EDL300E-120 FOT.

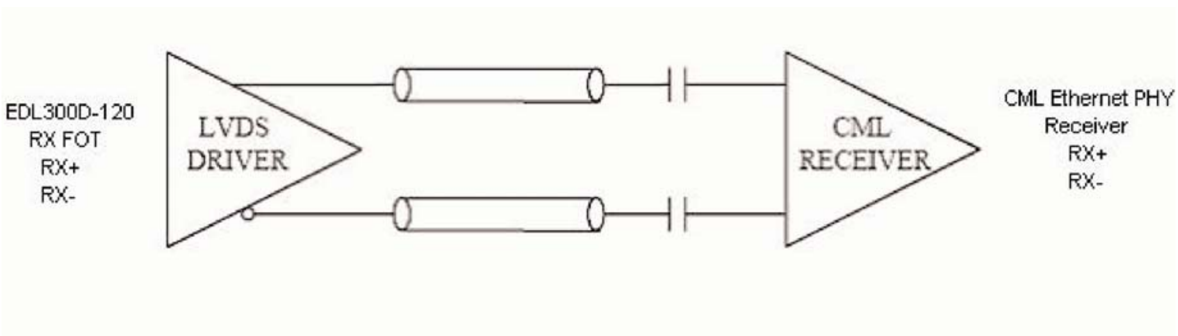

Figure 8.
interface between Firecomms EDL300D-120 FOT receiver and the CML Ethernet PHY receiver.

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3.6 Examples of Interfaces

3.6.1 IC+ Ethernet PHY

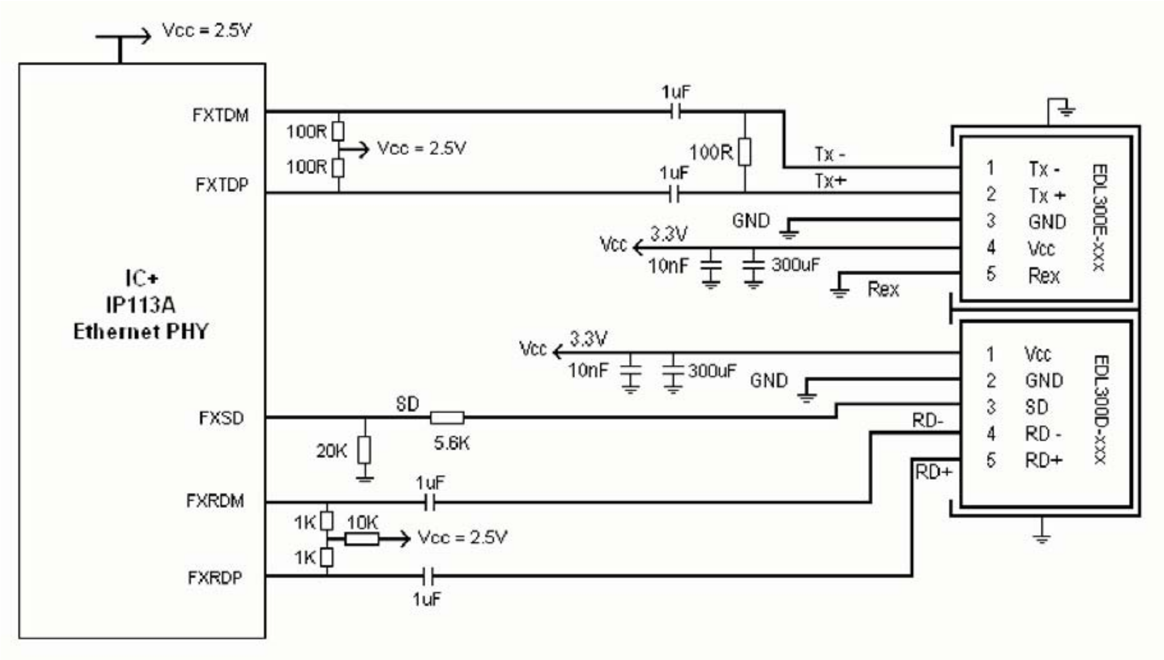

Figure 9.
IC+ 100BaseFX Ethernet PHY interface to Firecomms EDL300x FOTs.

3.6.2 MicroLinear Ethernet PHY

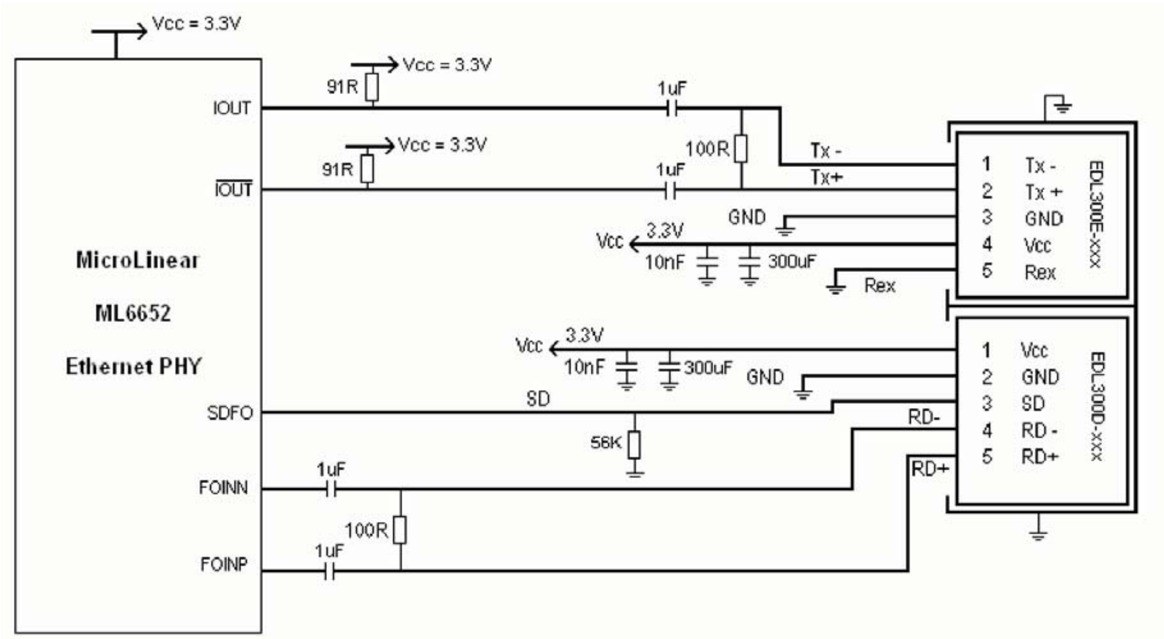

Figure 10.
MicroLinear 100BaseFX Ethernet PHY interface to Firecomms EDL300x FOTs.

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3.6.3 Broadcom Ethernet PHY

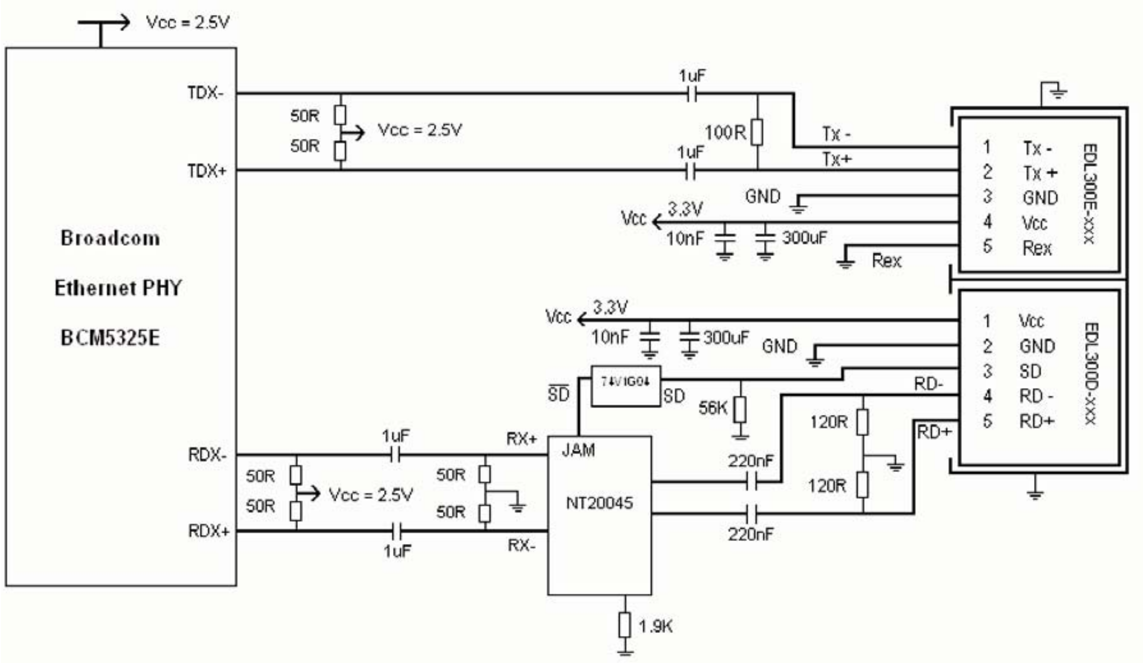

Figure 11.
Broadcom 100BaseFX Ethernet PHY interface to Firecomms EDL300x FOTs.

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4 OPTICAL AND ELECTRICAL CROSS TALK

Optical cross talk occurs when stray light from the transmitter FOT is picked up by the adjacent receiver FOT. The stray light from the transmitter interferes with the receiver and appears as signal noise. This reduces the overall system sensitivity. A physical barrier must be used to optically isolate the transmitter from the receiver.

Electrical cross talk occurs when electro-magnetic pulses generated by the pulsing action of the transmitter induce current in the receiver and thereby add noise to the receiver and reduce overall system sensitivity. A metal barrier or metalized/conductive plastic barrier must be used to isolate the transmitter FOT from the receiver FOT. The metal or conductive-plastic shield must be grounded. If conductive-plastic is being used, the bulk resistance measured across the shield must be less than 50Ω to provide sufficient electrical noise isolation.

When designing a conductive shield to isolate the transmitter and receiver FOTs care must be taken not to touch the metal tabs located at the top of the FOTs. For clearance dimensions please refer to Figure 12.

Connector systems such as the SMI have built in metalized plastic or metal barriers designed in to minimize optical and electrical cross talk. Similarly the Optolock bare-fiber housing has a metal shield to give both optical and electrical isolation of the transmit and receive FOTs.

Figures 1 and 2 illustrate the importance of a grounded shield between the transmit and receive FOTs.

5 POWER AND GROUND DESIGN

5.1 General Power and Ground Filtering

Follow good design practices to minimize noise from digital switching and power supply circuits. Ensure the power supply is rated for the load. Keep power and ground noise levels below 50mV. Use bulk capacitors (4.7 – 10uF) between the power and ground planes to minimize power supply switching noise. Use 0.01uF decoupling capacitors to reduce high-frequency noise on the power and ground planes.

For the 3.3V supply to the EDL300x transceivers it is recommended to provide a separate supply line from the main 3.3V source to each of the EDL300E-120 (transmitter FOT) and EDL300D-120 (receiver FOT) with a ferrite bead rated at 100mA with 10uF on each side of the ferrite bead to stop switching noise from traveling through the ferrite.

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It is recommended to place both a 10nF and a 300uF decoupling capacitor across the 3.3V and ground connections to both transceivers as close as possible to the component pins.

It is acknowledged that when typical consumer transceiver housings such as Optolock or connectors such as the SMI are used in combination with a single-sided board, the distance between the power line decoupling capacitors and the component pins is by necessity longer than normally recommended. For this reason, a value of 300uF, has been specified above the typical standard recommendation of 10uF.

5.2 Power and Ground Planes

Provide ample power and ground planes. Avoid breaks in the ground plane especially in areas where it is shielding high-frequency signals. Route high-speed signals above a continuous ground plane. When possible fill unused areas of the signal planes with solid copper and attach them with vias to a Vcc or ground plane that is not located adjacent to the signal layer. This technique called “signal layer filling,” can improve capacitive coupling of the power planes.

Use chassis ground in the area from the RJ45 connector to the 100/10BaseTX magnetics. Keep high-speed signals other than the data differential pairs out of the area between the EDL300x FOTs and the PHY.

When laying out ground planes care must be taken to avoid creating a loop antenna effect. Run all ground planes as solid square or rectangular regions. Avoid creating loops with ground planes around other planes.

Ensure chassis ground loop is voided at some point to prevent loop antenna effect.

5.3 Differential and Signal Layout

Route differential pairs close together and away from other signals. Keep both traces of each differential pair as identical to each other as possible. Keep each differential pair on the same plane. Minimize vias and layer changes. Keep transmit and receive pairs away from each other. Run orthogonally, or separate with a ground plane layer.

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6 MECHANICAL SPECIFICATIONS FOR PCB LAYOUT

6.1 PCB Footprint

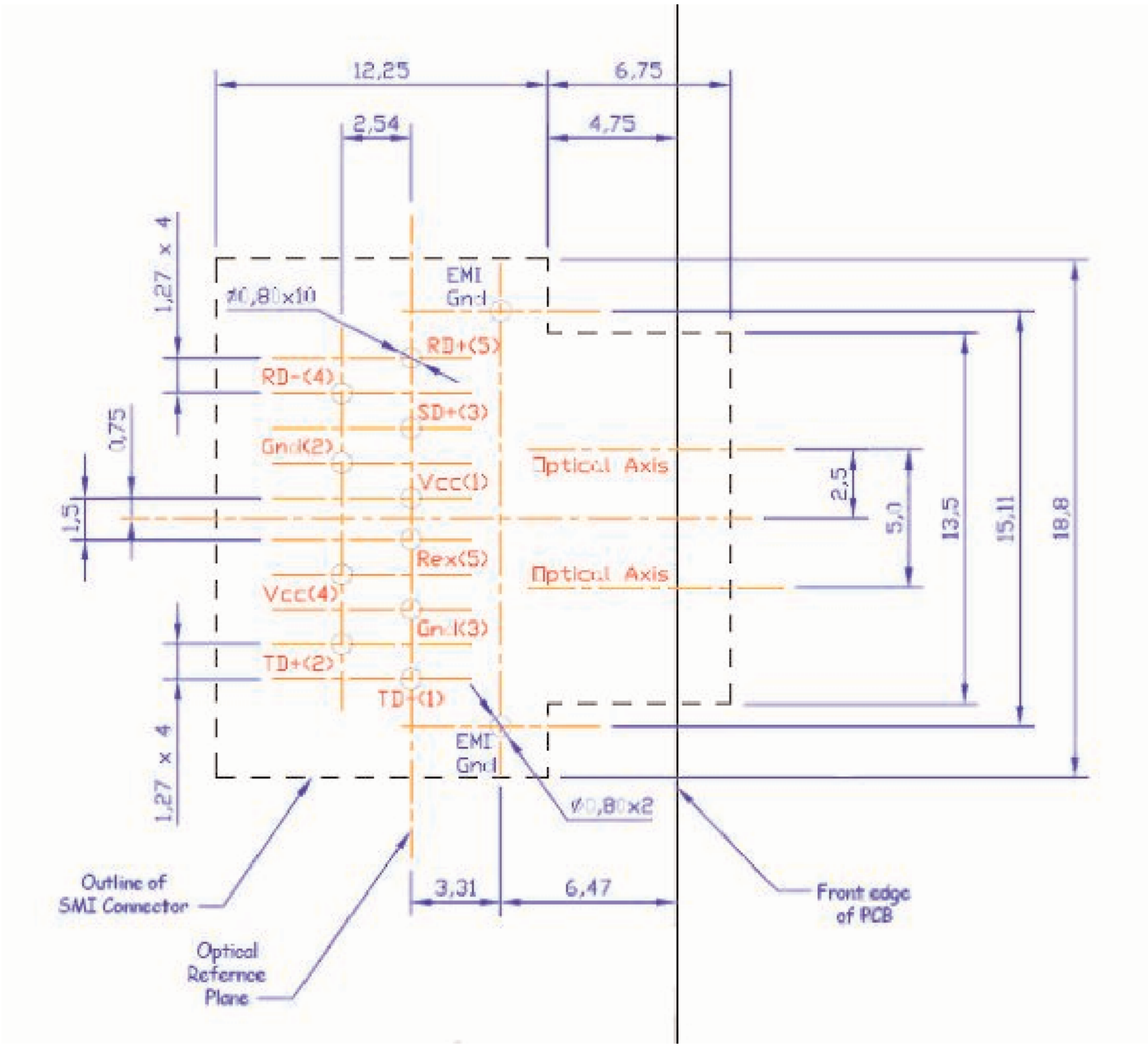

Figure 12.
Mechanical board layout for Firecomms EDL300K-120 FOT pair in an SMI or Optolock.
This is the PCB as viewed from the top of the PCB looking down.

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6.2 FOT Mechanical Dimensions

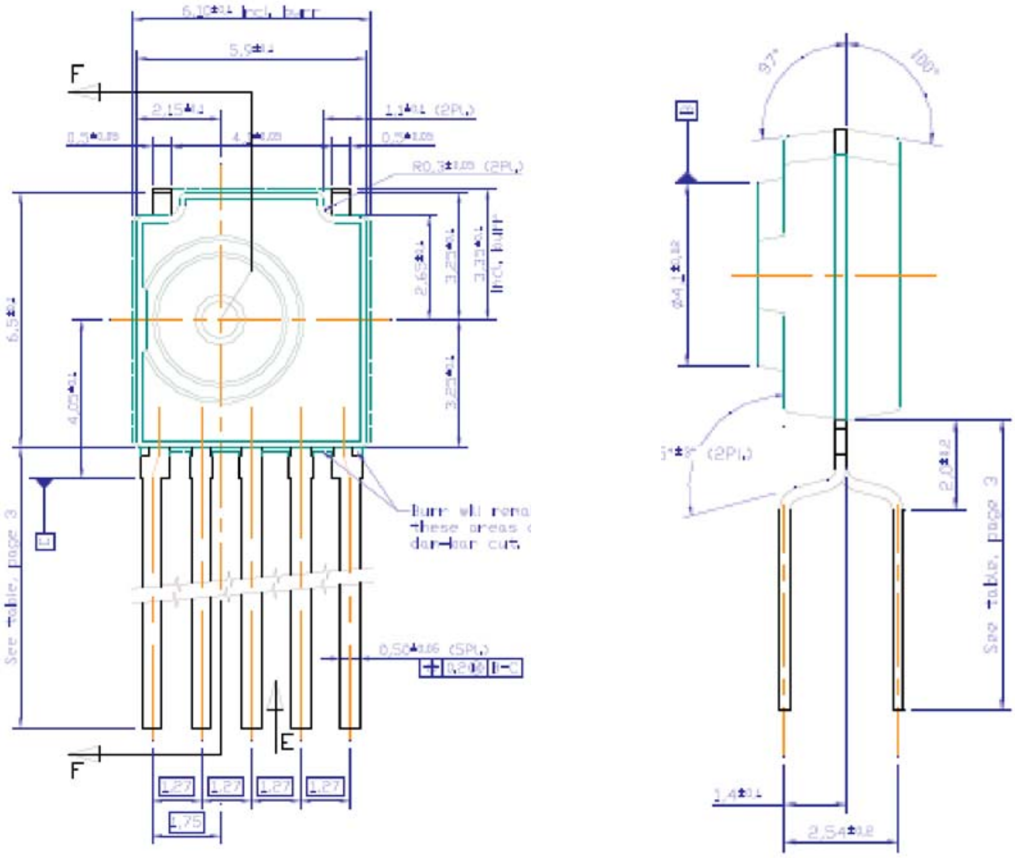

Figure 13.
Mechanical dimensions of Firecomms EDL300E-120 and EDL300D-120.

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7 SYSTEM CLOCK

PHY ICs require a system clock which for 100BaseFX is typically specified as 25 MHz ± 100 ppm. Each PHY IC will have recommendations on the optimum clock choice; it is advised that these recommendations are carefully adhered to. As a general guideline for overall optimization it is recommended that the chosen clock should meet a minimum of:

- Duty Cycle Distortion (DCD) no greater than 35% to 65%
- TTL voltage levels (VOH > 2.0V)

For 100 Mbps operation where the system is required to run at its maximum line rate for the majority of its operating time, we recommend that crystals be chosen to have a rate of 25 MHz to 25 MHz +100ppm. This can be obtained by request to the clock manufacturers. This choice minimizes the probability of a packet being dropped because of clock mismatch between PHY ICs located at opposite ends of a link. This would apply to applications supporting the media streams such as triple-play and IPTV.

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