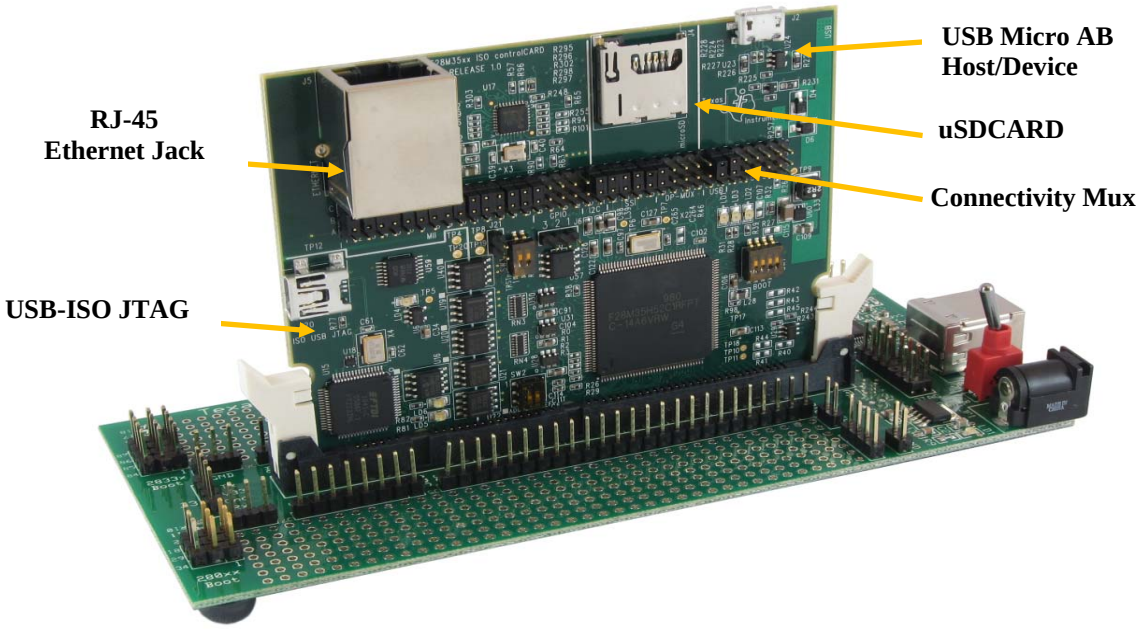
Concerto F28M35xx controlCARD



Texas Instrument's **Concerto F28M35xx controlCARD** can be used as a quick evaluation board with control, connectivity signals and ports to F28M35xx MCU.

1. The controlCARD features: Rev1.0:

- Small size – 90mm x 70mm (3.5" x 2.8")
- DIMM100 compatible cards for C2000 system application boards
- Isolated XDS100 V2 JTAG port for easy interface to Code composer 4.2.x
- Connectivity mux connector allows easy interface to connectivity ports on the top of the controlCARD and to the legacy DIMM compatible signals at the bottom
- Rev1.0 controlCARD runs on the TI controlCARD docking station. Use 5V input supply on the docking station to power 3.3V regulator on the the controlCARD
- Supports EMAC, USB host/device, SDmicro card and serial comms
- GPIO, ADC and other key signals routed to gold connector fingers
- Clamping diode protection at ADC input pins
- Isolated RS-232 communication

Note:

1. **See cautionary notes /errata for rev1.0 card BOM and isolation care in section 2.**
2. **Download ControlSUITE from www.ti.com for latest update on software, documentation and examples**

2. Exceptions on Docking station/controlCARD set up:

- The docking station JTAG port is disconnected by default. To use it you need to populate R40 to R46. The ISO JTAG port and the docking station JTAG port should not be used simultaneously.

- Rev1.0 release is an early adopter Concerto cCard kit. **Apply caution while using these board in high voltage board testing. Use external isolator if necessary.**

- CAUTION: J2 supports USB host/device connectivity. This USB port is not isolated USB port. Care should be taken while connecting external USB devices, while this card is plugged in high power application boards.
  External USB isolation buffer will be required, while debugging high power application boards/systems.

- R311 bias to EMAC Phy-U17 is removed to enable TX_ER signal. This will limit one of the RJ45 LED not to toggle during EMAC activity. A pull up on this pin will make the LED work properly.

- Connectivity Mux ABC position 5, shares the BOOT mode pin GPIO43. For reliable read of BOOT pin GPIO43 (SW1_4) jumper on position 5 of the Connectivity Mux ABC should be removed. However, GPIO43 status does not limit boot_ to_ flash mode, both 0x7 and 0x6 value from boot Switch SW1 will enable this mode.

2.1 Errata/Caution

2.1.1 ADC input BOM change. Control card ADC inputs do not have preferred value (2.2uf). - C91, C85, C99,C117,C79,C94, C104, C100, C96,C93, C92, C110. This will impact ADC conversion and results.

Recommend these caps be replaced with 3.3nf for better ADC results. These changes have been Control cards shipped since Oct'11.

2.1.2 Rev1.0 Control cards have isolated JTAG stage. Early control card samples have (wrong cap C276 - .10uf/ 10V) values between the isolation section.

The existing caps are not recommended for good isolation. Please remove these caps while emulating in high voltage environment (>10V).

Control cards shipping from Nov'11 will not have this cap across isolation section.

2.1.3 X2.2, X2.4, C264.2, C265.2 and U32.94 make up a signal net which contains a clean ground for maintaining proper clock generation. The current controlCARD schematics have these pins additionally tied to the system ground. This is incorrect. Instead, only the above terminals should be tied together as stated in the device datasheet.

3. Hardware package

Each controlCARD includes a "*Hardware Developer's Package,*" and a set of "*soft collateral*" files which makes deploying this technology very easy.
These files include:

- Schematics
- Bill of materials (BOM)
- Gerber files

4. References

Isolated JTAG – ISO JTAG:

J20	USB_A connector is intended for XDS100V2 JTAG emulation and SCI communication through dedicated FTDI logic

Connectivity ports/Jumpers:

J2	USB micro AB connector supports USB 2.0 host/device
J4	SD Micro card adaptor through SPI port
J5	Ethernet port
J6	EEPROM write protect. Jumpers on pins 1-2 connects WP pin to 3.3V (protected). Jumpers on pins 2-3 connects WP pin to GND (not protected)
J21	Default unconnected. Connected if isolated EMU0 signal is needed for JTAG.

LEDs:

LD1	Turns on when controlCARD is powered on (Green)
LD2	Controlled by PC6_GPIO71 (Red)
LD3	Controlled by PC7_GPIO70 (Red)
LD4	Power for ISO JTAG logic (Green)
LD5	UART/SCI Rx activity indicator
LD6	UART/SCI Tx activity indicator

SW1: Controls the boot mode options of the F28M35xx device

M3 boot Mode	C28x boot Mode	PG2_GPIO34	PG3_GPIO35	PG7_GPIO47	PF3_GPIO43
Boot from Parallel IOs	Boot from Master	X	0	0	0
Boot from M3 RAM	Boot from M3	X	0	0	1
Boot from M3 serial peripherals (UART0/SSI0/I2C0)	Boot from M3	X	0	1	0
Boot from M3 CAN	Boot from M3	X	0	1	1
Boot from M3 Ethernet	Boot from M3	X	1	0	0
Boot from M3 Flash	Boot from Master	X	1	1	1

SW2: ADC VREF control

The ADC reference will range from 0 to 3.3V by default. However, if the ADC in the ADC registers is configured to use external limits, the ADC will convert its full range of resolution from VREF-LO to VREF-HI.

Position1 - Controls VREF-HI, the value that the ratio-metric ADC will convert as the maximum 12-bit value, which is 0x0FFF. In the downward position, VREF-HI will be connected to 3.3V. In the upward position, VREF-HI will be connected to pin 66 of the DIMM100-socket. This would allow a connecting board to control the ADC VREF-HI value. This extends VREF-HI connections to both the ADCs on the F28M35xx device.

Position 2 - Controls VREF-LO, the value that the ratio-metric ADC will convert as the minimum 12-bit value, which is 0x0000. In the downward position, VREF-LO will be connected to 0V. In the upward position, VREF-LO will be connected to pin 16 of the DIMM100-socket. This would allow a connecting board to control the ADC-VREFLO value. This extends VREF-LO connections to both the ADCs on the F28M35xx device.

SW3: TRST/ ISO SCI communication signal enables

Position 1:

ON - TRST signal from ISO JTAG circuit will be connected to F28M35xx. Needed during JTAG debug using ISO JTAG.

OFF - TRST signal from ISO JTAG circuit will NOT be connected to F28M35xx. Needed when the application is running from flash at power up without the JTAG connections.

Position 2:

ON - RS-232 transceiver will be enabled and allow communication through a serial cable via pins 2 and 42 of the DIMM-100 socket. Putting SW3 in the "ON" position will allow the F28M35xx controlCARD to be DIMM signal compatible with the F2808, F28044, F28335, F28035 and F28027 controlCARDs. GPIO-28 will be stuck as logic high in this position.

OFF - The default option. SW5 in the "OFF" position allows GPIO-28 to be used as a GPIO. Serial communication is still possible, through the FTDI – FT2232 chip.

5. Connectivity mux connector (ABC)

F28M35xx MCU GPIO functions have been partitioned as "connectivity ports" and "control ports". DIMM 100 connector supports all the control signals/standard communication functions and maintains compatibility across all C2000 28x device families.

Connectivity mux – The mux uses physical jumpers to allow easy access to the connectivity ports on the top edge of the card (i.e. USB, Ethernet, uSDCARD) or redirects the GPIOs to the DIMM100 connector to maintain signal compatibility with the C2000 legacy applications and devices.

Unmuxed signals (pins 32 -36) should not be populated with jumpers. These are signals are intended to be used with boards that can be connected to Connectivity Mux.

6. MAC address

Concerto device Ethernet examples use a fixed TI's MAC address: **A8-63-F2-00-00-80.** Refer to the board label for a unique TI's MAC ID assigned for each Concerto controlCARD. User applications can program a fixed MAC address in the non-volatile memory reserved for MAC address. Refer to device documentation for details.

7. F28M35xx control/connectivity signal mapping using the connectivity mux:

				F28M35xx -cCard		Revision 1.1		
	A_Row			B_Row		C_Row		
	To DIMM 100 connector			F28M35xx or DIMM		To Connectivity ports		
Connects to DIMM 100 compatible signal map	C28_GPIO49	Jumper positions	1	PH1_GPIO49	Jumper positions	M3_MII_RXD0	Ethernet	DIMM signal / Peripheral functions are active if Jumper selections are placed per the color code
	C28_GPIO30		2	PE6_GPIO30		M3_MII_MDIO		
	C28_GPIO40		3	PG0_GPIO40		M3_MII_RXD2		
	C28_GPIO41		4	PG1_GPIO41		M3_MII_RXD1		
	C28_GPIO43		5	PG3_GPIO43		M3_MII_RXDV		
	C28_GPIO51		6	PH3_GPIO51		M3_MII_TXD2		
	C28_GPIO54		7	PH6_GPIO54		M3_MII_TXEN		
	C28_GPIO55		8	PH7_GPIO55		M3_MII_TXCK		
	C28_GPIO56		9	PJ0_GPIO56		M3_MII_RXER		
	C28_GPIO58		10	PJ2_GPIO58		M3_MII_RXCK		
	C28_GPIO59		11	PJ3_GPIO59		M3_MII_MDC		
	C28_GPIO60		12	PJ4_GPIO60		M3_MII_COL		
	C28_GPIO61		13	PJ5_GPIO61		M3_MII_CRS		
	C28_GPIO62		14	PJ6_GPIO62		M3_MII_PHYINTRn		
	C28_GPIO63		15	PJ7_GPIO63		M3_MII_PHYRSTn		
	C28_GPIO32		16	PF0_GPIO32		M3_PF0/CAN1RX	CAN0/1	
	C28_GPIO33		17	PF1_GPIO33		M3_PF1/CAN1TX		
	C28_GPIO6		18	PA6_GPIO6		M3_PA6/CAN0RX		
	C28_GPIO31		19	PE7_GPIO31		M3_PE7/CAN0TX		
	C28_GPIO14		20	PB6_GPIO14		M3_I2C0SDA	I2C	
	C28_GPIO15		21	PB7_GPIO15		M3_I2C0SCL		
	C28_GPIO16		22	PD0_GPIO16		M3_SSIOTX	SSI	
	C28_GPIO17		23	PD1_GPIO17		M3_SSIORX		
	C28_GPIO18		24	PD2_GPIO18		M3_SSIOClk		
	C28_GPIO19		25	PD3_GPIO19		M3_SSIOFss		
	C28_GPIO54		26	DIMM_pin 20		C28_GPIO60	DIMM IO options	
	C28_GPIO55		27	DIMM_pin 70		C28_GPIO61		
	C28_GPIO56		28	DIMM_pin 22		C28_GPIO62		
	C28_GPIO57		29	DIMM_pin 72		C28_GPIO63		
	C28_GPIO57		30	PJ1_GPIO57		M3_USB0FLT	USB	
	C28_GPIO42		31	PG2_GPIO42		M3_USB0DM		
Un_muxed signals	PC4_GPIO68/MII_RXD3	Do not populate	32	PG5_GPIO45/USB0DP	Do not populate	PF5_GPIO37/MII_RXD3	Un_muxed signals	
	PH4_GPIO52/MII_TXD1		33	PF6_GPIO38/USB0VBUS		PH5_GPIO53/MII_TXD0		
	PG6_GPIO46/USB0ID		34	PC5_GPIO69/USB0EPEN		PG7_GPIO47/MII_TXER		
	NC		35	GND		NC		
	3.3V		36	NC		5V		