TEXAS INSTRUMENTS

TPD1S514

SLVSCF6 – February 14, 2014

TPD1S514 USB CHARGER Over Voltage, Surge and ESD Protection FOR V_{BUS} PIN

1 Features

- Input DC Voltage Protection at VBUS_CON up to 30V
- Low RON nFET Switch Supports Host and Charging Mode
- Withstands up to 100V Open Circuit Surge Voltage (per IEC61000-4-5)
- Internal 20 ms startup delay
- Internal 3.4 ms soft-start delay
- USB Inrush current compliant
- ESD Performance VBUS_CON
  - ±15 kV Contact Discharge (IEC 61000-4-2)
  - ±15 kV Air Gap Discharge (IEC 61000-4-2)
- Integrated Input Enable
- Precision OVP from 5.9V to 6V
- Thermal shutdown feature
- WCSP Package

2 Applications

- Cell Phones
- Tablets
- eBooks
- Portable Media Players
- 5V Power Rails

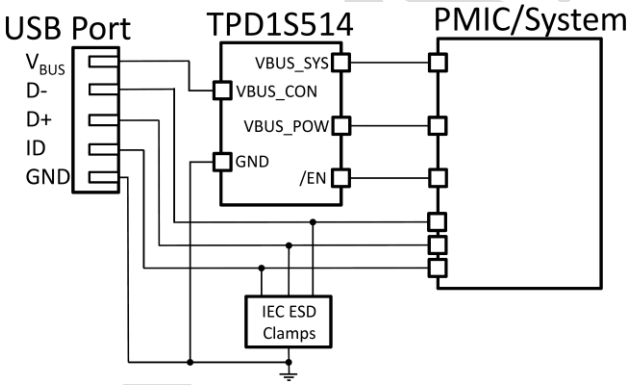
3 Description

The TPD1S514 is a single-chip solution for USB connector's VBUS line protection. The bi-directional nFET switch ensures safe current flow in both charging and host mode while protecting the internal system circuits from any over-voltage conditions at the V_{BUS_CON} pin. On the V_{BUS_CON} pin, this device can handle over-voltage protection up to 30V. After the /EN pin toggles low, the TPD1S514 waits 20 ms before turning ON the nFET through a soft start delay.

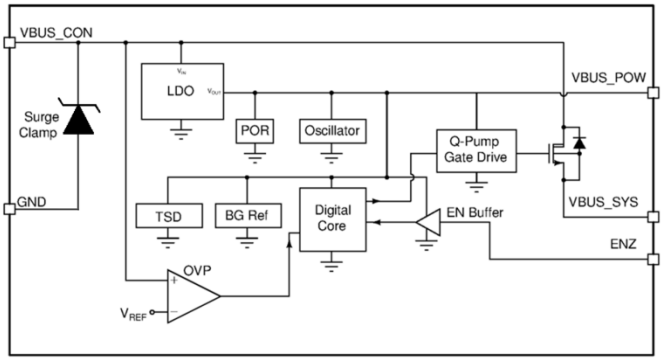
Device Information

ORDER NUMBER	PACKAGE (PIN)	BODY SIZE
TPD1S514YZ	WCSP–YZ (12)	1.288 mm x 1.988 mm

4 Simplified Schematics



TPD1S514 Circuit Protection Scheme



TPD1S514 Block Diagram

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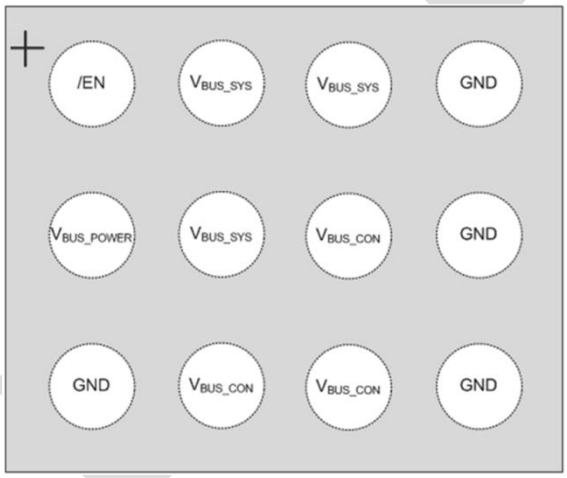
5 Revision History

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	WCSP – YZ (0.4 mm pitch)	Tape and reel	TPD1S514YZR	TBD

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

6 Terminal Configuration and Functions



12 Pin YZ Package
1.288 mm x 1.988 mm
(Top View)

Terminal Functions

Terminal		Type	Description
Name	No.		
/EN	A1	I	Enable Active-Low Input. Drive /EN low to enable the switch. Drive /EN high to disable the switch.
V_{BUS_POWER}	B1	O	5V Power source controlled by V_{BUS_CON}
V_{BUS_SYS}	A2, A3, B2	IO	Connect to internal V_{BUS} plane
V_{BUS_CON}	B3, C2, C3	IO	Connect to USB connector V_{BUS_CON}; IEC61000-4-2 ESD protection IEC61000-4-5 Surge protection
GND	A4, B4, C1, C4	G	Connect to PCB ground plane

7 Specifications

7.1 Absolute Maximum Ratings (1)

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{BUS_CON}	Supply voltage from USB connector		-0.5	30	V
V_{BUS_SYS}	Internal Supply DC voltage Rail on the PCB		-0.5	20	
IBUS	Continuous input current on V_{BUS_CON} pin(2)			3.5	A
IOUT	Continuous output current on V_{BUS_CON} pin(2)			3.5	A
I_{PEAK}	Peak Input and Output Current on V_{BUS_CON}, V_{BUS_SYS} pin (10 ms)			8	A
I_{DIODE}	Continuous forward current through the FET body diode			1	A
V_{POWER}	Continuous Voltage at V_{BUS_POWER}			5.9	V
V_{EN}	Voltage on Input pin (/EN)			7	V
T_{STG}	Storage temperature range		–65	150	°C
T_A	Operating Free Air Temperature		-40	85	°C
IEC 61000-4-2 Contact Discharge		V_{BUS_CON} pin		±15	kV
IEC 61000-4-2 Air-gap Discharge		V_{BUS_CON} pin		±15	kV
IEC 61000-4-5 Peak Pulse Current (t_p = 8/20µs)		V_{BUS_CON} pin		TBD	A
IEC 61000-4-5 Peak Pulse Power (t_p = 8/20µs)		V_{BUS_CON} pin		TBD	W
IEC 61000-4-5 Open circuit voltage (t_p = 1.2/50 µs)		V_{BUS_CON} pin		100	V
C_{LOAD}	Output load capacitance	V_{BUS_SYS} pin	0.1	100	µF
C_{CON}	Input capacitance	V_{BUS_CON} pin	0.1	50	µF
C_{POW}	V_{BUS_POWER} Capacitance	V_{BUS_POWER} pin	0.1	4.7	µF

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Thermal limits and power dissipation limits must be observed.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
Storage temperature		-65	150	Cº

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{BUS_CON}	Supply voltage from USB connector				5.9	V
V_{BUS_SYS}	Internal Supply DC voltage Rail on the PCB				5.9	V
C_{LOAD}	Output load capacitance	V_{BUS_SYS} pin		2.2		µF
C_{CON}	Input capacitance	V_{BUS_CON} pin		1		µF
C_{POWER}	Capacitance on V_{BUS_POWER}	V_{BUS_POWER} pin		1		µF
T_A	Operating free-air temperature		-40		85	ºC

7.4 Thermal Information

THERMAL METRIC(1)		YZ	UNIT
		12 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	89	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.6	
θ_{JB}	Junction-to-board thermal resistance	16.3	
ψ_{JT}	Junction-to-top characterization parameter	2.7	
ψ_{JB}	Junction-to-board characterization parameter	16.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/A	

7.5 Electrical Characteristics

7.5.1 Supply Current Consumption

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	MAX	UNIT
V_{BUS_CON} Operating Current Consumption	I_{VBUS_SLEEP}	Measured at V_{BUS_CON} pin, V_{BUS_CON} = 5V, /EN =5V	150	245	µA
V_{BUS_CON} Operating Current Consumption	I_{VBUS}	Measured at V_{BUS_CON} pin, V_{BUS_CON} = 5V, /EN =0V and no load	228	354	µA
V_{BUS_SYS} Operating Current Consumption	I_{VBUS_SYS}	Measured at V_{BUS_SYS} pin, V_{BUS_SYS} = 5V, /EN =0V and V_{BUS_CON} =Hi Z	210	373	µA
Host Mode Leakage current	I_{HOST_LEAK}	Measured at V_{BUS_SYS}. V_{BUS_CON} =Hi Z, /EN=5V, V_{BUS_SYS} =5V	90	218	µA

7.5.2 Electrical Characteristics /EN Pin

T_A = 25°C (unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage	/EN	V_{IH}		1.2		6	V
Low-level input voltage	/EN	V_{IL}		0		0.8	V
Input Leakage Current	/EN	I_{IL}	V_I = 3.3V			1	µA

7.5.3 Electrical Characteristics OVP Circuit

T_A = 25°C (unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage Protection Threshold	V_{BUS_CON}	V_{OVP_RISING}	T_A=25C	5.9	5.95	5.99	V
Hysteresis on OVP	V_{BUS_CON}	V_{HYS_OVP}	V_{BUS_CON} decreasing from 20V		100		mV
Input under voltage lockout	V_{BUS_CON}	V_{UVLO}	V_{BUS_CON} voltage rising from 0V to 5V	2.7	3.1	3.5	V
Hysteresis on UVLO	V_{BUS_CON}	V_{HYS_UVLO}	Difference between rising and falling UVLO thresholds		80		mV
Input under voltage lockout	V_{BUS_CON}	$V_{UVLO\_FALLING}$	V_{BUS_CON} voltage falling from 5V to 0V	2.6	3.0	3.4	V
V_{BUS_SYS} under voltage lockout	V_{BUS_SYS}	V_{UVLO_SYS}	V_{BUS_SYS} voltage rising from 0V to 5V	2.8	3.7	4.3	V
V_{BUS_SYS} UVLO Hysteresis	V_{BUS_SYS}	$V_{HYS\_UVLO\_SYS}$	Difference between rising and falling UVLO thresholds on V_{BUS_SYS}		730		mV
V_{BUS_SYS} under voltage lockout	V_{BUS_SYS}	$V_{UVLO\_SYS\_FALLING}$	V_{BUS_SYS} voltage falling from 7V to 5V	2.6	3.0	3.4	V

7.5.4 Thermal Shutdown Feature

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	MAX	UNIT
Thermal Shutdown	T_{SHDN}	Junction temperature	145		°C
Thermal-Shutdown Hysteresis		Junction temperature	25		°C

7.5.5 Electrical Characteristics nFET Switch

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switch ON Resistance	R_{DS_ON}	V_{BUS_CON} = 5 V, I_{OUT} = 1A, T_A = 25°C		39	50	mΩ

7.5.6 Electrical Characteristics VBUS_Power Circuit

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage on V_{BUS_POWER} during OVP	V_{CLAMP}	V_{BUS_CON}> OVP		5.0	5.5	V
Output Voltage on V_{BUS_POWER} during normal operation	V_{BUS_POWER}	V_{BUS_CON} = 5 – 15 V, I_{BUS_POWER} = 1 mA; T_A = 25°C	4.7	4.95		V
Output Current on V_{BUS_POWER}	$I_{BUS\_POWER\_MAX}$	V_{BUS_CON} = 5 – 15 V			3	mA

7.6 Timing Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB Charging Turn-ON Delay	t_{DELAY}	Measured from /EN asserted LOW to nFET begins to Turn ON, excludes soft-start time		20		ms
USB Charging rise time (Soft Start Delay)	t_{SS}	Measure V_{BUS_SYS} rise time from 10% - 90% with 1 MΩ load/ No C_{LOAD}		3.4		ms
USB Charging Turn-OFF time	t_{OFF_DELAY}	Measured from /EN asserted High to V_{BUS_SYS} falling to 10% with R_{LOAD} = 10Ω and No C_{LOAD} on V_{BUS_SYS}		5.5		µs
OVER VOLTAGE PROTECTION						
OVP Response time	$t_{OVP\_response}$	Measured from OVP Condition to FET Turn OFF (1)(2)			100	ns
Recovery Time	t_{OVP_Recov}	Measured from OVP Clear to FET Turn ON (1)(3)		20		ms

(1) Shown in TIMING DIAGRAM Plots
(2) Guaranteed by design, not production tested
(3) When measured against 8/20 µs surge per IEC61000-4-5

8 Detailed Description

8.1 Overview

The TPD1S514 provides a single-chip ESD protection, surge protection and over voltage protection solution for portable USB charging and Host interfaces. It offers over voltage protection at the V_{BUS_CON} pin up to 30V. The TPD1S514 also provides a VBUS_POWER pin that indicates to the system if a fault condition has occurred. The TPD1S514 offers ESD clamp and a Surge Clamp for V_{BUS_CON} pin, thus eliminating the need for external TVS clamp circuits in the application.

The TPD1S514 has an internal oscillator and charge pump that controls the turn-on of the internal nFET switch. The internal oscillator controls the timers that enable the charge pump. If V_{BUS_CON} is less than V_{OVP}, the internal charge pump is enabled. After a 20 ms internal delay, the charge-pump starts-up, turns on the internal nFET switch through a soft start If at any time V_{BUS_CON} rises above V_{OVP}, the nFET switch is turned OFF.

8.2 Functional Block Diagram

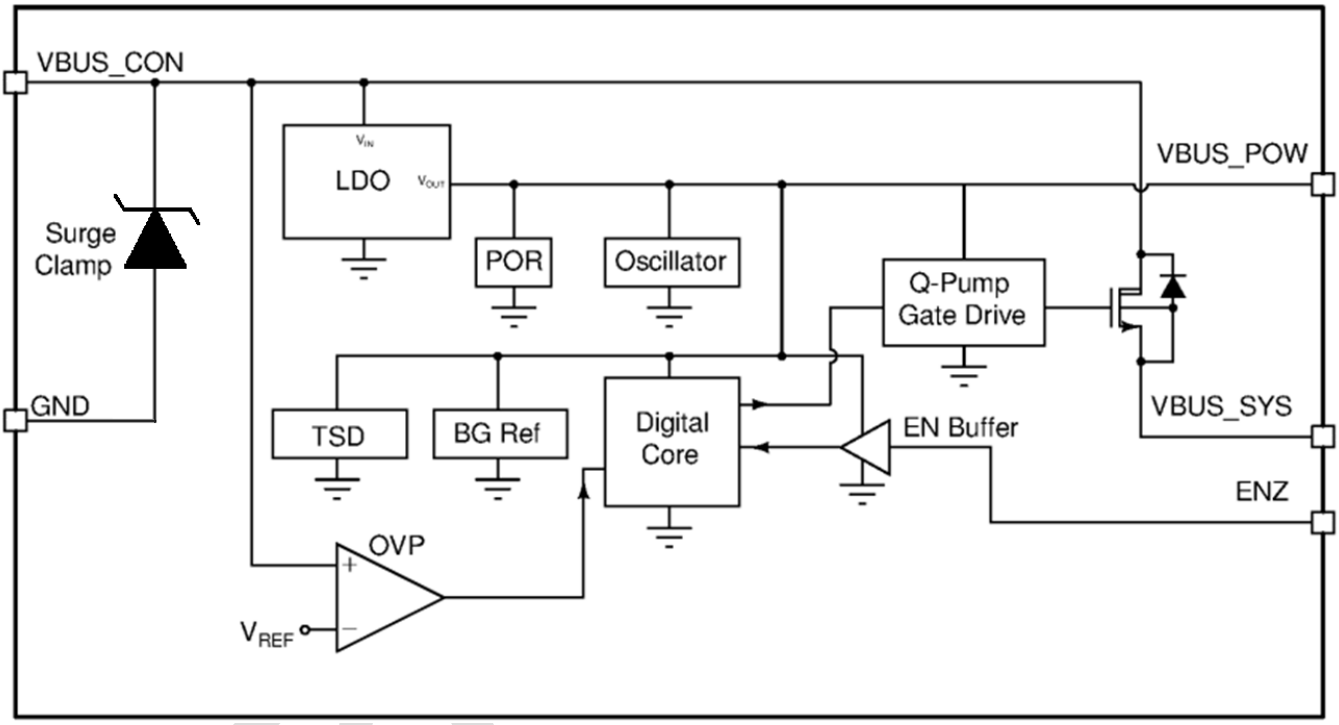


Figure 10. TPD1S514 Block Diagram

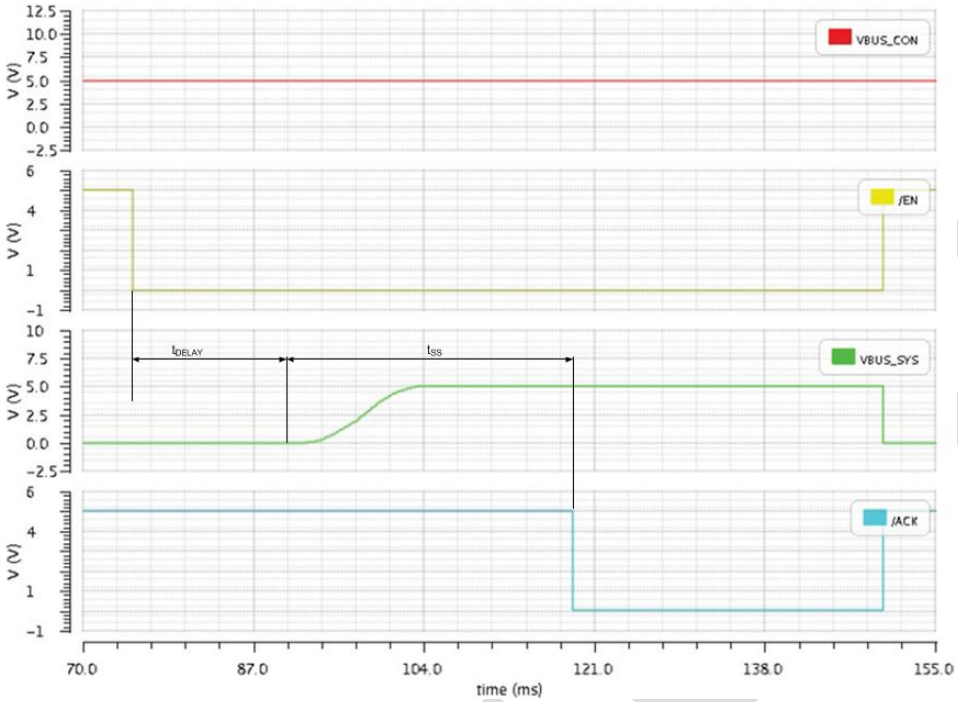
8.3 OVP OPERATION

When the V_{BUS_CON} voltage rises above V_{OVP}, the internal nFET switch is turned OFF, removing power from the system. The response is very rapid, with the FET switch turning off in less than 100 ns. The nFET is turned OFF. This pin can be pulled up through external resistors to indicate a OVP condition. When the V_{BUS_CON} voltage returns below $V_{OVP} – V_{HYS-OVP}$, the nFET switch is turned on again after the internal delay of t_{OVP_Recov}. This delay time ensures that the V_{BUS_CON} supply has stabilized before turning the switch back on. After t_{OVP_Recov}, the TPD1S514 turns ON the nFET through a soft start to ensure that the USB Inrush current compliance is met. When the OVP condition is cleared and the nFET is completely turned ON.

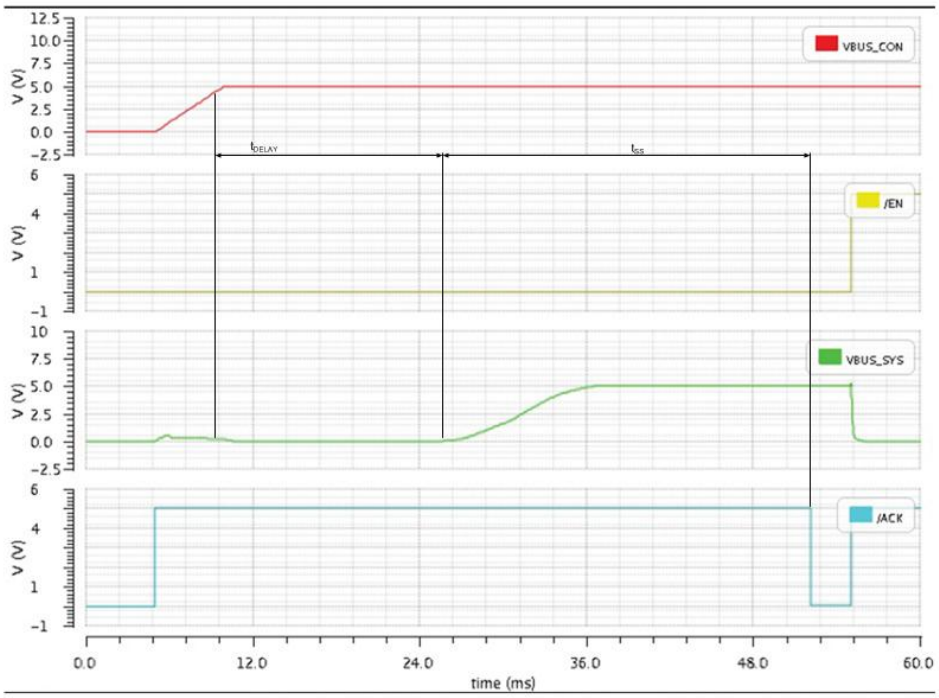
PRODUCT PREVIEW

8.4 TIMING DIAGRAMS

Enabling the Load Switch

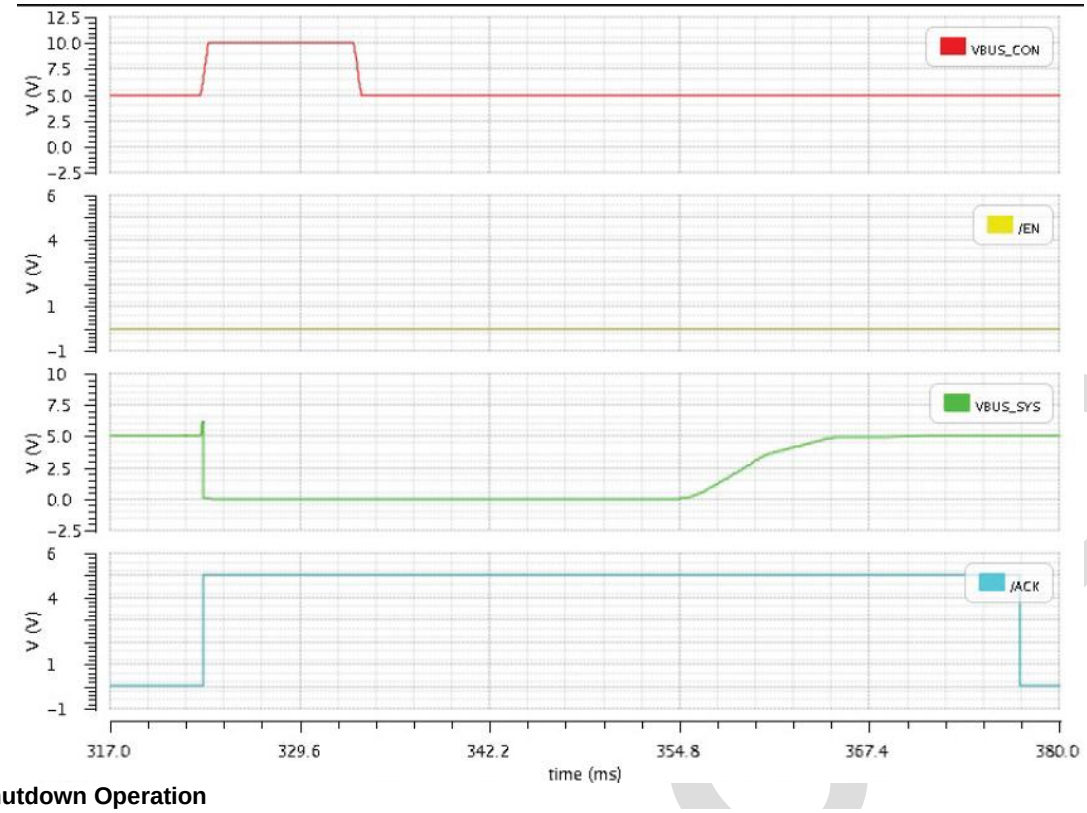


Connecting V_{BUS_CON}

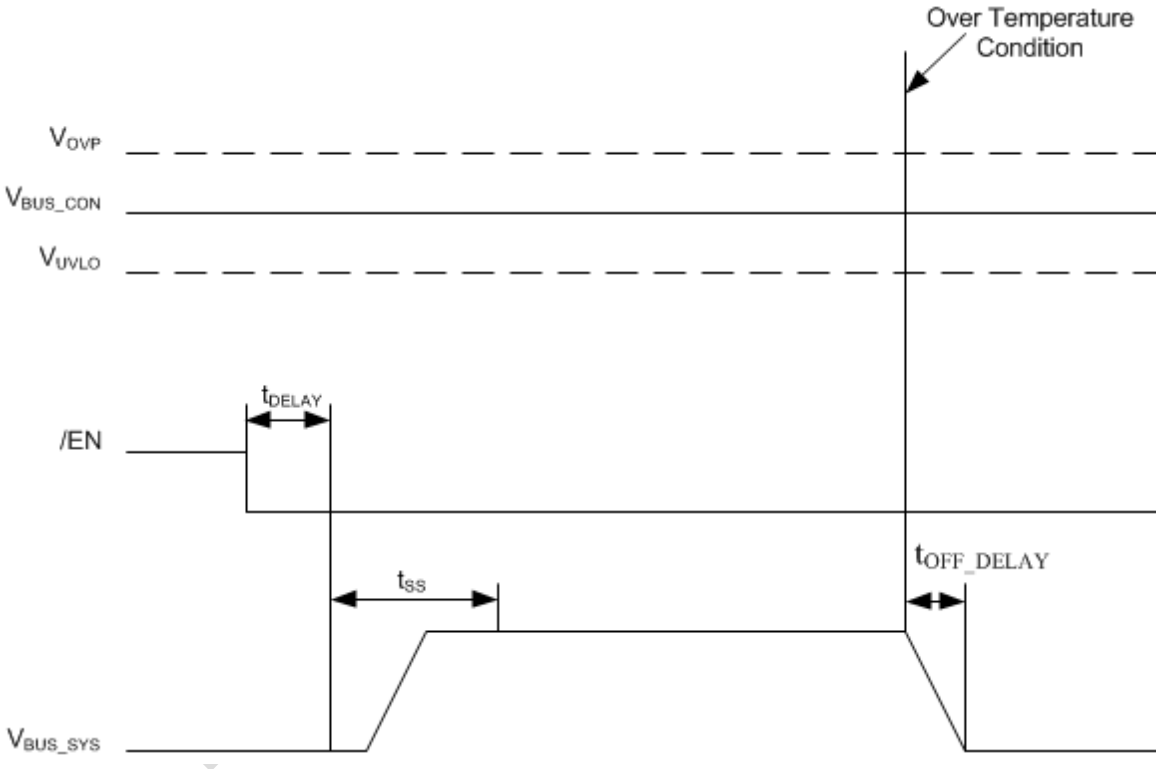


OVP Operation

PRODUCT PREVIEW



Thermal Shutdown Operation



PRODUCT PREVIEW

9 Device Documentation Support

9.1 ESDS

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.2 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from Disclosing party under this Agreement, or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

9.3 Glossary

SLYZ022 – TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.