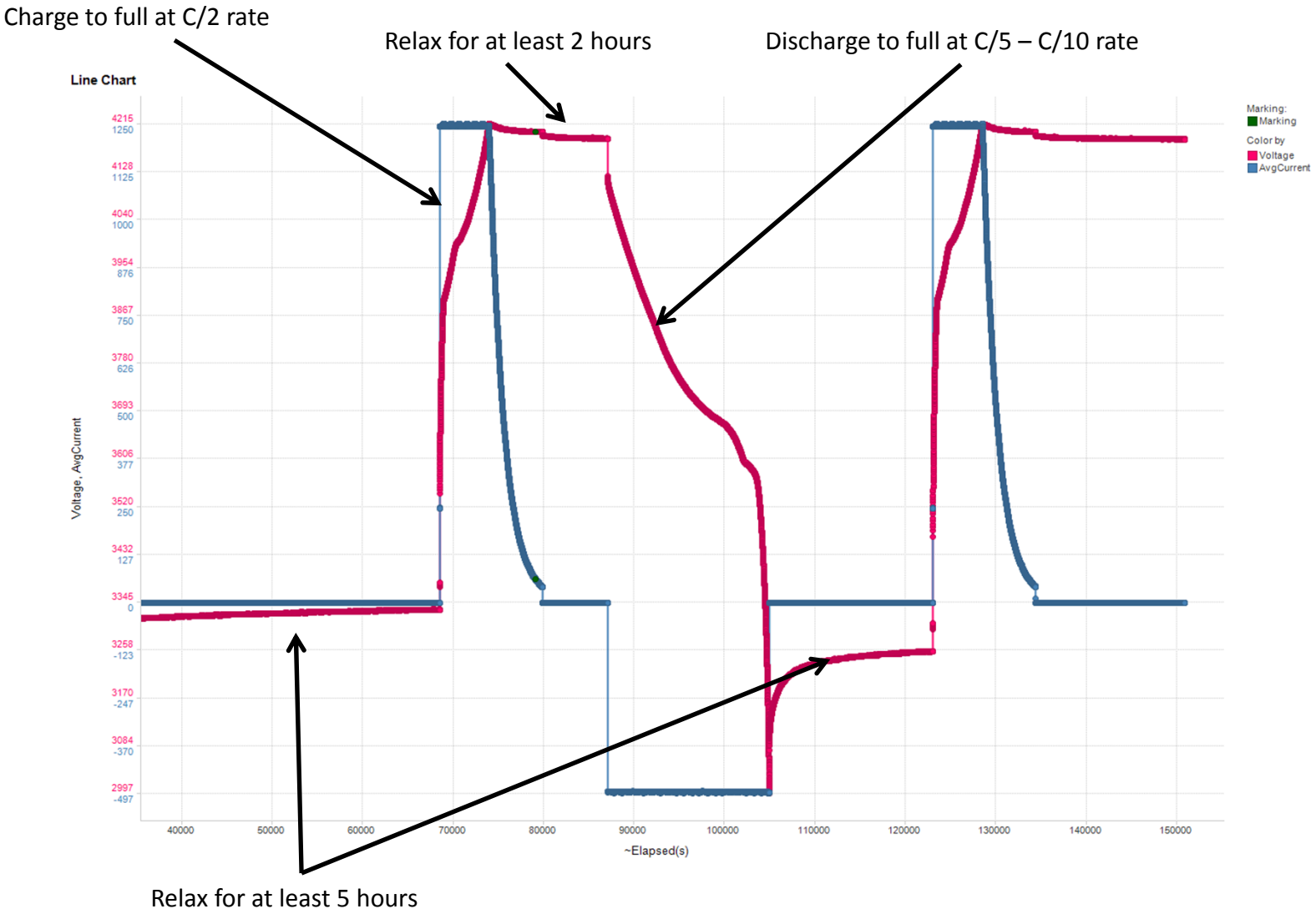
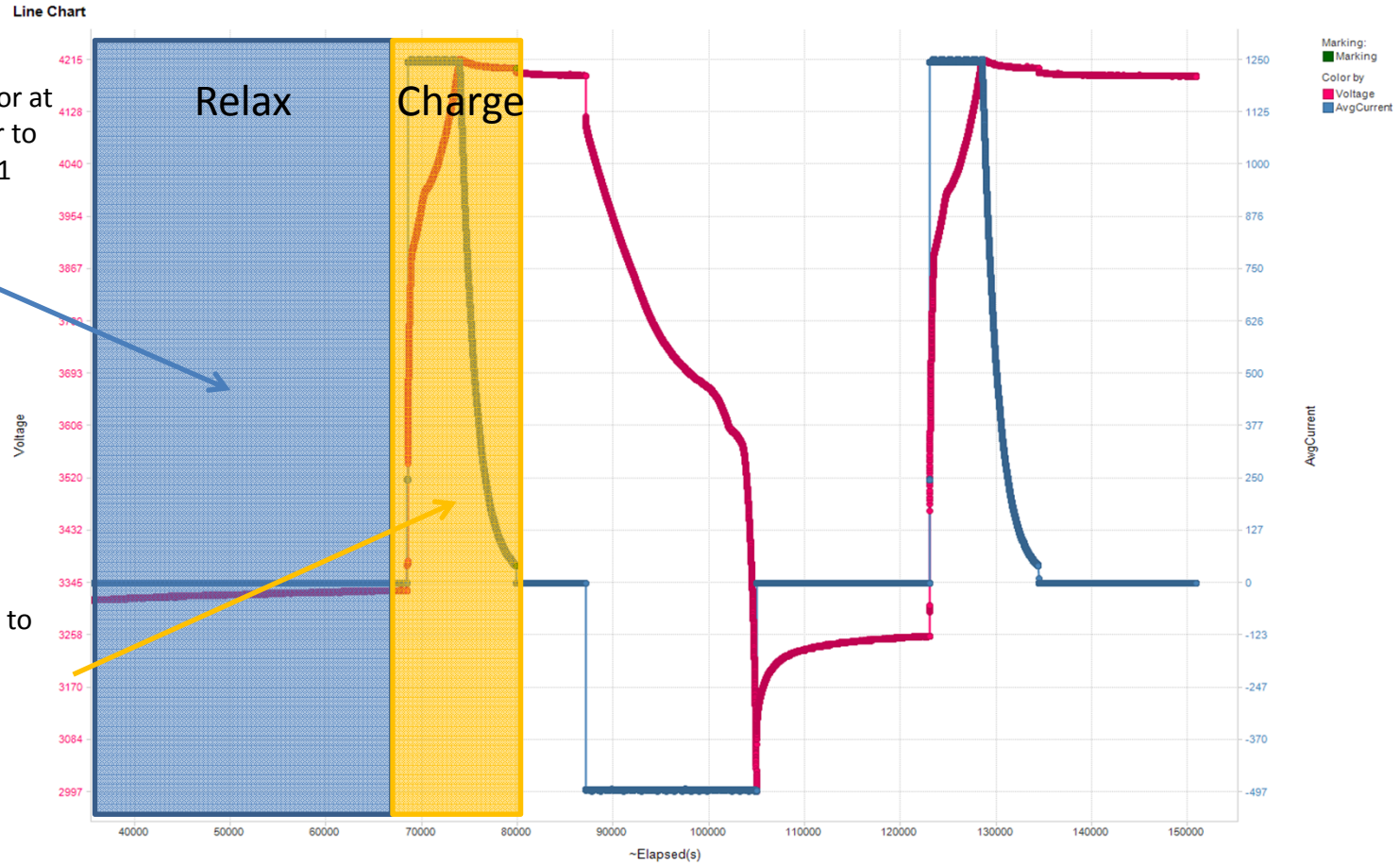
Learning Cycle Overview



Learning Cycle Break Down

Relaxation of a depleted battery for at least 5 hrs in order to reach the dV/dt < 1 uV/s condition

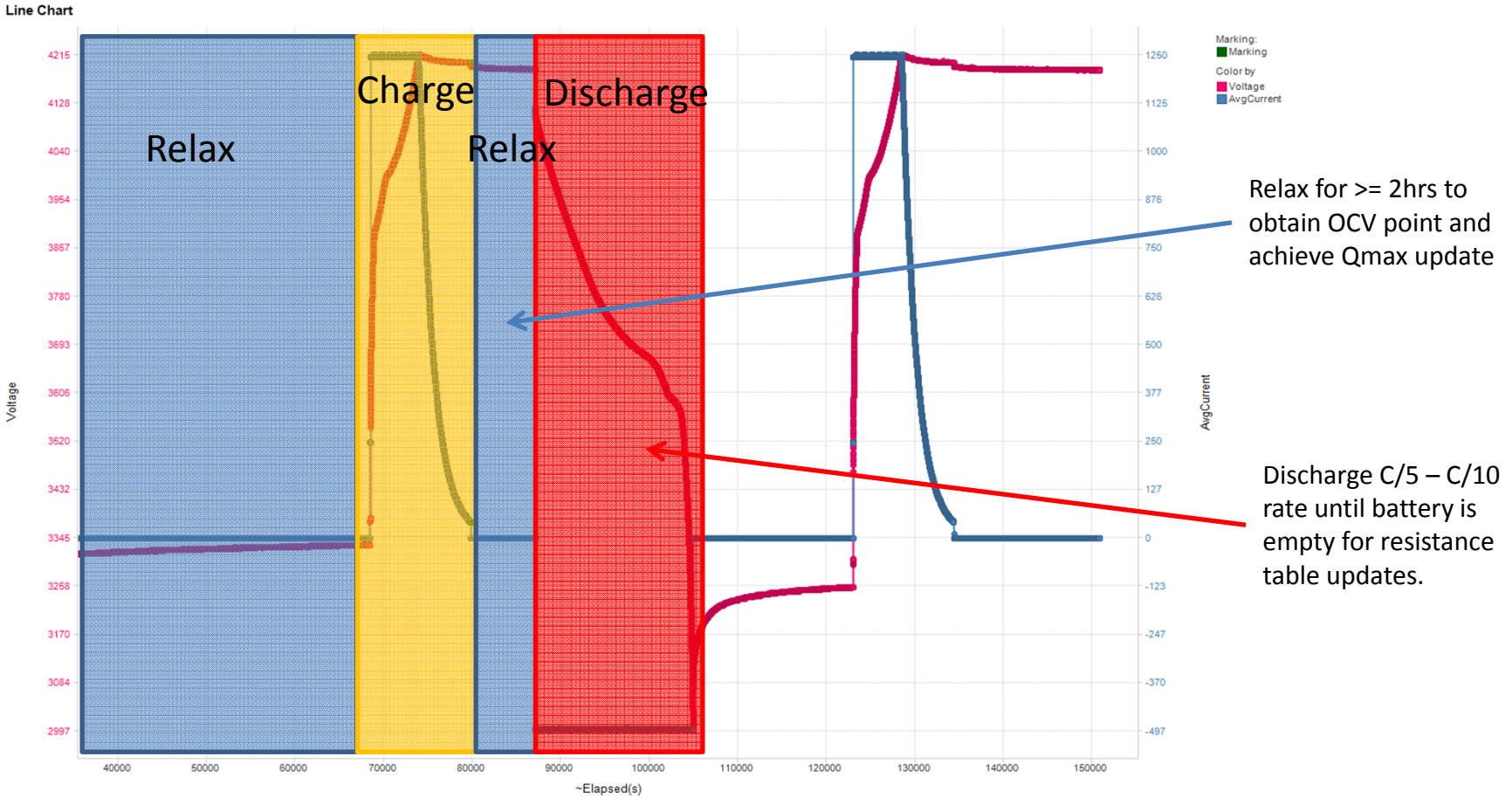
Charge the battery to full (typically C/2 constant current charge)



The Learning cycle should start with a depleted battery (typically ***Voltage()*** < 3200 mV). The learning cycle should also start out with the battery being in the relaxed state. The bq2742x will recognized a relaxed battery when dV/dt < 1 uV/s

After the dV/dt condition is reached, the bq2742x will take an open circuit voltage (OCV) reading and store the value for a future Qmax update. An indication of this would be the [RUP_DIS] bit in the Control Status register should be clear and the [VOK] bit in the Control Status register should clear. The battery can now be charged to full.

Learning Cycle Break Down

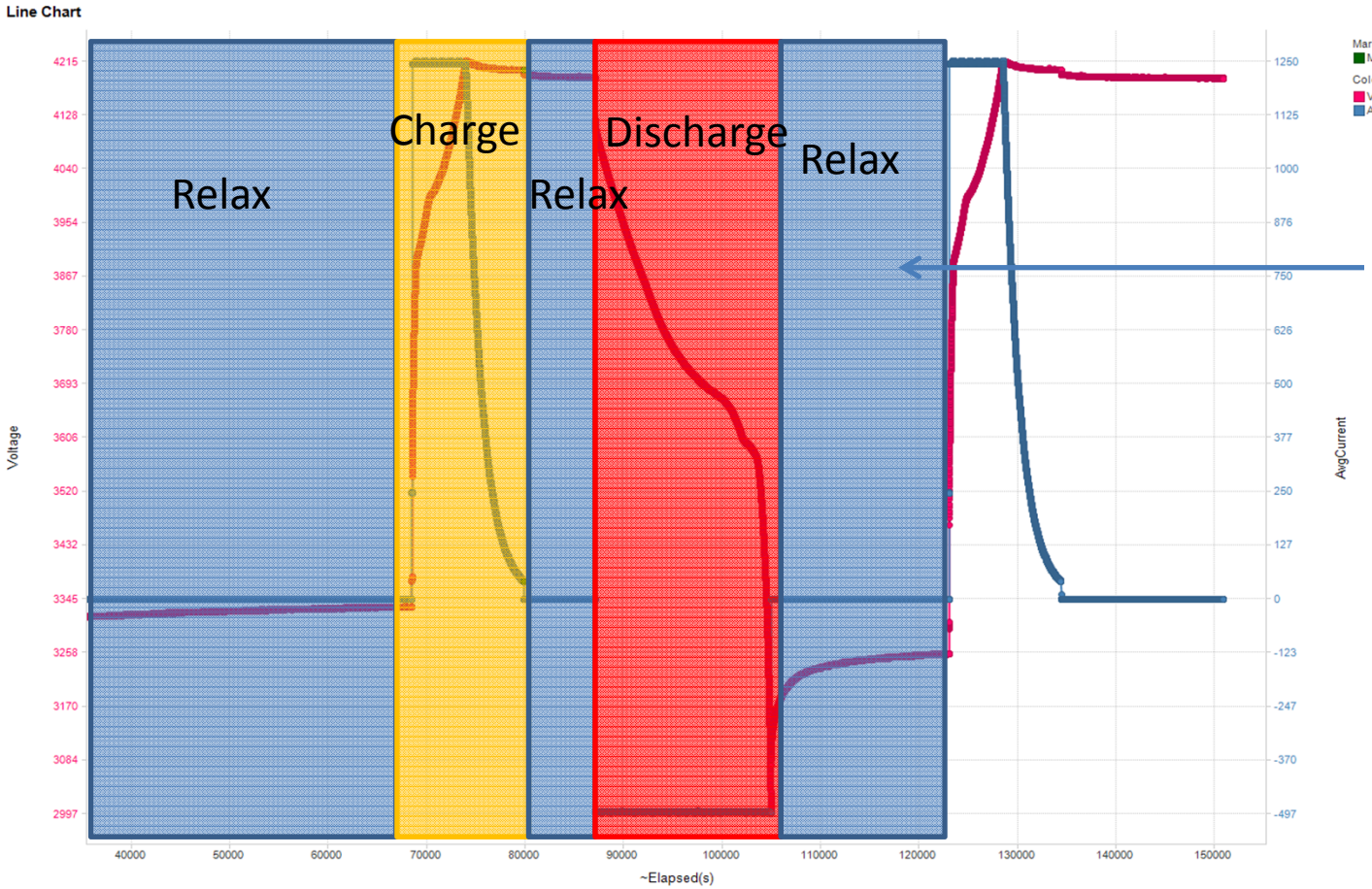


After the battery has charged to full. The [FC] bit in the Flags() register should set. The battery should now relax for at least 2 hours in order to meet the dV/dt < 1 uV/s condition for another OCV measurement.

Once the dV/dt < 1 uV/s condition has been meet the bq27425 will take anoter OCV measurement. At this point a Qmax update can be completed and the [QMAX_UP] bit in the ControlStatus() register will set.

After the Qmax update has occurred, the battery can be discharged to empty in order to allow for resistance table updates. The discharge charge should be between C/5 – C/10.

Learning Cycle Break Down



Relaxation of a depleted battery for at least 5 hrs in order to reach the dV/dt < 1

uV/s condition

During the discharge, the [RES_UP] bit in the ControlStatus() register should set. Upon exiting discharge mode the resistance table in RAM will update to the resistance table in NVM memory.

At the battery has been discharged to empty. The battery should be allowed to relax at least 5 hours in order to allow the bq2742x to obtain another OCV point. After the OCV point is taken another Qmax update will occur.

Learning Cycle