

bq76PL536 – Improving Communications

Scope:

The bq76PL536 is designed to communicate at high speed in the noisy conditions present in automotive and industrial large format battery applications. These environments are typically filled with nearby noise sources producing very fast rise-time signals and broad-spectrum RF interference. Sources include single and 3-phase inverters, DC/DC converters, motor commutation, contactor arc, and even inductively coupled noise from nearby very high current bus bars.

For starters, good layout of PCB's, use of ground planes, and high-quality, low capacitance shielded cable are required necessities of a successful system. Other factors contributing to success include minimizing cable distances, careful attention to grounding, keeping cables and PCB assemblies away from noise sources, and taking steps to reduce common-mode noise in the '536 stack.

Outlined below are some specific steps to maximize the integrity of communications with the bq76PL536 and reduce susceptibility to noise to a minimum, thereby reducing the bit-error rate to an acceptable level.

Background:

The '536 uses a current-mode interface for communications up the stack –

1. As an optimum way to eliminate the need for other forms of expensive isolation between IC's which would otherwise be required due to the high common-mode voltage between chips.
2. As a means of reducing the effects of capacitance on the signaling. The ideal current mode interface keeps the signal line (track or cable) at the same voltage potential at all times, only modulating the current. Because the voltage does not change, the driver does not need to charge or discharge the capacitance, stray or intentional. This allows for much faster signaling with minimal power dissipation.
3. As a simple, reliable, and low cost implementation technique.

Each interface signal between any two vertically stacked IC's uses ~1mA to communicate. Logic 0 is represented by a low current (<100µA), and logic 1 by a high current (~1mA). The voltage at this point is clamped at about 1V above the north IC's VSS pin. The signaling between the two IC's is referenced to the VSS of the north IC.

Although the ideal current mode interface maintains the signal path at a constant voltage, practical design considerations in the real world create small amounts of voltage fluctuation between IC's. The design compromises include cabling and associated capacitance, impedance mis-matches, driver and receiver limitations, slight process variations in batches of IC's, leakage currents, system noise (HF to

VHF range), etc. The resulting small voltage must be charged and discharged by the driver, resulting in extra signal delays as a function of cable capacitance.

The connection to the host microcontroller (μC) is a typical 4-wire Serial Peripheral Interface (SPI) link using conventional voltage mode signaling. The host-SPI link is only available at the base device where the “HOST” pin is connected to VSS. The base device translates these signals to a current mode interface, and sends them up the stack over the vertical bus (VBUS). The same four signals are used, CS (Chip-Select), SCLK (Serial Clock), SDI (Serial Data In, also called MOSI) and SDO (Serial Data Out, also commonly known as MISO).

Note that the sense of CS is inverted by the base chip, a logic 0 on the host pin asserts the interface and sends a ‘1’ up the stack, and vice-versa. When CS transitions to the asserted state, the communications interface in the base and all other chips in the stack is reset, and resynchronized. This is to prevent an IC which misses a clock or “sees” extra ones due to noisy conditions from holding the bus and preventing communications.

In the vertical stack of IC’s, it is generally easier to talk to an IC than return data from it. This is because the CS, SCLK, and SDI signals travel north with about the same delays, and maintain their timing relationships. But to receive data, the clock must travel to the destination IC, which then puts its data on the SDO pin. This signal must now travel back down the stack through all the intervening IC’s and associated delays, and arrive at the host in time for the other clock edge to latch it in. So, the total READ signal delay is $\sim 2x$ the WRITE delay, times the number of IC’s in the stack.

Recommendations – Vertical Bus:

4. Minimize cable capacitance

As previously explained, delays in the signal path are directly proportional to capacitance in the signal path. A small amount is introduced by the IC pins (nominally 5pF), but the bulk is from tracks and especially from cabling. To minimize delays, it is important to keep tracks and wiring as short as possible.

Type	Manufacturer	Part No.	Conductors	Gauge	Shield	Z _{TYP} Ω	pF/m (Cond to Cond)	pF/m (Cond to Gnd)
Round	Alpha	45198	8	22	Foil		62	112
Round	Alpha	45108	8	22	Foil/braid		62	112
Round	Tyco/Madison	122FJ00011	8	24	Foil	110	38	67
Ribbon	Tyco/Madison	1-1437373-4	16	28	Foil/braid	57 (GSG) ¹		92
Ribbon	Tyco/Madison	1-57040-6	16	28	None ²	135 (GSG) ¹	43	

Notes: 1) Ground-Signal-Ground
2) included for comparison, not recommended

5. Use shielded cable

While shielding increases the amount of capacitance exhibited by cable, it is critical to keep as much noise as possible out of the signal path. High quality shielding is recommended for all applications where stack size is greater than a few devices or cable runs exceed 10cm.

6. Increasing the “holding” current

A small holding current of ~250nA is applied to the signal lines by the ‘536 in the logic ‘0’ state to maintain the voltage on the wire. Many designs will benefit from increasing this current to between 1 and 10µA to indirectly improve the Signal to Noise Ratio (S/N). This is easily done by adding a resistor to each signal near the first transmitter. Each IC will in turn mirror this current from input to output through the stack. This causes a modest increase in current consumption in the stack, but with the benefit of tremendously improved communications reliability.

The resistor value is calculated as follows:

Northbound signals (CS_N, SCLK_N, SDI_N, CONV_N):

$$R_{HN} = V_{NOM} / I_{HOLD}$$

Where: V_{NOM} = the average voltage applied to the resistor, equal to $V_{BRICK_{AVG}}$ of the base IC

I_{HOLD} is the desired holding current

Example:

Using $LiFe_2PO_4$ cells, $V_{NOM} = 19.8V$ ($3.3V * 6$ cells)

$$I_{HOLD} = 10\mu A$$

$$R_{HN} = 19.8 / 10.0E-6 = 1.98E+6$$

The closest standard value of 2.0M is selected for R.

Southbound signals (SDO_S, optionally FAULT_S, ALERT_S, DRDY_S):

$$R_{HS} = V_{SRC} / I_{HOLD} \text{ (the voltage source used is REG50 = 5.0V)}$$

$$R_{HS} = 5.0 / 10.0E-6 = 500E+3$$

The closest standard value of 510K is selected for R.

7. Add filtering to reduce noise

The receiver design in the bq76PL536 can allow high frequency noise to integrate and push up the node voltage slightly between bit transitions. This voltage delta must now be dealt with in charging and discharging the delta as applied to the cable and IC input capacitance. The charging and discharging of the parasitic capacitance results in slightly longer rise and fall times in the signal path, which also increases with each IC.

To partly mitigate the effects of the noise induced signal delays, a small filter capacitor C_{RF} should be added to the signal line as close to the IC as possible. Values in the range of 22pF to

100pF are good choices, with 33pF recommended. Total node capacitance should be kept below 100pF unless the SPI clock rate is lowered to compensate. Refer to Appendix A for details of the effects of this capacitor on bit rate.

While it may seem contradictory to place this small capacitor in the signal path in light of the goal to minimize capacitance, this capacitor behaves differently than the distributed or stray capacitance of the cable or tracks. The benefit of using this capacitor placed locally to remove noise outweighs the slightly negative effect on signal rate.

8. Add capacitance between ground planes

To improve common-mode rejection chip to chip, a small capacitor C_{COM} is added between ground planes. This ties the planes together and they appear as one large ground plane to AC (RF) currents. The value is non-critical in the range 3.3nF to 10nF, a typical value is 3.3nF. This capacitor is very important to reduce the RF susceptibility (EMC) of the device.

If cabling is used, the cable shield is connected directly to VSS of the north IC, and through this capacitor to the VSS plane of the south chip.

9. Series resistance in VBUS

A series resistor R_S between each north-south connection is shown on reference schematics for the bq76PL536. This resistor is used to limit currents flowing in the communications path during certain hot-plug, random cell connection order events. The resistor does not enhance communications. The resistor should be located near the transmitter pins (CS_N, SCL_N, SDI_N, CONV_N, SDO_S, FAULT_S, ALERT_S, DRDY_S).

10. Non-SPI signal improvements

The signals FAULT, ALERT, are low speed and transition rarely. These signals do not explicitly require the R_{HS} and C_{RF} parts, but they may be included for completeness and symmetry in the design.

The signal DRDY is a high speed signal, but not used in all designs (systems which employ a 1ms tick in their RTOS can simply request a conversion on one tick, and read it on the next). If your design uses the DRDY signal to indicate a conversion is complete, then R_{HS} should be installed on the top IC, and C_{RF} should be installed on each IC except the topmost one.

Recommendations – Host Connections:

1. Adding series R to reduce reflections

Often an ISO7241 or similar buffer / driver/ isolator IC will be installed between the base '536 and the host microcontroller (μC). These types of IC's have very fast drivers with high edge rates. The fast signals can lead to unwanted reflections may cause multiple edges on the signal lines to the '536. The multiple edges in turn may lead to bus errors caused by extra clocks or false communications interface resets inside the device.

To reduce this unwanted behavior, a series resistor can be added to the link between the ISO part and the '536 IC. The resistor takes advantage of the track and chip capacitance to form a small RC low-pass filter. In rare cases, a small capacitor (10-50pF) may also be required near the receiving device. The resistor is located close to the transmitter, and is typically a value between 75 and 1K ohms, 100 is recommended as a nominal value.

2. Adding a ferrite bead or inductor to reduce EMC

Adding a small ferrite bead or inductor to the signal lines near the '536 will further reduce the susceptibility to high-frequency RF fields. Recommended part values are shown in reference schematics available from TI. This is usually added in addition to the series resistor described above.

3. Improving common-mode rejection

Capacitors linking ground planes were added in the section above to remove differences in AC potentials between IC's, and tie all of them to a common reference point at VSS_{BASE} . This same technique can be extended to remove sources of large common-mode dv/dt shifts due to stray capacitance between the source of the common-mode and the stack. This situation is artificially created when the battery VSS is separated from the communications source by galvanic isolator chips and isolated DC/DC converters, such that the two sides do not share a common reference point. This is an important safety consideration, but is hard on single-ended communications.

The effect of this can be reduced by adding an AC-coupled common connection point. In the accompanying diagram shown in Appendix B, this is composed of two series capacitors and series resistors. Generally, the values are not critical and can be selected empirically. The capacitor provides the AC connection; the R is added to lower the Q of the resonant loop created by the transformer L, parasitic C and added capacitors. Two series caps are used to reduce shock hazard in the event one cap fails. The decision to add this circuit is left to the design engineer, many designs will function correctly without it.

Troubleshooting:

CAUTION

Dangerous High-Voltages are present in the stack and at the device which may cause injury or death.
Follow appropriate safety precautions for working with high voltage circuits.

1. Use the TI supplied Windows Graphical User Interface (WinGUI)

The TI interface should successfully connect to your standard SPI port. This provides a known good software environment to start from. Make sure the checkbox “Hdwe IO” is unchecked, as the hardware supporting this feature is unavailable in most user designs, and software IO will always work. Use the lowest bit rate setting available (125kbs) as a starting point.

2. How many IC are visible?

Did the WinGUI (or your firmware) find the expected number of IC’s? This indicates that communications are working, at least in part.

3. Writes are OK, but reads are corrupt?

Tack a low-current LED and ~1.5K current limit resistor between the GPIO pin and REG50. Can you reliably toggle the LED? If so, northbound communications are OK, and the CS, SCLK, and SDI lines are basically working.

Find out how far up the stack you can do this. Use BROADCAST commands to write to all devices simultaneously.

4. The scope shows reads beginning, but data suddenly transitions to all 0 from SDO pin - why?

This is often caused by noise on the CS path causing the internal communications engine to reset unexpectedly. When this occurs, the engine is no longer addressed, and the output goes to 0. Monitor this signal leading up to the problem IC, looking for noise and spikes. An isolated oscilloscope should be used, and for a given north-south link, the north VSS should be used as the “ground” reference.

Use the WinGUI communications capture tool to capture packets, and share results with TI FAE’s if necessary.

5. Data looks mostly correct, but errors occur near end of packet, especially on long packets. Data changes unexpectedly, out of sync with clock edges. Why?

This is often caused by noise on the SCLK_x line. Examine the SCLK signals, beginning with the host connection at the SCLK_H pin. Look for multiple pulses and ringing, which must be eliminated. Increasing the value of C_{RF} (which may require a reduction in bit rate) may help.

Use the WinGUI communications capture tool to capture packets, and share results with TI FAE’s if necessary.

Appendix A – Parametric Tables

Total C Loading	30pF	30pF	30pF
# Chips in stack	Round trip delay	Max clk rate	Select SCLK rate
32	2.59E-06	193.42E+03	125000
31	2.51E-06	199.60E+03	125000
30	2.43E-06	206.19E+03	125000
29	2.35E-06	213.22E+03	125000
28	2.27E-06	220.75E+03	125000
27	2.19E-06	228.83E+03	125000
26	2.11E-06	237.53E+03	125000
25	2.03E-06	246.91E+03	125000
24	1.95E-06	257.07E+03	250000
23	1.87E-06	268.10E+03	250000
22	1.79E-06	280.11E+03	250000
21	1.71E-06	293.26E+03	250000
20	1.63E-06	307.69E+03	250000
19	1.55E-06	323.62E+03	250000
18	1.47E-06	341.30E+03	250000
17	1.39E-06	361.01E+03	250000
16	1.31E-06	383.14E+03	250000
15	1.23E-06	408.16E+03	250000
14	1.15E-06	436.68E+03	250000
13	1.07E-06	469.48E+03	250000
12	985.00E-09	507.61E+03	500000
11	905.00E-09	552.49E+03	500000
10	825.00E-09	606.06E+03	500000
9	745.00E-09	671.14E+03	500000
8	665.00E-09	751.88E+03	500000
7	585.00E-09	854.70E+03	500000
6	505.00E-09	990.10E+03	500000
5	425.00E-09	1.18E+06	1000000
4	345.00E-09	1.45E+06	1000000
3	265.00E-09	1.89E+06	1000000
2	185.00E-09	2.70E+06	1000000

Table 1 – Recommended operating configuration with noise margin

Cable capacitance	70pf	30pf	none
C _{RF}	30pF	30pF	30pF
Total C Loading	100pf	60pf	30pf
# Chips in stack	SCLK max	SCLK max	SCLK max
32	Not Valid	Not Valid	125000
31	Not Valid	Not Valid	125000
30	Not Valid	Not Valid	125000
29	Not Valid	Not Valid	125000
28	Not Valid	125000	125000
27	Not Valid	125000	125000
26	Not Valid	125000	125000
25	Not Valid	125000	125000
24	Not Valid	125000	250000
23	Not Valid	125000	250000
22	Not Valid	125000	250000
21	Not Valid	125000	250000
20	Not Valid	125000	250000
19	Not Valid	125000	250000
18	125000	125000	250000
17	125000	125000	250000
16	125000	125000	250000
15	125000	125000	250000
14	125000	250000	250000
13	125000	250000	250000
12	125000	250000	500000
11	125000	250000	500000
10	125000	250000	500000
9	250000	250000	500000
8	250000	250000	500000
7	250000	500000	500000
6	250000	500000	500000
5	500000	500000	1000000
4	500000	500000	1000000
3	500000	1000000	1000000
2	1000000	1000000	1000000

Table 2 – Recommended operating configuration with additional margin for noise-induced delay.

Cable capacitance	70pf	30pf	none
C _{RF}	30pF	30pF	30pF
Total C Loading	100pf	60pf	30pf
# Chips in stack	SCLK max	SCLK max	SCLK max
32	125000	125000	250000
31	125000	125000	250000
30	125000	125000	250000
29	125000	125000	250000
28	125000	125000	250000
27	125000	125000	250000
26	125000	250000	250000
25	125000	250000	250000
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22	125000	250000	250000
21	125000	250000	250000
20	125000	250000	500000
19	125000	250000	500000
18	125000	250000	500000
17	250000	250000	500000
16	250000	250000	500000
15	250000	250000	500000
14	250000	250000	500000
13	250000	250000	500000
12	250000	500000	500000
11	250000	500000	500000
10	250000	500000	500000
9	250000	500000	1000000
8	500000	500000	1000000
7	500000	500000	1000000
6	500000	1000000	1000000
5	500000	1000000	1000000
4	1000000	1000000	1000000
3	1000000	1000000	1000000
2	1000000	1000000	1000000

Table 3 – Recommended operating configuration for quiet systems. No additional margin for noise.

Appendix B – Connection Diagrams

bq76PL536 Vertical Communications Circuit Improvements

NOTES:

R_{HN} resistors are added to the BASE device as shown to supply a larger "holding" current up the stack. Intermediate devices do not have these added hold-current resistors. Resistance value is non-critical, selected to provide 1-10uA holding current. See text to determine value. $R_{HN} = 2M$ provides ~10uA at ~20V (3.3V/cell).

C_{RF} provides enhanced noise immunity at the expense of interface speed (reduced signaling rate). Recommended values are 22-100pF (33pF). If used, C_{RF} should be added to all devices in the stack, close to the receiver.

R_S provides enhanced resistance to hot-plug issues. Values in the range 0R-1K can be used, at the expense of interface speed. These resistors do not improve communications, but are used to limit hot-plug surge currents, and are present between all devices if used. R_S is placed close to the transmitter.

If C_{RF} and R_S are used, they should be placed close to the IC transmitter or receiver as shown. The delay on each VBUS SPI signal must be be the same.

C_{COM} provides common-mode AC voltage coupling between devices. Values are not critical and 3.3nF to 10nF are recommended.

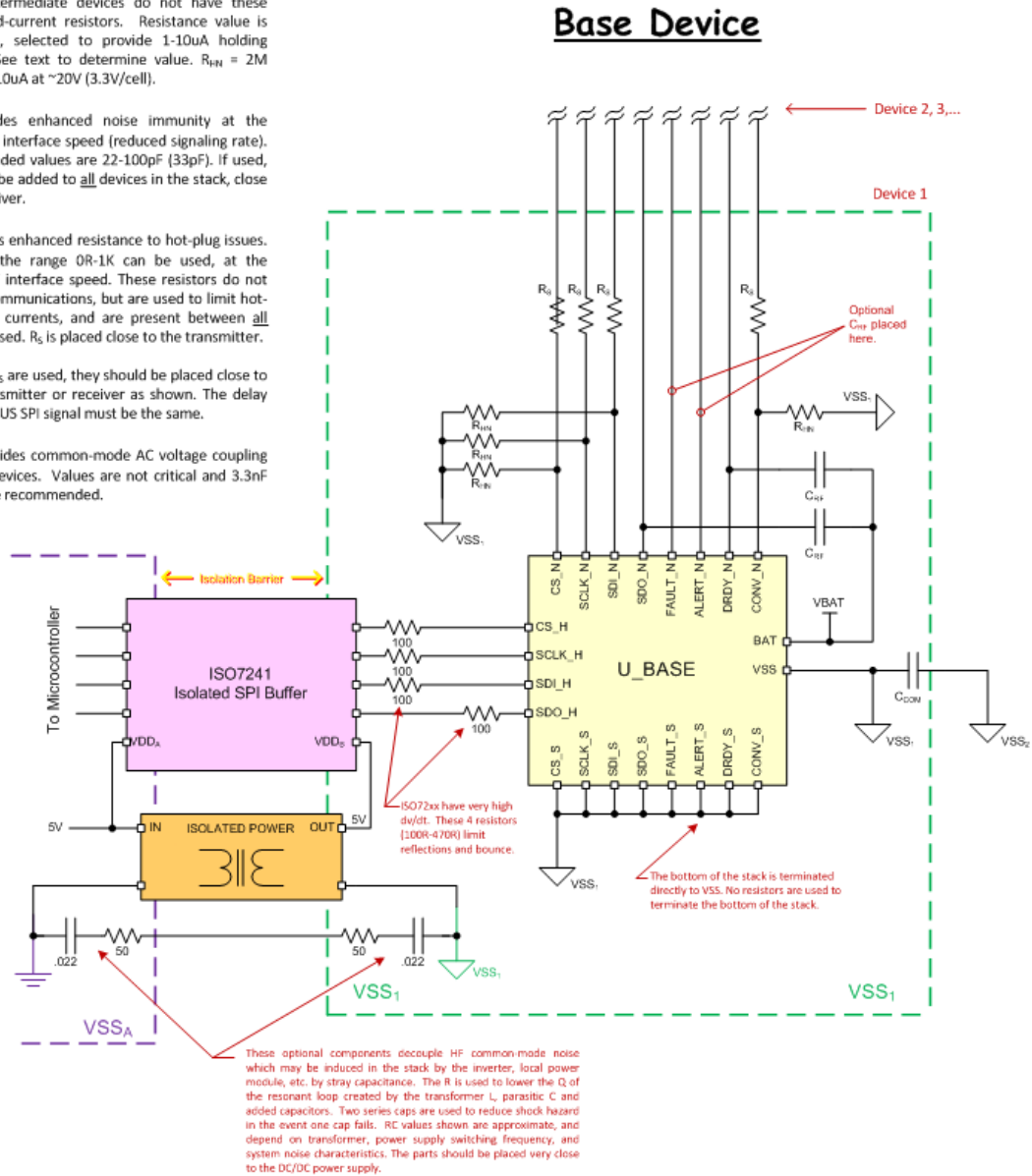


Figure 1 - Base device wiring.

All Middle Devices

NOTES:

The R_{HN} and R_{HS} resistors are not added to mid-devices.

C_{RF} provides enhanced noise immunity at the expense of interface speed (reduced signaling rate). Recommended values are 22-100pF (33pF). If used, C_{RF} should be added to all devices.

R_S provides enhanced resistance to hot-plug issues. Values in the range 0R-1K can be used, at the expense of interface speed. These resistors do not improve communications, but are used to limit hot-plug surge currents, and are present between all devices if used.

If C_{RF} and R_S are used, they should be placed close to the IC transmitter or receiver as shown. The delay on each VBUS SPI signal should be the same.

C_{COM} provides common-mode AC voltage coupling between devices. Values are not critical and 3.3nF to 10nF are recommended.

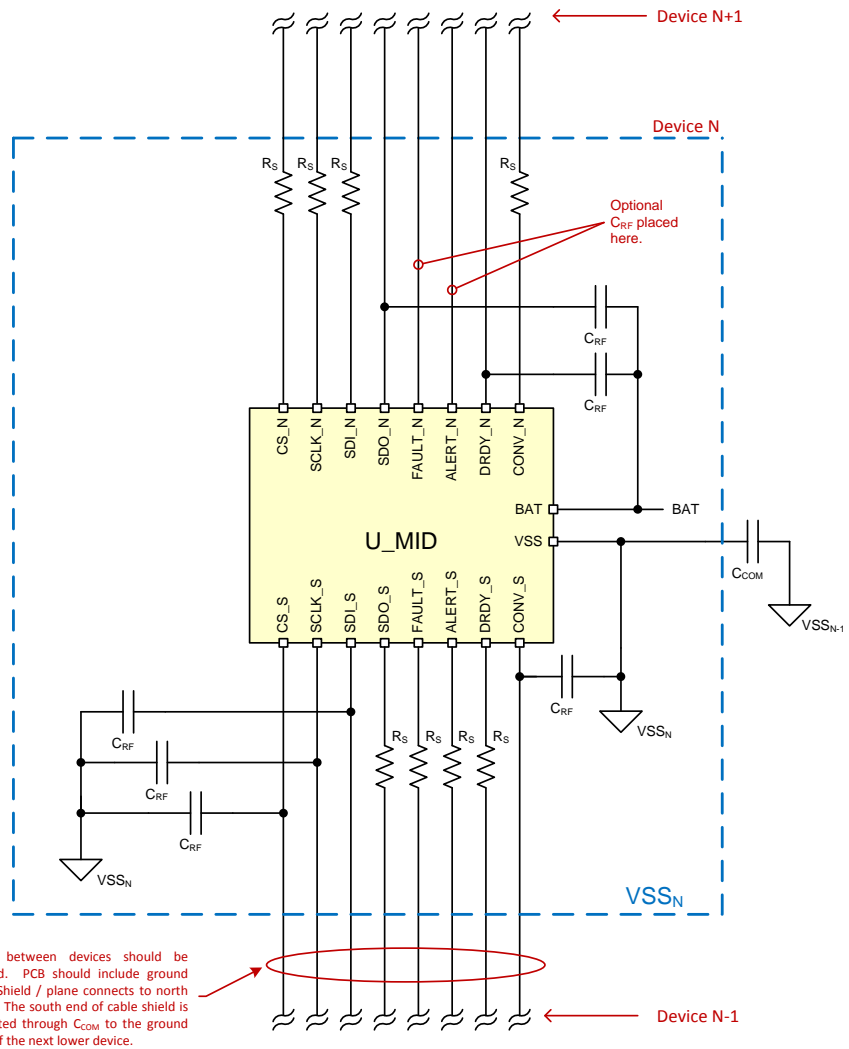


Figure 2 - Middle device wiring.

Top Device

NOTES:

The R_{HS} resistors are added to the TOP device as shown to supply a larger “holding” current down the stack. Intermediate devices do not have these added hold-current resistors. Resistance value is non-critical, selected to provide 1-10uA holding current. See text to determine value. $R_{HS} = 510K$ provides ~10uA when connected to the 5.0V REG50 supply as shown.

C_{RF} provides enhanced noise immunity at the expense of interface speed (reduced signaling rate). Recommended values are 22-100pF (33pF). If used, C_{RF} should be added to all devices.

R_S provides enhanced resistance to hot-plug issues. Values in the range 0R-1K can be used, at the expense of interface speed. These resistors do not improve communications, but are used to limit hot-plug surge currents, and are present between all devices if used.

If C_{RF} and R_S are used, they should be placed close to the IC transmitter or receiver as shown. The delay on each VBUS SPI signal should be the same.

C_{COM} provides common-mode AC voltage coupling between devices. Values are not critical and 3.3nF to 10nF are recommended.

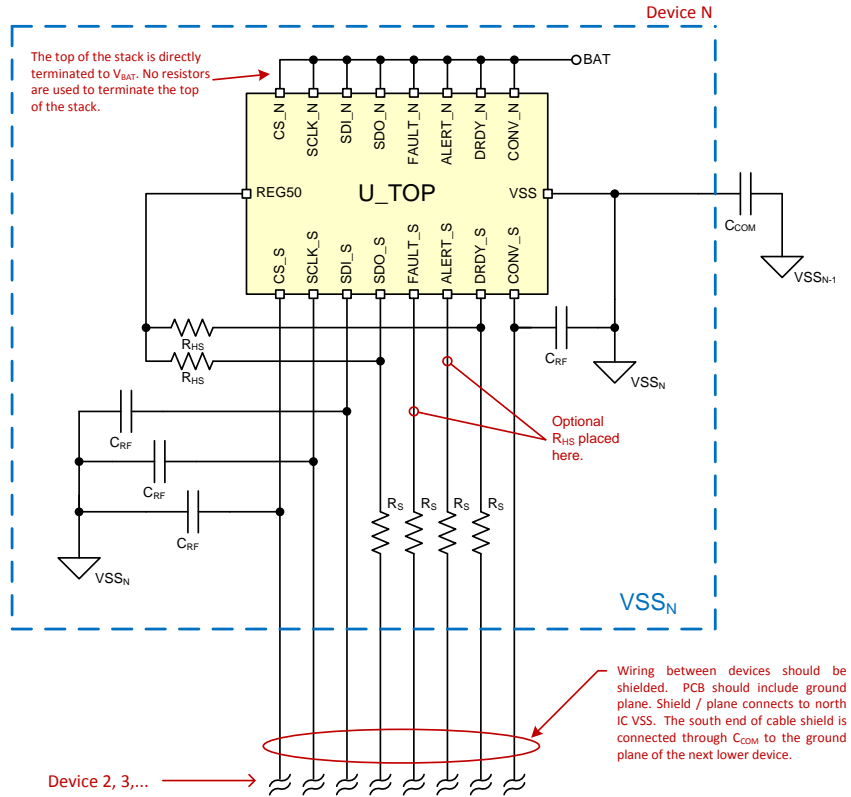


Figure 3 - Top device wiring.