bq76PL536 Vertical Communications Circuit Improvements

NOTES:

* - The asterisk designates supplemental resistors added to the TOP and BASE devices as shown to supply a larger "holding" current. Intermediate devices do not have these added hold-current resistors. Resistance value is non-critical, selected to provide 1-10uA holding current. Values shown provide ~10uA at ~20V (3.3V/cell).

C_{RF} provides enhanced noise immunity at the expense of interface speed (reduced signaling rate). Recommended values are 22-100pF (33pF). If used, C_{RF} should be added to all devices.

PCB layout with good ground plane or shielded cable should be used for all vertical communications bus signals for best performance.

R_S provides enhanced resistance to hot-plug issues. Values in the range 0R-1K can be used, at the expense of interface speed. These resistors do not improve communications, but are used to limit hot-plug surge currents, and are present between all devices if used.

If C_{RF} and R_S are used, they should be placed close to the IC transmitter or receiver as shown. The delay on each VBUS SPI signal should be the same.

C_{COM} provides common-mode AC voltage coupling between devices. Values are not critical and 3.3nF to 10nF are recommended.
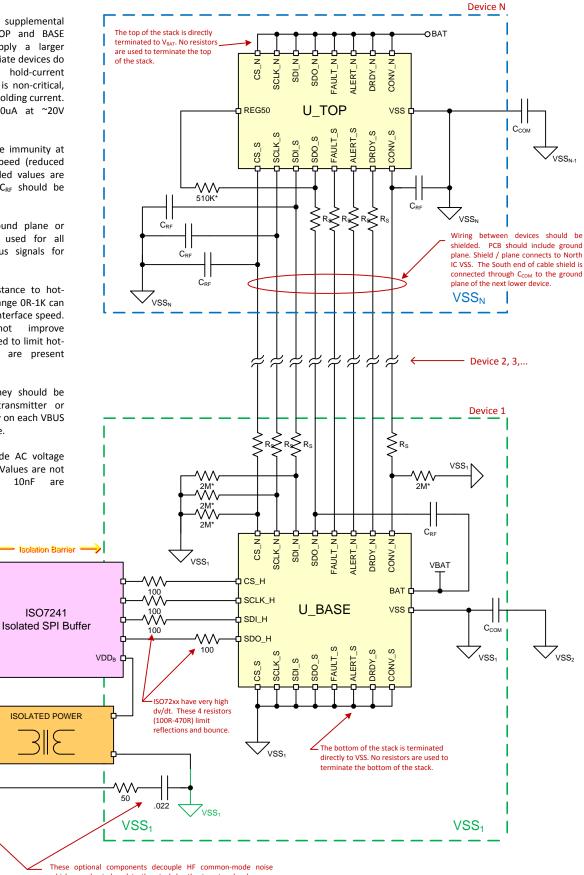
The top of the stack is directly terminated to V_{BAT}. No resistors are used to terminate the top of the stack.

Device N

U_TOP

CS_N SCLK_N SDI_N SDO_N FAULT_N ALERT_N DRDY_N CONV_N

REG50 VSS

CS_S SCLK_S SDI_S SDO_S FAULT_S ALERT_S DRDY_S CONV_S

BAT

C_{COM}

VSS_{N-1}

510K*

C_{RF}

C_{RF}

C_{RF}

R_S R_S R_S R_S

C_{RF}

VSS_N

VSS_N

VSS_N

Wiring between devices should be shielded. PCB should include ground plane. Shield / plane connects to North IC VSS. The South end of cable shield is connected through C_{COM} to the ground plane of the next lower device.

Device 2, 3,...

Device 1

R_S R_S R_S R_S

VSS_1

2M*
2M*
2M*

2M*

C_{RF}

VSS_1

Isolation Barrier

CS_N SCLK_N SDI_N SDO_N FAULT_N ALERT_N DRDY_N CONV_N

CS_H 100
SCLK_H 100
SDI_H 100
SDO_H 100

ISO7241
Isolated SPI Buffer

U_BASE

VBAT

BAT

VSS

C_{COM}

VSS_1 VSS_2

VDD_A VDD_B

CS_S SCLK_S SDI_S SDO_S FAULT_S ALERT_S DRDY_S CONV_S

To Microcontroller

ISO72xx have very high dv/dt. These 4 resistors (100R-470R) limit reflections and bounce.

5V

ISOLATED POWER

VSS_1

The bottom of the stack is terminated directly to VSS. No resistors are used to terminate the bottom of the stack.

.022 50   50 .022

VSS_1

VSS_A

VSS_1

VSS_1

These optional components decouple HF common-mode noise which may be induced in the stack by the inverter, local power module, etc. The R is used to lower the Q of the resonant loop created by the transformer L, parasitic C and added capacitors. Two series caps are used to reduce shock hazard in the event one cap fails. RC values shown are approximate, and depend on transformer, power supply switching frequency, and system noise characteristics.