Layout plan for UCD9224 & related circuitry:
Top & bottom layer: Signal traces
Layer two: ground plane
layer 3: Analog ground near near UCD9224
to pick up all analog connections
and V33 elsewhere
if inner layers needed for signal traces
use layer 3, not 2

Generally: most critical to get
filter caps close as possible to respective pins
Pins 36 7 47 to be tied directly to U1 powerpad
and have a feed thru close by to layer 3

target 1.2v across eap – ean at nominal vout

C17, C19 near U1 pins 33,34

ceramic friendly part

170mW U2 TPS71733DCKx

5V C4 1uF IN OUT C5 0.01uF GND EN NR/FB C14 4.7uF TP5 V33 C17 0.01uF R44 10 V33_A C15 4.7uF C19 0.01uF R99 0

C7 0.1uF C16 0.01uF C6 0.1uF C13 1uF V33_A

500mV reference for current monitors

V33 R37 5.62k 0.5V R38 1k

V33 R30 10k R31 10k TH11 TH13 R29 10k TH12 R35 10k

CH2_SENSE+ R21 1k differential pair R22 100k C11 680pF R36 10 CH2_SENSE–

CH1_SENSE+ R19 1k differential pair R20 100k C10 680pF R26 10 CH1_SENSE–

(Sheet 2)

U1 UCD9224RGZ

48	ADCref	22	GPIO–2
41	V33FB	21	GPIO–1
34	V33A	31	(JTAG)nTRST
33	V33D	30	(JTAG)TMS
35	BPCap	29	(JTAG)TDI/Sync_In
		28	(JTAG)TDO/Sync_Out
		27	(JTAG)TCK
		39	EAP2
		40	EAN2
		37	EAP1
		38	EAN1
		24	TMUX–1
		23	TMUX–0
		46	Temperature
		43	ADDR_1
		44	ADDR_0
		20	PMBus_Cntrl
		19	PMBus_Alert
		11	PMBus_Data
		10	PMBus_Clk
		4	Vin/lin
		32	Dgnd1
		36	Agnd1
		47	Agnd2
		49	PwPd
		5	nRESET
		12	DPWM–1A
		13	DPWM–1B
		14	DPWM–2A
		16	DPWM–3A
		9	SRE–1A
		18	SRE–1B
		15	SRE–2A
		17	SRE–2B
		6	FLT–1A
		7	FLT–1B
		8	FLT–2A
		25	FLT–3A
		42	CS–1A
		2	CS–1B
		3	CS–2A
		1	CS–3A
		45	Vtrack
		26	PowerGood

TH4 TH5 TH6 R2 133k PM ADDRESS R5 133k

R40 51 PWM_MAIN_1A R41 51 PWM_MAIN_1B R42 51 PWM_MAIN_2A R43 51 PWM_MAIN_2B

SRE–1A SRE–1B SRE–2A SRE–2B

CURRENT_LIMIT_FLAG_1A CURRENT_LIMIT_FLAG_1B CURRENT_LIMIT_FLAG_2A CURRENT_LIMIT_FLAG_2B

R39 1M R32 1M R33 1M R34 1M

R10 2k R9 2k R8 2k R3 2k

AVERAGED_OUTPUT_CURRENT_PH_1A
AVERAGED_OUTPUT_CURRENT_PH_1B
AVERAGED_OUTPUT_CURRENT_PH_2A
AVERAGED_OUTPUT_CURRENT_PH_2B

TH2 TH3 C9 0.01uF C12 0.01uF C3 0.01uF C8 0.01uF

C2 0.01uF R7 2.74k R4 15k 12VIN R24 10k V33

V33 R25 100k R27 100k R28 100k R23 1M

J2 NC NC NC NC NC PM Bus

TP1 TP2 TP3 TP4

Digital Control

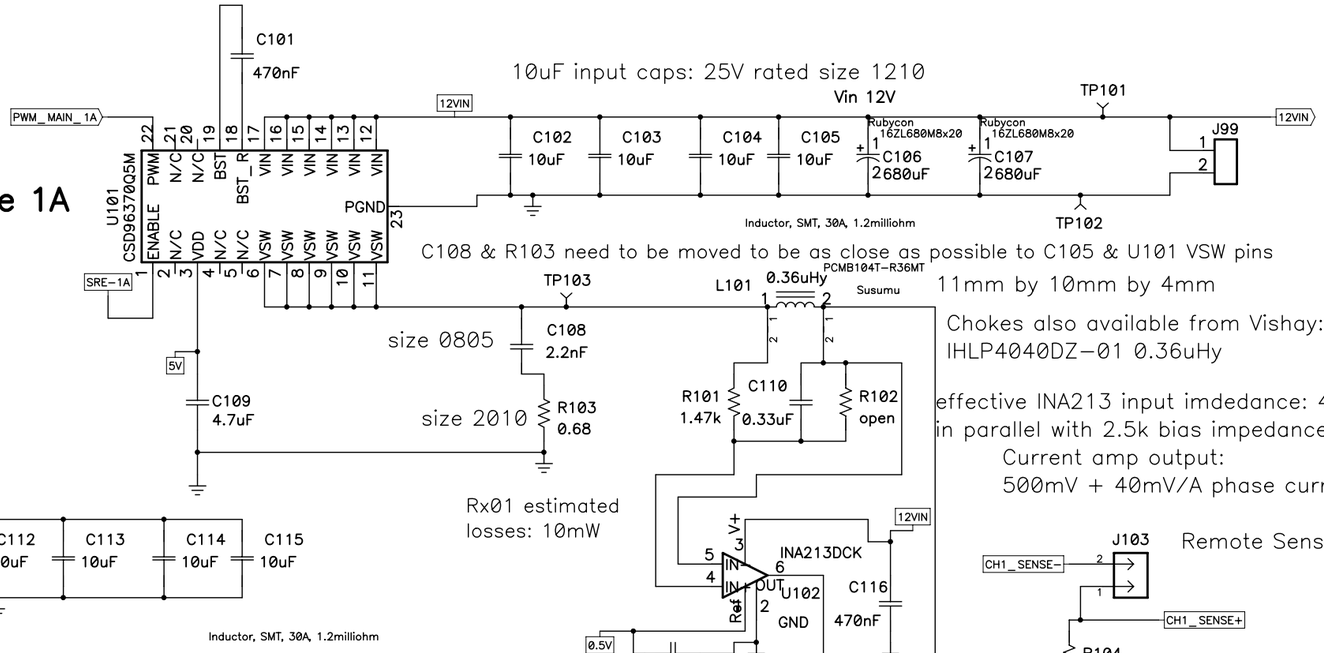
This page started with Ed Jung's HPA397E1 rev E1.08 board

Texas Instruments

Title	UCD9224 / CSD96370Q5M 2 Outputs		
Size C	Number PMP6000		Rev A
Date February 16, 2011		Drawn by Josh Mandelcorn	
Engineer Josh Mandelcorn	Filename PMP6000_revA.sch	Sheet 1 of 3	

Layout plan for power stages:
layers top & bottom for most power and signal traces
layer 2 will be ground,
power pad of U101 and U103 to ground with several vias
Get as much ground plane around U101 and U103 on each layer to cool these parts

Pwr Stage 1A



Pwr Stage 1B

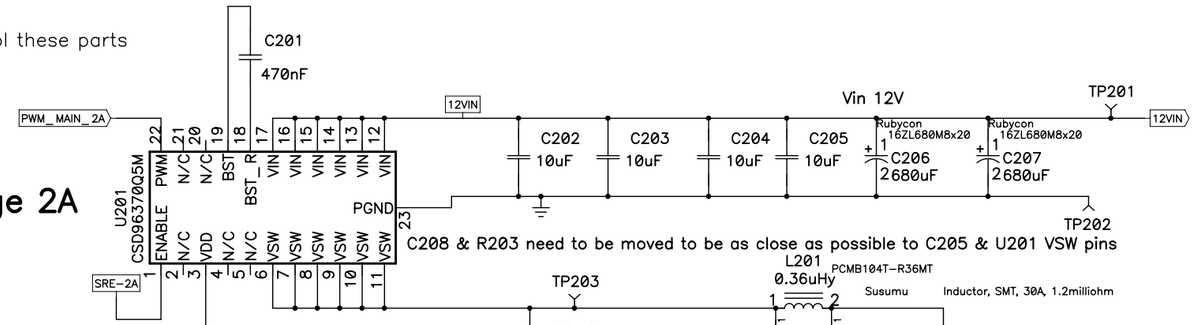
Channel 1

Texas Instruments

Title: UCD9224 / CSD96370Q5M 2 Outputs		
Size: C	Number: PMP6000	Rev: A
Date: February 16, 2011		Drawn by: Josh Mandelcorn
Engineer: Josh Mandelcorn	Filename: PMP6000_revA.sch	Sheet: 2 of 3

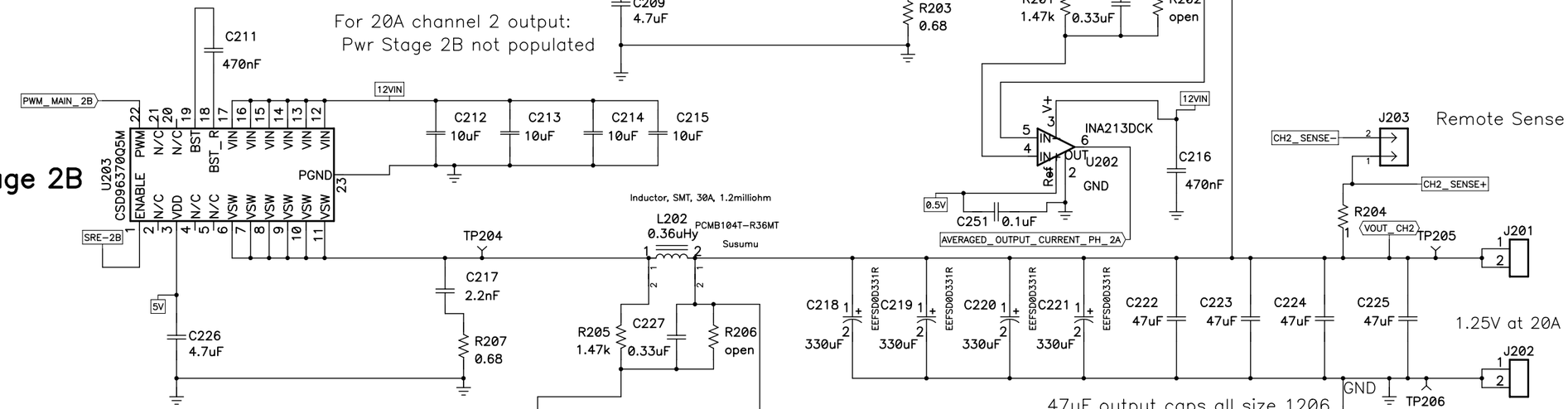
Layout plan for power stages:
layers top & bottom for most power and signal traces
layer 2 will be ground,
power pad of U201 and U203 to ground with several vias
Get as much ground plane around U201 and U203 on each layer to cool these parts

Pwr Stage 2A



For 20A channel 2 output:
Pwr Stage 2B not populated

Pwr Stage 2B



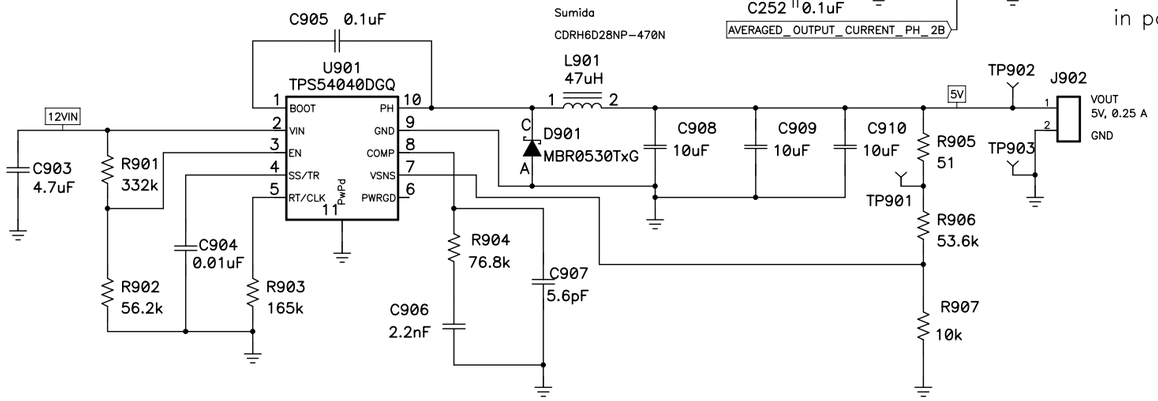
C217 & R207 need to be moved to be as close as possible to C215 & U203 VSW pins

47uF output caps all size 1206

All 4 output ceramics need to be in one place
near positive output connector
on current rev A layout:
stack Cx22 / Cx23 on top of Cx24 / Cx25

effective INA213 input imdedance: 40k
in parallel with 2.5k bias impedance or 2.353k
target 500mV + 40mV/A typical
48mV/A max or about 2V at 30A

Bias For Gate Drive



Channel 2 & 5V

Texas Instruments

Title: UCD9224 / CSD96370Q5M 2 Outputs			
Size: C	Number: PMP6000		Rev: A
Date: February 16, 2011		Drawn by: Josh Mandelcorn	
Engineer:	Filename: PMP6000_revA.sch	Sheet: 3 of 3	