Paralleling Power – Choosing and Applying the Best Technique for Load Sharing

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ABSTRACT

Redundant and distributed power systems often invoke the need to parallel power stages for a variety of reasons, among them enhanced reliability, enabling the use of standardized designs with varying loads, distributing heat sources, and for improved maintainability. However, paralleling usually requires load sharing to equalize stresses, and while many techniques have been used, there are many compromises between complexity and performance. This topic attempts to simplify the selection process by describing and comparing the more popular approaches and, through analysis and example, provide guidelines for the designer. Load share techniques from simple droop methods to closed loop current control - as well as many variations of each - are included in this material together with the design information to simplify their application.

I. INTRODUCTION

The topic of paralleling power supplies was on the sideline of design engineering tasks for decades. Except in a few specialized application areas like high reliability and redundant systems typically used in space, military, telecommunication central power systems and high end mainframe computers, sharing the load current among several parallel operated power supplies was not required.

Recent efforts in standardization, miniaturization and the proliferation of high current, low voltage power supplies have directed additional attention to various techniques to parallel power stages. The fundamental difficulty using parallel power processing circuits is to ensure that the load current is properly distributed among the parallel connected power modules. Only then, the design can be optimized for the highest reliability and lowest cost by ensuring equal temperature rise and by minimizing the power rating of the individual components.

As a starting point, it is important to establish the purpose and benefits of parallel power supplies and accompanying load sharing techniques in a typical power system design.

Standardization – load sharing enables the use of lower power, standardized modules across several applications promoting design reuse. The standardized approach makes power system solutions easily transferable between different end equipment platforms significantly reducing the time-to-market period. At the same time it increases component selection by allowing to choose from a wider variety of lower power components more readily available from different manufacturers.

Modularity – the resulting modularity provides great flexibility to the user. Systems can be easily reconfigured to accommodate broad variety of output voltage and load current combinations. Expandability of such a system provides a simple way to keep up with increasing load current requirements.

Redundancy – when implemented, maximizes system availability in critical applications. A redundant system has at least one reserve module which provides extra output current above and beyond the maximum current required by the load. Additional benefits of redundant power systems include improved maintainability as faulty units can be exchanged without system interruption. Furthermore, enhanced reliability is achieved through operating the modules below their full output current rating thus reducing their power dissipation and temperature rise.

Thermal management – the primary driver in all paralleling schemes for lower power applications is the decentralized heat dissipation of the parallel power stages. By distributing the power dissipation among a larger number of power components and over an increased surface area, thermal management and airflow requirements can be kept at a more economical level.

Equalizing temperature rise – it is well established knowledge among reliability engineers that operating temperature has a profound effect on the life expectancy of electronic components. A well designed load sharing circuit ensures equal distribution of the load current among the parallel connected power supplies. Matching currents mean equal power dissipation, i.e. very similar temperature rise which will improve the long term reliability of the system.

Minimizing component ratings – voltage and current ratings of electronic components in the power supply are proportional to the continuous power rating of the circuit. Since the accuracy of load sharing has a direct impact on the maximum power each power stage has to process, the chosen load sharing technique has a direct, measurable impact on the cost of the system.

The price to pay for all these benefits is the added complexity introduced by the load share circuit which varies widely depending on the implemented technique.

II. PARALLELING POWER STAGES

The simplest concept of paralleling is demonstrated in Fig. 1 picturing parallel operated power stages controlled by a single control loop. The operation is based on a single feedback loop and pulse width modulator (PWM). The controller generates the duty cycle D which is distributed for the main power switches.

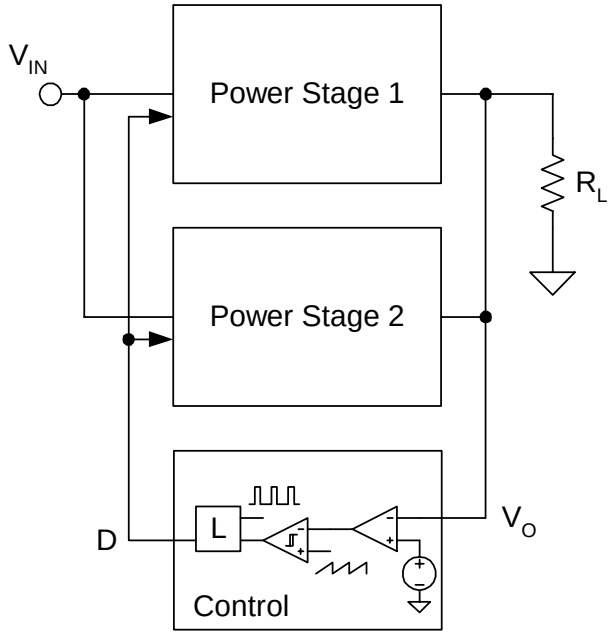

Fig. 1. Concept of parallel power stages.

This approach assumes voltage mode control because the single PWM comparator is unable to control the individual currents of the power stages. Thus, the clock ramp is used to determine the necessary duty ratio. In order to achieve load sharing among the modules, the power stages must be identical. Not only the components, but the printed circuit board layouts of the power stages must match very well.

Unfortunately, 100 percent matching is not achievable in practice, which will have an effect on how well the load current is distributed in this system. Component tolerances and parasitic circuit elements will ultimately introduce minor difference in the effective duty ratio of the power stages even though the control duty ratio, D is identical for each one of them.

Since the input and output voltages are common for all the parallel units there is only one correct duty ratio which satisfies the transfer function of the chosen topology. To demonstrate this phenomenon, Fig. 2 shows the effective duty cycles and energy storage inductor current waveforms of two parallel power stages used in Fig. 1.

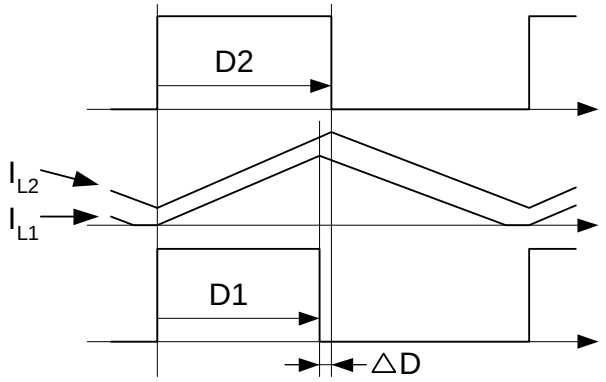

Fig. 2. Effective duty ratio difference and its effect on the inductor current waveforms.

The correct duty cycle always corresponds to the longest conduction period of the main switch, while energy transfer from the input to the output takes place. This can be proven easily by looking at the volt-second balance, i.e. current waveform in the energy storage inductors. In this case the actual output inductor value and switching frequency have no effect, since they will influence the ripple current amplitude only.

As shown in Fig. 2, the duty cycle D2 keeps the current constant as the starting and finishing points of the current waveforms are equal. Accordingly, the shorter D1 duty cycle is insufficient to apply enough volt-second product for balance to be reached. Therefore the average current in L2 will decrease until – in steady state – discontinuous mode operation is established as pictured in Fig. 2.

Based on these observations, the operation of the system can be described as follows: at light load, while all power stages are in discontinuous inductor current mode (DCM), they will share the load current reasonably well. As soon as the operation is in continuous inductor current mode (CCM), the power stage with the largest effective duty ratio will deliver most of the load current while the other stages stay in DCM. Their average output current will remain relatively low and can be estimated as:

$$I_O \approx \frac{I_{L,P-P}}{2}$$

Considering the above findings the system in Fig. 1 would never work, because only one unit – with the largest effective duty cycle – could operate in continuous inductor current mode and it would deliver almost all of the load current. Fortunately, there is a balancing mechanism which makes this approach useable. As current increases in the converter, there are resistive voltage drops which work in our favor. Fig. 3 explains what happens when the resistive voltage drop is taken into consideration.

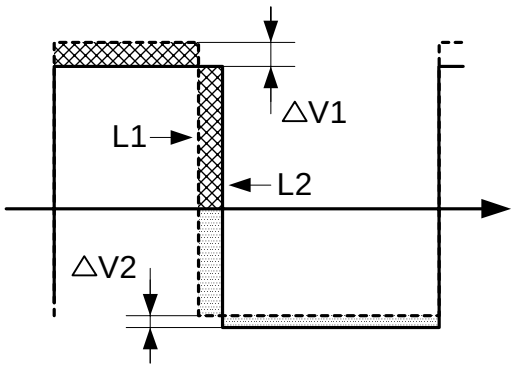

Fig. 3. Volt-second balancing based on parasitic resistive voltage drop.

As current increases in the power stage with the largest duty cycle so does the resistive voltage drop. Fig. 3 depicts a steady state operating point where the voltage drops ΔV1 and ΔV2 provide the necessary balancing mechanism. The required voltage drops correspond to a very well defined constant current difference between the two output currents. Once this ΔI is developed between the two outputs, both inductor can operate in CCM thus they will share the load. ΔI depends on the input and output voltages, V_{IN} and V_O respectively, transformer turns ratio where it is applicable ($N=N_P/N_S$), the duty cycle difference, ΔD and the equivalent resistance, R_{EQV} in the path of the current.

ΔI can be calculated based on the equivalent circuit of Fig. 4 which represents a generic power stage where all components are transformed to the energy storage inductor side of the circuit. In this model, R'_P is the primary side resistance transformed to the secondary side by the turns ratio, R_{SEC} is the resistance of the secondary winding of the transformer, R_{SW} is the resistance of the forward switch, R_{IND} is the winding resistance of the inductor and R_{SR} is the resistance of the freewheeling rectifier element. Depending on the power stage topology, some components might not be present in the equivalent circuit.

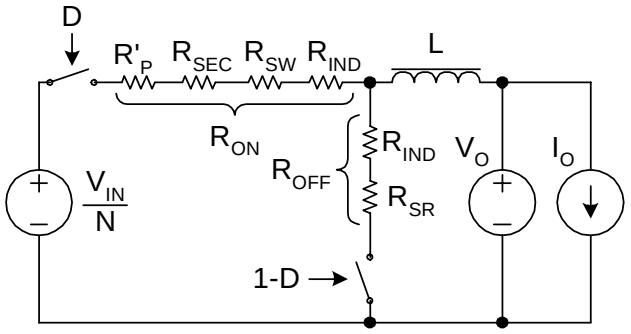

Fig. 4. Simplified power stage model.

The calculation is based on the fact that the average voltage applied on the left hand side of the inductor must be equal to the output voltage V_O. This condition can be expressed as:

$$\left(\frac{V_{IN}}{N} - I_O \cdot R_{ON}\right) \cdot D - I_O \cdot R_{OFF}(1-D) = V_O$$

which expression can be rearranged as:

$$\frac{V_{IN}}{N} \cdot D = V_O + I_O \cdot \left(R_{ON} \cdot D + R_{OFF} \cdot (1-D)\right)$$

From this, the equivalent resistance can be found as:

$$R_{EQV} = R_{ON} \cdot D + R_{OFF} \cdot (1-D)$$

Although R_{EQV} is a function of the duty cycle, it can be assumed that for small duty cycle change its value is constant. After substituting R_{EQV} and looking at the effect of small change in duty cycle:

$$\frac{V_{IN}}{N} \cdot \Delta D = \Delta I_O \cdot R_{EQV}$$

which gives:

$$\Delta I_O = \frac{V_{IN}}{N \cdot R_{EQV}} \cdot \Delta D$$

This equation shows that the current difference is constant. The equation can be further modified for percentage errors at a chosen operating point (I_O). It is the ratio of the module's output current deviation to the load current divided by the number of parallel power stages (n):

$$\%E(I_O) = \frac{(n-1) \cdot V_{IN} \cdot D}{n \cdot N \cdot R_{EQV} \cdot I_O} \cdot \%D$$

The above equation can be used to calculate the current sharing accuracy as a function of the load current and effective duty cycles of the power stages. Since the output current shows up in the denominator on the right hand side, the percentage of error diminishes at higher output currents which is consistent with a fixed current error. Finally, Fig. 5 summarizes the load sharing characteristic of the system in Fig. 1 using two power trains.

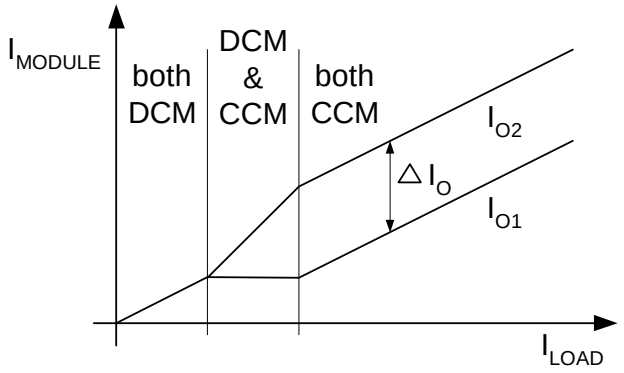

Fig. 5. Load share profile of parallel power stages (single voltage mode controller).

As mentioned before, one of the main disadvantages of this technique is that it can not be implemented with current mode control. Even simple current limiting can be troublesome using only one current sense signal representing the sum of the currents in the parallel power stages.

In order to implement cycle-by-cycle current limiting in the individual power stages, parts of the PWM logic must be implemented locally as shown in Fig. 6.

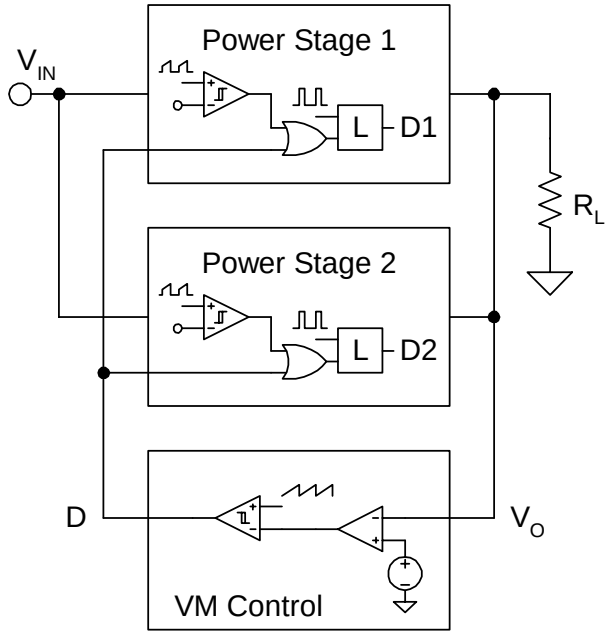

Fig. 6. Parallel power stages with independent cycle-by-cycle current limit.

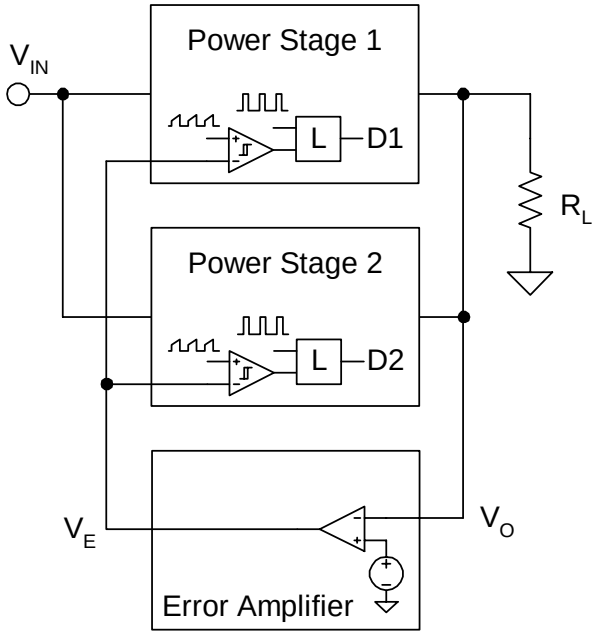

Fig. 7. Current mode control for parallel power stages.

In voltage mode control, it is still desirable to use a single PWM controller to determine the operating duty cycle and distribute D between the parallel power stages. This master duty ratio can be truncated by the cycle-by-cycle current limit comparator to protect the individual circuits against over current.

This technique is preferred over duplicating the PWM comparators at the power stage level because it prevents additional errors due to variation between local ramps. Inequality in ramp amplitude and ground potentials can easily turn into duty cycle difference when using a common feedback signal. As shown previously, duty cycle difference can cause large discrepancy in output currents in absence of a balancing mechanism.

Of course, once a current comparator is introduced to the system for cycle-by-cycle protection, current mode control can be readily implemented which can maintain equilibrium for the parallel connected power stages. Fig. 7 displays the simplified schematic of a current mode configuration for parallel power stages.

This approach still uses a single voltage error amplifier for output voltage regulation. The error signal, V_E is distributed throughout the system. The control is based on comparing the peak currents of the parallel power stages to this common error voltage. The duty cycles now can be individually adjusted to maintain similar current levels in the parallel connected power circuits. Consequently, peak current mode control eradicates the large error caused by duty cycle inequality. Unfortunately it has its own error sources which will determine the performance of the system. These error terms are demonstrated in the simplified schematic of Fig. 8 and will help to quantify the potential accuracy of the technique.

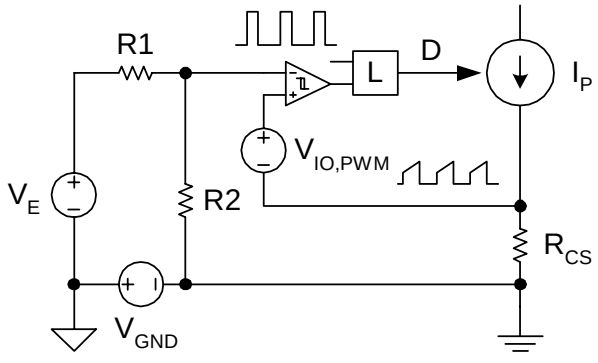

Fig. 8. Error sources in peak current mode control.

Since each power stage determines its own unique operating duty ratio to control the peak current in the circuit, the PWM comparator and logic must be locally duplicated. The common error signal is than compared to the measured current sense signal at the input terminals of the PWM comparator in each power stage. There are three components which affect the accuracy of the peak current measurements. According to Fig. 8, V_{GND} is the potential difference between the analog ground of the error signal V_E and the respective power grounds which serve as the reference potential for the current sense resistor. The tolerance of the resistor value itself is another source for error. Finally, the input offset voltage of the PWM comparator contributes to the inaccuracies as well. The following equation gives the relationship between the controlled peak current and the variables in the measurement circuit:

$$(V_E + V_{GND}) \cdot G_{DIV} = I_P \cdot R_{CS} + V_{IO,PWM}$$

where the divider gain is defined as:

$$G_{DIV} = \frac{R2}{R1 + R2}$$

The peak current, I_P can be expressed as:

$$I_P = \frac{G_{DIV} \cdot (V_E + V_{GND}) + V_{IO,PWM}}{R_{CS}}$$

This peak current is the sum of the peak magnetizing and the peak output inductor currents as shown in Fig. 9. Therefore, the effect of the magnetizing and output inductor value on the average output current should be analyzed next. These errors are not related to measurement accuracy. They stem from the fundamental operation of peak current mode control and a systematic peak-to-average error.

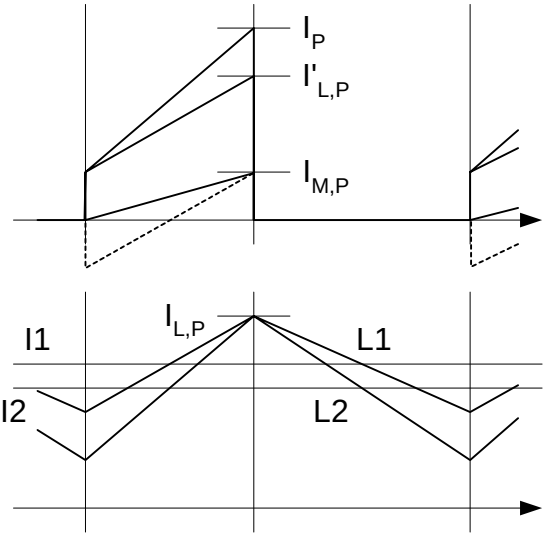

Fig. 9. Contributions of magnetizing and output inductor tolerances to load share error.

According to the waveforms, the peak current can be expressed as:

$$I_P = I_{M,P} + I'_{L,P}$$

where

$$I_{M,P} = \frac{V_{IN}}{L_M} \cdot D \cdot T$$

and

$$I'_{L,P} = \frac{1}{N} \cdot \left(I_O + \frac{(V_{IN} - V_O \cdot N) \cdot D \cdot T}{2 \cdot N \cdot L_O} \right)$$

The first expression describes the effect of the magnetizing inductance while the second equation gives the peak-to-average error as a function of the output inductor value. Equating the two expressions of I_P and solving it for I_O yields:

$$I_O = \left(G_{DIV} \cdot (V_E + V_{GND}) + V_{IO,PWM}\right) \cdot \frac{N}{R_{CS}} - N \cdot V_{IN} \cdot D \cdot T \cdot \frac{1}{L_M} - \frac{(V_{IN} - V_O \cdot N) \cdot D \cdot T}{2 \cdot N} \cdot \frac{1}{L_O}$$

TABLE 1. ABSOLUTE AND PERCENTAGE ERRORS IN CURRENT SHARING USING PEAK CURRENT MODE CONTROL

	Variable	Actual difference (ΔI_O)	Percentage output current error ($\%I_O$)
	$V_{IO,PWM}$	$\Delta I_{O1} = \frac{N}{R_{CS}} \cdot V_{IO}$	$\%E1 = \frac{N}{I_O \cdot R_{CS}} \cdot V_{IO}$
2	V_{GND}	$\Delta I_{O2} = \frac{G_{DIV} \cdot N}{R_{CS}} \cdot V_{GND}$	$\%E2 = \frac{G_{DIV} \cdot N}{I_O \cdot R_{CS}} \cdot V_{GND}$
3	R_{CS}	$\Delta I_{O3} = \frac{N \cdot (G_{DIV} \cdot (V_E + V_{GND}) + V_{IO})}{R_{CS}^2} \cdot \Delta R_{CS}$	$\%E3 = \frac{N \cdot (G_{DIV} \cdot (V_E + V_{GND}) + V_{IO})}{I_O \cdot R_{CS}} \cdot \%R_{CS}$
4	L_O	$\Delta I_{O4} = \frac{(V_{IN} - N \cdot V_O) \cdot D \cdot T}{2 \cdot N \cdot L_O^2} \cdot \Delta L_O$	$\%E4 = \frac{(V_{IN} - N \cdot V_O) \cdot D \cdot T}{2 \cdot N \cdot I_O \cdot L_O} \cdot \%L_O$
5	L_M	$\Delta I_{O5} = \frac{V_{IN} \cdot D \cdot T \cdot N}{L_M^2} \cdot \Delta L_M$	$\%E5 = \frac{V_{IN} \cdot D \cdot T \cdot N}{I_O \cdot L_M} \cdot \%L_M$

The error contribution of any particular variable can be determined by differentiating the equation. The differentiation has to be carried out one by one for all the variables. The results are given in Table 1 above.

Notice again that all expressions in the right column have I_O in the denominator indicating that the load share accuracy improves at higher load currents. Important to note that the load share accuracy depends not only the control technique, but also on the topology, switching frequency and operating point through the parameters V_{IN}, D, T and the transformer turns ratio, N where it is applicable. Naturally, for non-transformer-coupled topologies N becomes one and the magnetizing inductor term (5) in Table 1 should be neglected.

Once the individual error terms are clarified the overall load share accuracy can be calculated either statistically or for worst case. If a certain load share accuracy must be guaranteed, the worst case error should be used:

$$\%E_{MAX} = \%E1 + \%E2 + \%E3 + \%E4 + \%E5$$

The two paralleling techniques discussed before use a single feedback loop and no dedicated circuitry to ensure equal current distribution between the power stages. These methods are capable to share the load current and can be implemented with no additional circuitry. Despite their simplicity and cost effectiveness they are rarely used because their lack of redundancy and sensitivity to single point failure. Furthermore, they are not truly modular because they must share either the duty cycle or the sensitive analog error signal generated by the error amplifier. Consequently the power circuits should be mounted in close proximity paying very careful attention to layout, noise and voltage drop in the ground connections. These often forgotten techniques are included for completeness and because they demonstrate the fundamental error sources and calculation methods in paralleling power supplies.

III. PARALLELING POWER SUPPLIES

What differentiates a power supply from a power stage is that it has its own dedicated controller. A power supply can operate either stand alone or in parallel when the requirements of load sharing are addressed in the system. Due to the need for stand alone operation these power supplies must provide output voltage regulation through their respective feedback loops which introduces the next level of complexity for load sharing. The problem can be easily demonstrated by looking at the simplified block diagram in Fig. 10.

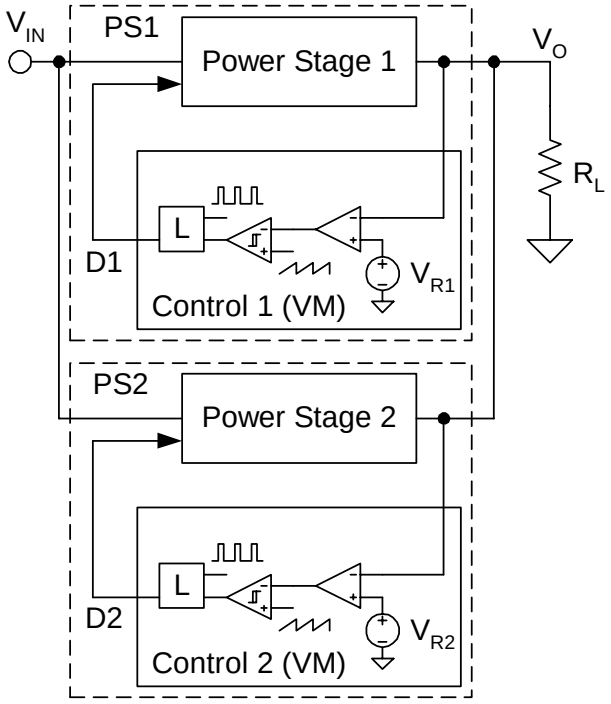

Fig. 10. Parallel connection of power supply modules.

Voltage regulation of a power supply is based on a closed negative feedback loop where the output voltage is compared to a reference voltage by the error amplifier. In case of two independent power supplies, it is inevitable that the references, V_{R1} and V_{R2} in Fig. 10, the feedback dividers and offsets are slightly different due to manufacturing tolerances. Therefore, each power supply has its own, slightly different output voltage levels – V_{O1} and V_{O2} – where the output voltage would be regulated in stand alone operation. This slight deviation in the individual output voltage levels is referred to as initial set point accuracy. A power supply's set point accuracy is determined by the accuracy of its reference, output voltage divider, the input offset of the error amplifier, and ground potential difference as depicted in Fig. 11.

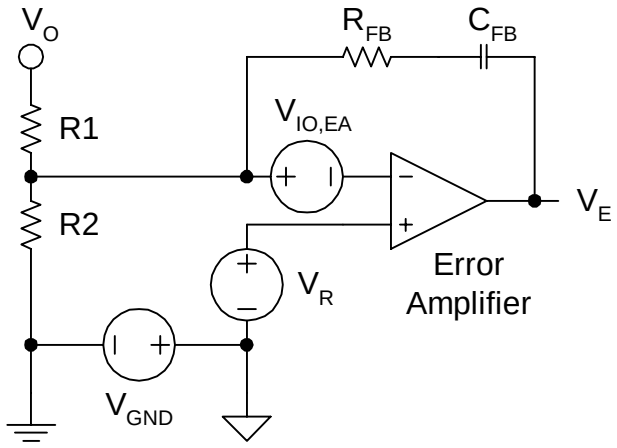

Fig. 11. Initial set point error components.

The voltage level where the output will be regulated can be found as:

$$V_O = \frac{R1+R2}{R2}\cdot\left(V_R + V_{GND} + V_{IO,EA}\right)$$

It is important to emphasize that ground potential difference between the reference points of the feedback divider and the voltage reference can be a serious contributor in set point inaccuracy. Often designers pay close attention to the input offset voltage of the error amplifier, usually in the millivolts range but neglect the potentially tens of millivolts of voltage drop in the ground connection which might turn out to be a more significant error source.

The set point accuracy equation can be solved using the previously shown partial differential method. The results are:

$$\%V_{O1} = \%V_R$$

$$\%V_{O2} = \frac{V_{GND}}{V_R}$$

$$\%V_{O3} = \frac{V_{IO,EA}}{V_R}$$

$$\%V_{O4} = \frac{2}{1+\frac{R2}{R1}} \cdot \%R_{1,2}$$

The first equation shows that the tolerance of the reference voltage directly impacts the set point. Assuming that V_{GND} and $V_{IO,EA}$ are negligible compared to the reference voltage, the second and third components will yield a much smaller dependency because the expression yields a very small value.

The effect of the resistive divider is rather interesting. Fig. 12 shows the normalized solution as a function of the resistor ratio R2/R1.

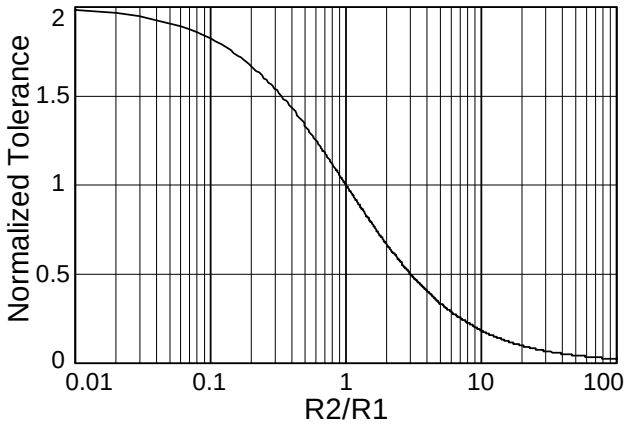

Fig. 12. Normalized output voltage tolerance versus feedback resistor ratio.

The chart covers the ratio from one hundredths to hundred and can be read as follows: find the actual R2/R1 ratio on the horizontal axes and read the corresponding multiplier on the vertical scale. If there are 1% resistors used in the design, multiply 1% by the number just read off the vertical axes. That is the contribution of the feedback divider to the initial set point inaccuracy. Interestingly, when R1=R2 using 1% resistors means ±1% output voltage variation but the same 1% type resistors can cause nearly ±2% output voltage error if R1 is significantly larger than R2.

The worst case set point accuracy is than estimated as:

$$\%V_O \approx \%V_R + \frac{2}{1+\frac{R2}{R1}} \cdot \%R_{1,2}$$

Set point accuracy is an important parameter because of its significant effect on the load share accuracy in the next couple of techniques to be discussed.

A. Sharing in current limit

The first technique is called inherent droop method where the overload protection of the power supply is utilized for sharing the load current. Modern power electronic modules are all protected against excessive output current by their current limit. Typical output characteristics of two identical power supplies are pictured on the V-I plane in Fig. 13. The effect of their initial set point and current limit tolerances are also highlighted in the diagram.

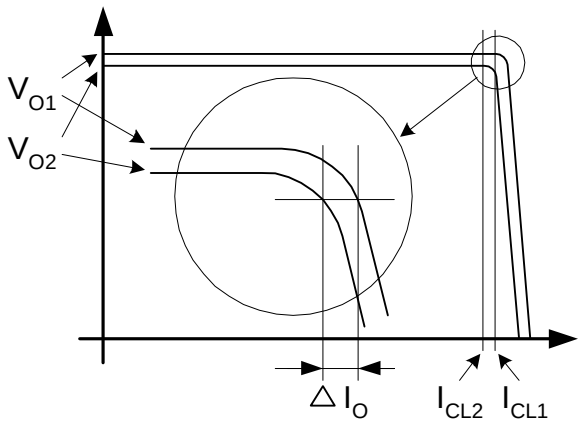

Fig. 13. Power supply output characteristics with current limit.

When these two power supplies are connected in parallel they will not be able to share the output current properly. Remember that we are paralleling two completely independent building blocks both capable of regulating the output voltage, although at slightly different levels. One would regulate the output at the level V_{O1} while the other requires an output voltage of V_{O2}. Initially, the output of the system is always regulated at the highest output voltage, in this example V_{O1}, as shown in Fig. 14. As the load

current increases this output voltage level is maintained until the power supply reaches its current limit point. Unfortunately, all other parallel connected power supplies with lower initial set points are not delivering any load current because their respective error amplifiers interpret the common output voltage as being too high. Once the power supply with the highest output voltage reaches its current limit, its operating mode changes from a constant voltage to a constant current source. As the load increases further the voltage falls to the next highest output voltage set point. At that point the second highest voltage power supply starts contributing to the output current until it reaches its maximum output current rating. Eventually, as the load current reaches its maximum value, all power supplies deliver their maximum output current.

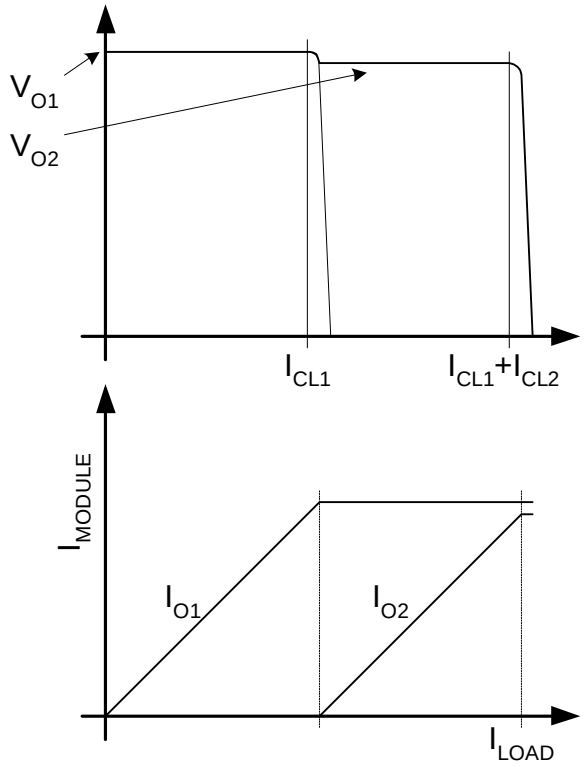

Fig. 14. Output characteristic and load current distribution of the parallel combination of the two power supplies of Fig. 10.

As Fig. 14 reveals, the output voltage is well regulated until the last member of the parallel connected group reaches its current limit operation. Unfortunately, the load current is not shared between the modules. Unless one module runs into current limit, the next lower set point unit can not deliver any current. This can be considered the worst possible scenario from reliability point of view. Unless the system is fully loaded, there will be power supplies which are in current limit while other ones idle at the same time causing wide variation in individual temperature rises.

Another potential problem to mention is the handover of control between the feedback loops. As one power supply reaches its current limit the output voltage starts to fall. It becomes regulated again at the next lower output voltage level where the next power supply can start supplying some load current. At this point the control is handed over from one power supply to another during which transition the output voltage could experience a glitch.

Obviously, this technique needs an accurate, reliable current limit. The accuracy of the current limit circuit is the determining factor how much current each module delivers in a parallel scheme. The tolerances of the current limit circuit can be analyzed using the equivalent circuit of Fig. 8 after replacing the error signal V_E with the reference voltage of the current limit circuit, V_{CL}. Accordingly, the equations listed in Table 1 are equally applicable after substituting V_E with V_{CL}. Additionally, the tolerance of V_{CL} has to be added to the error sources which can be expressed as:

$$\Delta I_{CL} = \frac{N}{R_{CS}} \cdot \Delta V_{CL}$$

or in percentages:

$$\%E6 = \frac{N \cdot V_{CL}}{I_{CL} \cdot R_{CS}} \cdot \%V_{CL}$$

Note that the $\frac{N \cdot V_{CL}}{I_{CL} \cdot R_{CS}}$ term is always one in current limit therefore the accuracy of the current limit is a direct function of the V_{CL} tolerance.

While this technique is clearly not recommended for load sharing, it highlights a couple of important aspects of paralleling independent power supplies. Primarily, component tolerances will set the output voltages apart. This initial output voltage difference prevents the units from sharing the load current due to the extremely low output impedance in voltage regulation mode. The output impedance of a power supply is the relationship between the change in output voltage in response to a change in output current. Once the unit enters current limit the output voltage becomes a strong function of the load which indicates high output impedance. The presence of the output impedance is then utilized in this rudimentary current sharing mechanism. A more sophisticated version of employing tightly controlled output impedance can be observed in the droop current sharing method.

B. The droop method

The technique has got its name from the fact that the output voltage of the power supply is made to slightly decrease as the load current increases. For the cursory observer it might look like the output voltage regulation is not working properly as the voltage *droops* at higher loads. But this is the result of the carefully selected output impedance which is designed into the power supply. The operating principle of this technique is summarized by a very simple equation and corresponding output characteristic of a power supply designed with droop method in Fig. 15.

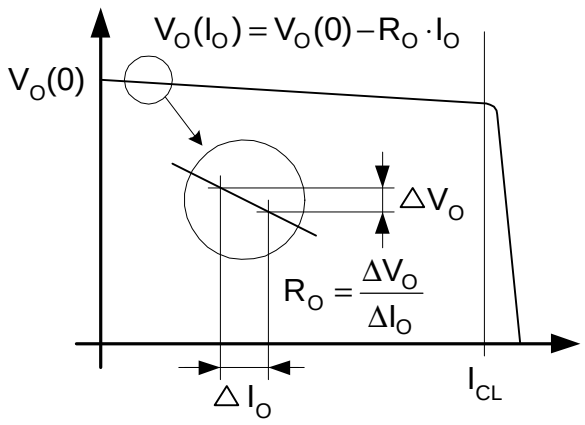

Fig. 15. Output characteristic with droop.

The fundamental difference between this output characteristic and the one in Fig. 13 is that a finite output impedance – R_O – can be observed through the entire voltage regulation region. A small constant slope of the graph to the left of the current limit region indicates the presence of R_O. The output voltage becomes the function of the load current and this phenomenon can be exploited for load sharing.

When two power supplies with droop output characteristics are paralleled in a system the load share accuracy depends on their initial set point accuracy and the tolerance of their output impedance according to Fig. 16.

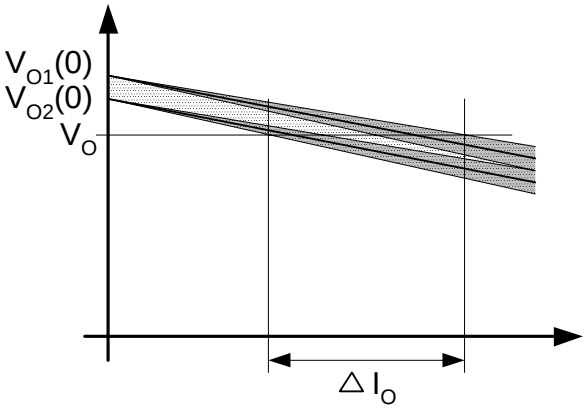

Fig. 16. Effects of set point and output impedance tolerances on load share accuracy.

In the above picture $V_{O1}(0)$ and $V_{O2}(0)$ represent the different output voltages with no load due to the tolerance of the initial set points. The gray shaded area is defined by the output impedance variation. V_O signifies the common output voltage of the parallel connected units while ΔI_O shows the worst case current sharing error between the modules. As the lines indicate the load share accuracy will depend on the tolerances but even more so on the actual value of R_O. A steeper slope, corresponding to higher output impedance could narrow ΔI_O between the individual output currents. Unfortunately, higher R_O also results in higher output voltage variation as the load current changes from zero to full load, therefore increasing the output impedance is not always feasible.

Since load sharing accuracy in these systems depends only on two components the mathematical analysis is rather simple. As mentioned before, the output characteristic of a power supply employing drop method can be given as:

$$V_O(I_O) = V_O(0) - R_O \cdot I_O$$

Rearranging the expression for Io and finding the partial derivatives yields the following two equations for output current tolerances as a function of initial output voltage and output impedance tolerances:

$$\%E1 = \frac{V_O(0)}{I_O \cdot R_O} \cdot \%V_O(0)$$

$$\%E2 = \frac{V_O(0) - V_O(I_O)}{I_O \cdot R_O} \cdot \%R_O$$

Closer examination of the equations shows a very large load share error due to the initial set point tolerance. The term multiplying the set point accuracy number in the first equation is the output voltage divided by the droop at a given output current. This number is load current dependent and it has its minimum value at full load in the 50 to 100 range. For example, assuming a 2% maximum droop of the nominal output voltage gives a minimum multiplier of 50. In the second equation the multiplier is one (1) which means the tolerance of the output impedance shows up directly in the load share error and it is constant for the entire load current range. The total error is the sum of the two errors. Fig. 17 summarizes the behavior of a system using parallel power supplies employing droop output characteristics.

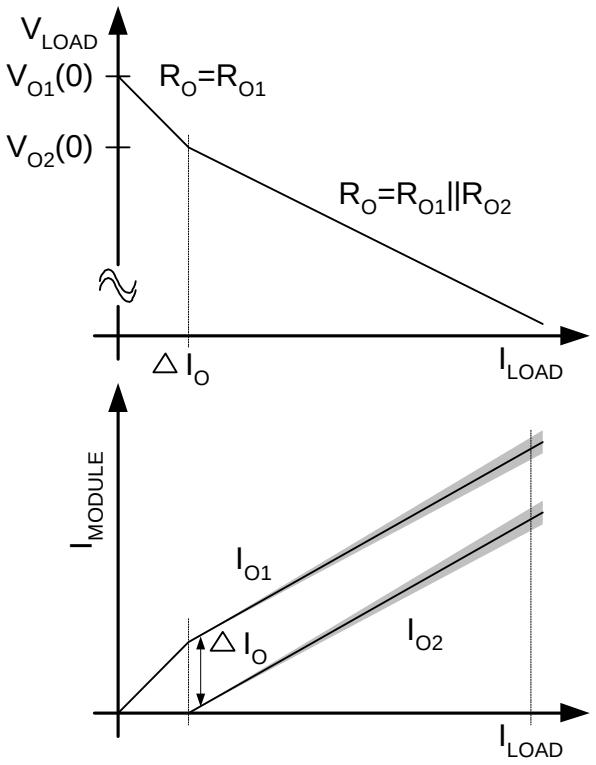

Fig. 17. System voltage and module currents of two paralleled power supplies designed with droop output characteristic.

It is interesting to notice the constant current deviation due to the initial set point tolerance which can be estimated as:

$$\Delta I_O = \frac{V_{O1}(0) - V_{O2}(0)}{R_{O1}}$$

assuming that $V_{O1}(0) > V_{O2}(0)$ as pictured in Fig. 17. Also shown, that at $I_{LOAD} = \Delta I_O$ the output impedance of the system is changing from R_{O1} to the parallel combination of R_{O1} and R_{O2}. The gray shaded area emphasizes the effect of the output impedance tolerance. When *n* number of power supplies are connected in parallel the system's equivalent output impedance is the parallel combination of all individual output impedances. That would suggest that if more modules are paralleled the individual output

impedances can be higher which should improve on the load share accuracy among the power supplies. Unfortunately increasing the number of modules does not help on the initial set point accuracy which is the major cause of current imbalance with droop method. Furthermore, it can be shown that the $I_O \cdot R_O$ product for a module remains constant in any system, independent of the number of units connected parallel therefore the load share accuracy can not be improved this way.

There are many different ways to implement the required output impedance – R_O – to achieve the desired droop output characteristic in a power supply.

Series resistance

Certainly the simplest idea is to use a low value resistor in series with the output of the power supply. Fig. 18 shows a typical arrangement for implementing R_O using a discrete resistor.

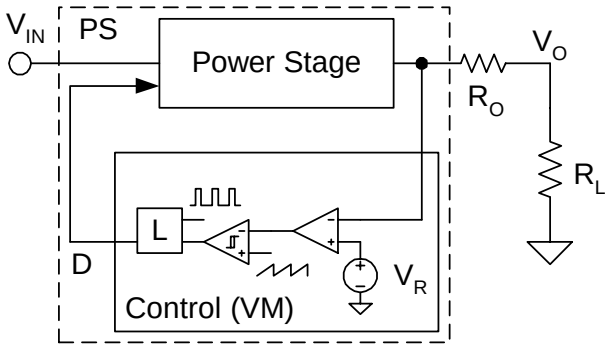

Fig. 18. Implementing finite output impedance with series resistor.

The important detail to notice is that the resistor must reside outside of the feedback loop. So the voltage across the load will have a current dependent component. In this case the tolerance of the series resistor is known and can be used to calculate the respective error component directly. Some of the disadvantages associated with this technique are the power dissipation of the resistor which is detrimental to the efficiency, the cost and relatively large printed circuit board area of a precision, low value, non-inductive resistor.

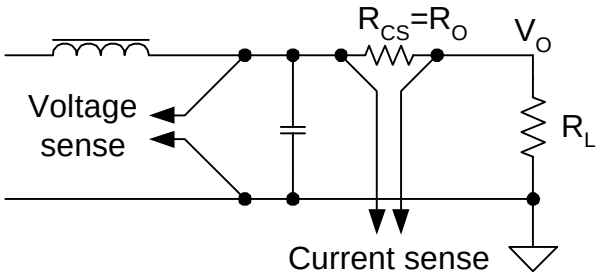

Fig. 19. Current sense resistor provides output voltage droop.

The problem can be mitigated if the current sense resistor – often present for overload protection – is used to implement the output impedance. This solution assumes that the power dissipation is acceptable and it requires the reposition of the current sense resistor R_{CS} according to Fig. 19.

Current dependent voltage feedback

This solution also utilizes the current sense information of the power supply to implement a finite output impedance but without the restriction on the value of the current sense resistor. The technique is based on summing the output current and voltage information and comparing it to a voltage reference by the error amplifier. While this approach can be implemented in many different ways, Fig. 20 illustrates an interesting circuit for summing the current and voltage information of a power supply.

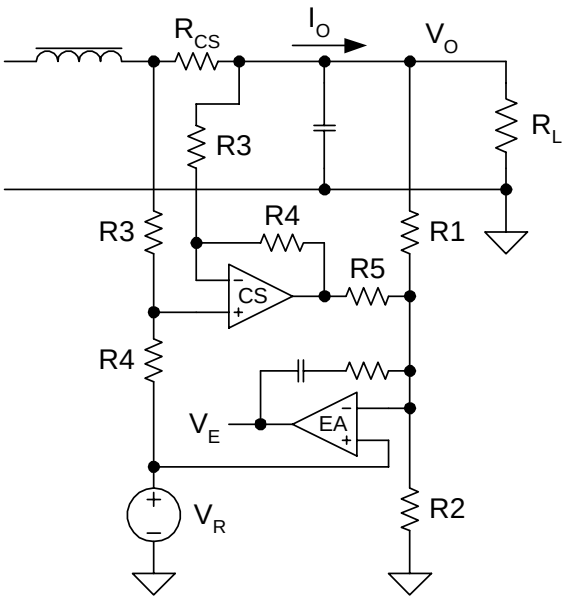

Fig. 20. Voltage feedback modulation using output current information.

The current sense amplifier is configured to reference the current sense signal to the same potential present at the non-inverting input of the error amplifier. This allows a simple addition of the current information to the feedback signal because the voltage across R5 will be proportional to the output current only. By properly choosing R3 and R4 values, the gain of the current sense amplifier is user programmable accommodating a wide selection of current sense resistor value to minimize power dissipation. The ratio of R1 and R5 provides the ultimate mechanism to set the output impedance of the power supply. The output voltage of the current sense amplifier, V_{CSO} in Fig. 20 equals:

$$V_{CSO} = V_R + \frac{R4}{R3} \cdot R_{CS} \cdot I_O$$

The circuit controls the output voltage according to the following relationship:

$$\frac{V_O - V_R}{R1} + \frac{V_{CSO} - V_R}{R5} = \frac{V_R}{R2}$$

After substituting the expression of V_{CSO} and rearranging for V_O:

$$V_O = \left(1 + \frac{R1}{R2}\right) \cdot V_R - \frac{R1}{R5} \cdot \frac{R4}{R3} \cdot R_{CS} \cdot I_O$$

The familiar expression for initial set point and droop characteristic can be recognized in this equation. The load share accuracy was calculated in the previous section as a function of set point and output impedance tolerance and those results can be applied here as well. The output impedance of the power supply is:

$$R_O = \frac{R1}{R5} \cdot \frac{R4}{R3} \cdot R_{CS}$$

Calculation of the output impedance tolerance can be carried out by the same partial differential method used earlier which gives the following solution:

$$\%R_O = \%R1 + \%R3 + \%R4 + \%R5 + \%R_{CSO}$$

As this result shows, adding the current sense amplifier is beneficial from efficiency and flexibility point of view but it increases the tolerance of the output impedance. Consequently the load share accuracy is slightly lower than in the previous example.

Using a limited gain error amplifier

This technique takes advantage of the natural output impedance of the power supply, best observed in open loop operation. The open loop output impedance can be defined using the equivalent circuit shown in Fig. 21.

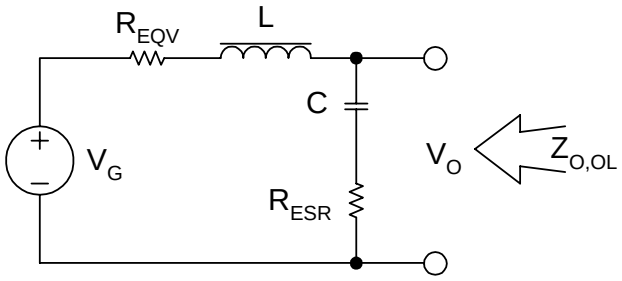

Fig. 21. Demonstration of the open loop output impedance.

The circuit consists of an ideal generator, V_G, the equivalent source impedance and the output filter. Since the primary interest is to use the power stage's output impedance to implement a droop characteristic, the parasitic resistances, in particular R_{EQV} must be considered. In open loop operation, the steady state output voltage droop is caused by the dc output impedance, which can be found easily as $R_{O,OL}=R_{EQV}$ where

$$R_{EQV} = R_{ON} \cdot D + R_{OFF} \cdot (1 - D)$$

as defined earlier in connection with Fig. 4. It is important to mention that the dc resistance of the filter inductor is part of the expression of R_{ON} and R_{OFF}, thus it is included in the equivalent resistance.

Once a negative feedback loop is implemented for voltage regulation, the power supply's output impedance is reduced significantly according to:

$$R_{O,DC} = \frac{R_{O,DC,OL}}{1 + G_{EA,DC}}$$

Assuming that the open loop output impedance is known and sufficiently high, a targeted output impedance can be realized by adjusting the dc gain of the voltage error amplifier in the power supply. With an integral compensation around the error amplifier the dc gain is very high, limited only by the open loop gain of the error amplifier. Accordingly, the output impedance becomes negligible and accurate output voltage regulation, which is independent of the load current is realized.

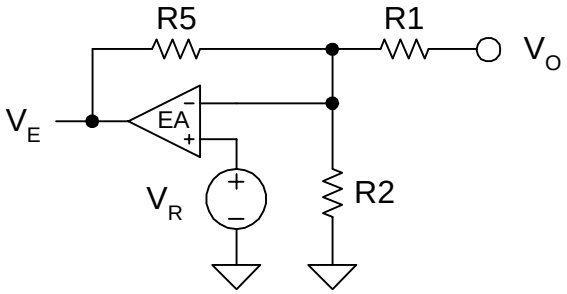

Fig. 22. Limited gain error amplifier configuration

On the other hand, using a limited gain error amplifier as pictured in Fig. 22, the dc gain is limited to:

$$G_{EA,DC} = \frac{R5}{R1}$$

By choosing R5 appropriately, the error amplifier gain can be set to implement the desired output impedance. This simplified approach is completely adequate to design the required droop output characteristic for the power supply. For completeness, Fig. 23 illustrates the output impedance in the frequency domain and the effect of the error amplifier gain with negative feedback.

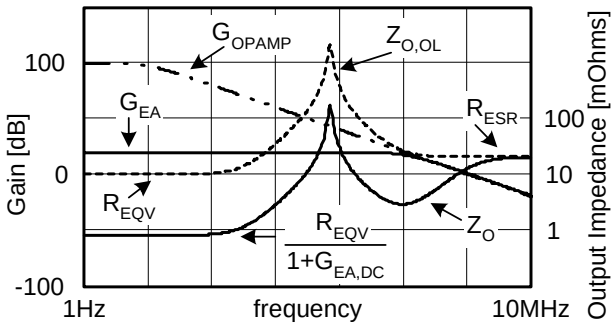

Fig. 23. Typical characteristics of the output impedance in the frequency domain with limited gain error amplifier.

At dc the open loop output impedance is the equivalent dc resistance looking back into the output of the power supply. As frequency increases, the output impedance rises due to the filter inductor. At higher frequencies the output capacitor shunts out the inductor and the output impedance falls to the value of the equivalent series resistance of the output capacitor. The solid lines in Fig. 22 demonstrates the effect of the limited gain error amplifier. The output impedance is reduced in a wide frequency range where GEA>1 (0dB) is maintained. Although this phenomenon is irrelevant from the output droop point of view, it provides useful insight how to reduce power supply output impedance in general.

Based on the equation found to determine the output impedance with a limited gain error amplifier, the accuracy of R_O depends on the tolerance of R_{EQV} and $G_{EA,DC}$ according to:

$$\%R_O = \%R_{EQV} + \frac{2}{1 + \frac{1}{G_{EA,DC}}} \cdot \%R$$

where $\%R_{EQV}$ denotes the accuracy of the source impedance and %R is the tolerance of R1 and R5 setting the gain of the error amplifier. The expression indicates a relatively large tolerance of the output impedance because R_{EQV} is defined by parasitic resistances in the power stage. Furthermore, temperature and duty cycle, i.e. load current and input voltage will vary the output impedance through their effect on the equivalent source impedance.

The limited gain error amplifier can provide for a much more accurate output impedance design if a unique property of current mode control is exploited. In both peak and average current mode control the error signal at the output of the voltage error amplifier is proportional to the output current of the converter as opposed to the duty ratio in voltage mode control. This fundamental difference in the control principle makes it possible to implement a more accurate output impedance with a limited gain voltage error amplifier in current mode control.

Using a typical limited gain error amplifier configuration as it was shown in Fig. 22, the principle of operation can be described and the design can be facilitated. Under a no load condition the error amplifier output idles at its minimum value which is required to regulate the output at its initial level. As the load current increases so does the error signal amplitude. At full load V_E reaches its maximum value above which the output current can not follow the error signal amplitude any more because of the current limit circuit – not shown in Fig. 22. Considering the current components summed together at inverting input of the error amplifier, it is easy to see that when V_E increases V_O must decrease. The relationship between V_E, V_O, V_R and the resistor values can be expressed by:

$$\frac{V_O - V_R}{R1} + \frac{V_E - V_R}{R5} = \frac{V_R}{R2}$$

From this equation the output voltage can be determined as:

$$V_O = \left(1 + \frac{R1}{R2} + \frac{R1}{R5}\right) \cdot V_R - \frac{R1}{R5} \cdot V_E$$

According to the above expression, the output voltage has two components. One is a constant value primarily defined by the reference voltage while the other one is proportional to the error voltage, thus to the load current. These components correspond to the initial set point at zero load and the droop. Taking into consideration that to adjust the output current of the converter from zero to full load (I_{CL}) requires the error signal to change from its minimum to its maximum value (ΔV_E), the equation can be modified to show the output current as a control parameter for the droop.

$$V_O = \left(1 + \frac{R1}{R2} + \frac{R1}{R5}\right) \cdot V_R - \frac{R1}{R5} \cdot \frac{\Delta V_E}{I_{CL}} \cdot I_O$$

where ΔV_E is the control range of the error amplifier output. From this the initial set point and output impedance of the converter can be found as:

$$V_O(0) = \left(1 + \frac{R1}{R2} + \frac{R1}{R5}\right) \cdot V_R$$

$$R_O = \frac{R1}{R5} \cdot \frac{\Delta V_E}{I_{CL}}$$

The tolerances can be calculated using the partial differentials as before. After the required mathematical manipulations the results are:

$$\%V_O(0) = \%V_R + 2 \cdot \left(\frac{R1}{R2} + \frac{R1}{R5}\right) \cdot \frac{V_R}{V_O(0)} \cdot \%R$$

$$\%R_O = \%V_{CL} + \%I_{CL} + 2 \cdot \%R$$

where $\%V_{CL}$ is the threshold tolerance of the current limit reference, $\%I_{CL}$ is the tolerance of the maximum output current including peak to average, current sense resistor and other factors as defined earlier. It is also assumed that all resistors have the same tolerance, %R.

Current sharing using droop output characteristic is an easy open loop technique which can be implemented with minimal or no additional components. It works without the need for communication between the parallel power supplies. Reasonable accuracy can be achieved by paying close attention to the initial set point accuracy of the individual modules using high performance voltage references and minimizing resistor tolerances in the feedback system. In very low output voltage, high current applications the acceptable output impedance might be restricted to keep the output voltage within its regulation window. This limitation has to be considered when choosing the droop method for load sharing.

From an efficiency point of view the series resistor technique carries the penalty of a potentially high power loss because the series resistance is predetermined by the required output impedance value. The second example where the current sense signal is added to the feedback signal provides a lower loss solution. Using a limited gain error amplifier in current mode control offers probably the most efficient way to design the desired droop characteristic.

C. Active current sharing

The most sophisticated and most accurate load sharing implementations rely on a closed loop negative feedback system, very similar to those control loops used to regulate the output voltage of a power supply. To make this approach work two pieces of information must be available in the system. One is the actual output current of the power supply and the other is the desired amount of output current. Since the goal is to evenly distribute the load current, the desired output current is the load current divided by the number of parallel modules. Therefore the task is two fold; measure the output current and generate the average output current information. In order to determine the average output current, the modules must be able to communicate, hence the units have to be connected. This connection which carries the average current information between the modules is the load share bus.

The output current of a particular power supply is compared to the average current information represented by the load share bus at the inputs of an error amplifier. The load share error signal is interfaced to the voltage error amplifier of the power supply. This error signal can be added either to the feedback node or to the reference of the voltage error amplifier depending on the designers preference. A greatly simplified diagram in Fig. 24 demonstrates the active current sharing principle.

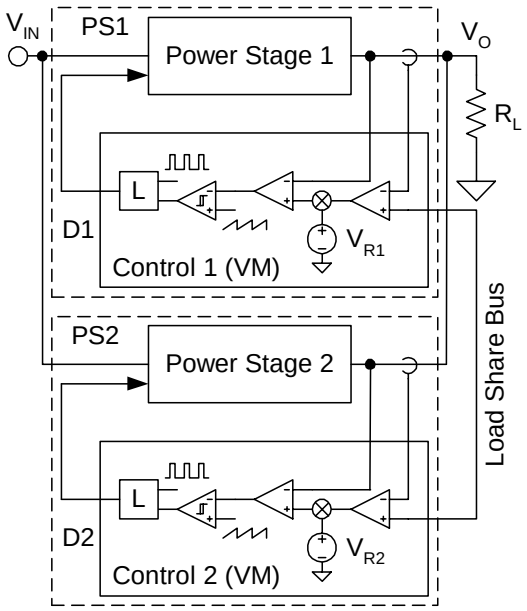

Fig. 24. Active load share principle.

As it is highlighted in the diagram active load sharing modifies the power supply's voltage reference to ensure equal output currents. Consequently all errors associated with the inner loop's initial set point and current measurement tolerance are eliminated by the load share error amplifier's corrective action. The output current measurement circuit of the load share controller, the generation of the average current information and possible ground potential differences among the parallel connected power supplies introduce new error sources which ultimately define the performance of the active load share technique. Many variations exist to produce the average current information and adjust the output voltage by the load share error signal but all of them can be classified into three fundamentally different solutions.

Dedicated master / slave active load share

In this arrangement one of the power supplies is selected to drive the load share bus using its own output current information. All other units take this information and adjust their own output current to match the current being delivered by the master. A typical implementation is pictured in Fig. 25.

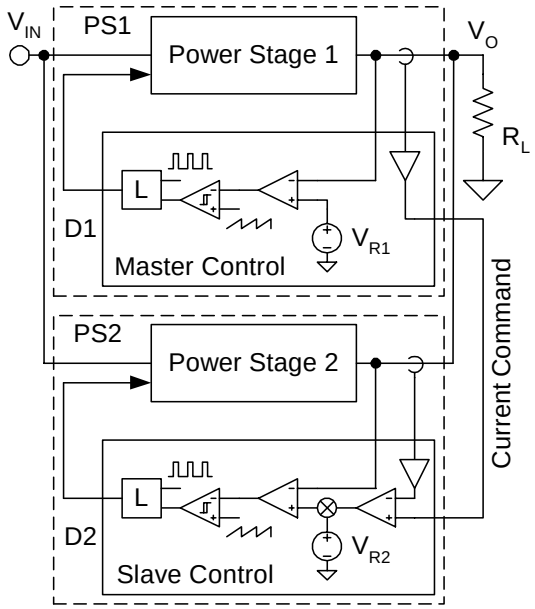

Fig. 25. Load Sharing with a dedicated master module.

Since the master module unilaterally controls the bus, the output current of the slave modules are not available for the master. Therefore, the master does not need a load share error amplifier. The load share bus becomes a current command for the slave modules. If the slave modules can deliver exactly the same current as the master then the load is perfectly distributed amongst all modules. Consequently, the signal on the current command bus still equals the average current information in the system.

The slave modules use an error amplifier with negative feedback to match their respective output current to the current command signal. Depending on the initial output voltages, the slave units might deliver either more or less current than the master. Accordingly, the output voltages of the slave units must be adjustable in both directions. Also note that the output voltage of the system is defined by the master only in a dedicated master-slave system.

There is one major disadvantage using a dedicated master module which impacts fault tolerance. If the master module fails, the current command is zero, consequently all units try to lower their respective output current to match the control signal. Generally, it is not possible for the slave units to lower their outputs that much because of the limited output voltage adjustment authority of the load share error amplifier. Nevertheless, the load share mechanism is decommissioned and the system reverts to a group of independent power supplies connected in parallel without a balancing mechanism as discussed earlier. In addition, output voltage regulation might be out of range since all power supplies are set to their minimum output voltage level by the load share error amplifier.

Automatic master / slave selection

The fault tolerance problem of the dedicated master-slave method can be addressed by a minor modification to the circuitry. Fig. 26 gives an idea of an automatic master selection scheme where any one of the parallel connected power supplies can assume the role of master and drive the current information presented on the interconnecting load share bus.

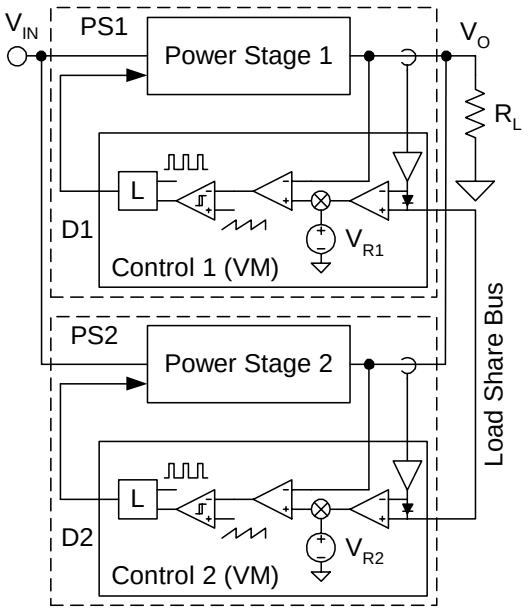

Fig. 26. Automatic master – slave load share concept.

In this implementation the power supplies are identical and they are all capable of taking the lead role as a master in the system. It is ensured by the ideal diode placed between the inverting and non-inverting inputs of the load share error amplifier. The master selection is taking place at start up before the load share loop becomes active. During this start up phase the current distribution is governed by the initial set points of the power supplies. The module with the highest output voltage will deliver more output current. Since all modules are copying their respective current information onto the load share bus, the diodes will allow the module with the highest current to seize control and drive the load share bus. In all other modules with lower currents, the diodes are reverse biased. The master is now singled out and provides the current command to the other power supplies. From this point on the operation of the system is identical to the one with a dedicated master unit. The slave modules adjust their output voltages to deliver the current demanded by the master. It is interesting to note that the master was selected because it has the highest output voltage among the modules. In order to match the output current of the master the slave units must increase their output voltage. This simplifies the adjustment circuit because it is only required to be able to adjust the output voltage upwards. Another consequence of the operation of the automatic master selection is that the output voltage is regulated at the highest set point among the parallel connected power supplies.

Using the automatic master method ensures the fault tolerance of the system. In case the master would fail, any one of the other units can take control of the bus based on the same selection criteria discussed in the previous paragraph.

The democratic load sharing

Democratic load sharing can be implemented with another minor variation on the automatic master slave implementation changing the ideal diode to a resistor as illustrated in Fig. 27.

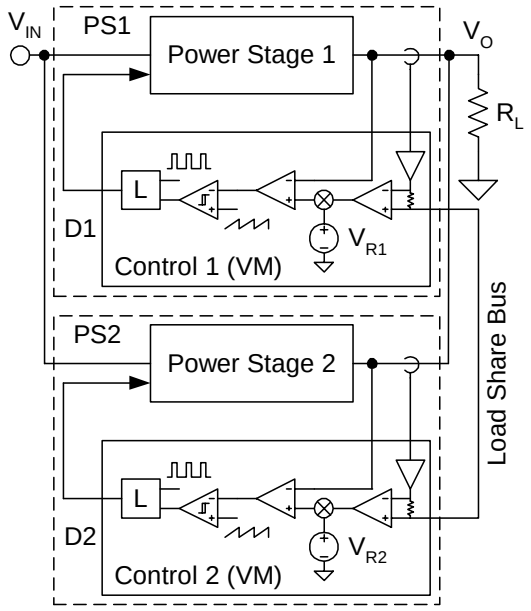

Fig. 27. Example of the democratic load share theory.

When a resistor is used between the two inputs of the load share error amplifier the bus becomes the true representation of the average current in the system. Due to the high gain of the error amplifier the system is in balance when the voltages across the resistors become zero. That happens when all modules measure the same output current.

A unique property of the democratic load share system is that not only the output current levels but also the output voltage of the system is determined by "voting". If the voltage error amplifier is allowed to adjust bi-directionally the individual output voltage set points of the modules are weighted. Initially higher output voltages are adjusted lower while the initially lower ones are getting raised until the desired current balance is established. Accordingly, the system output voltage might be closer to the nominal output voltage of the system than any of the module output voltages connected parallel.

Although democratic load share provides perfect balance for currents and system output voltage during normal operation it fails to provide fault tolerance. When a power supply fails or disabled, its output current is zero. Unless it is removed from the "democratic voting" scheme it can falsify the average current information on the load share bus. This phenomenon is highlighted in Fig. 28.

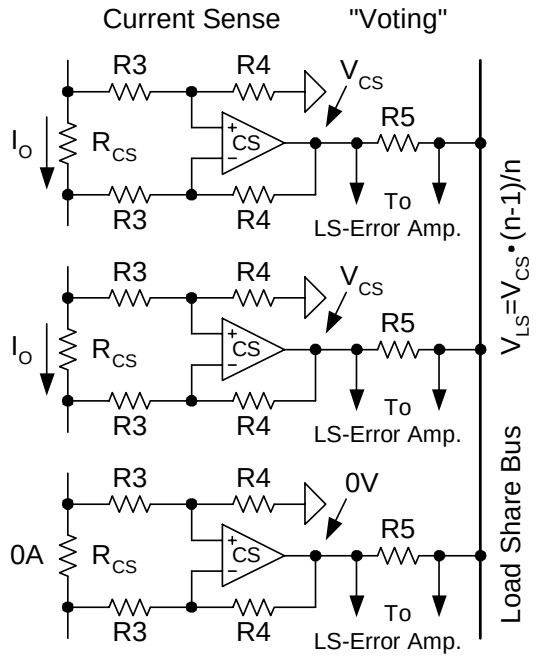

Fig. 28. The effect of faulty module in democratic load share system.

Practically the faulty module drags down the bus. The measured output current is always higher than the average representation on the bus causing all the active load share error amplifiers to saturate and the current sharing to fail. The solution is to disconnect the faulty power supply from the "voting" which will restore the load share operation for the rest of the system.

Active load share error components

All three active load share circuits comprise the same building blocks therefore they can be analyzed the same way. These sub-circuits are the current sense amplifier, the load share error amplifier and the bus driver circuit which might be slightly different depending on the load share mechanism.

The current sense amplifier provides a user programmable gain stage to scale the signal present across the current sense resistor. It is desirable to work with the highest possible load share bus voltage to minimize the inaccuracies due to the input offset of the load share error amplifier and the possible ground potential difference among the load share controllers. The current sense measurement error can be analyzed based on the schematic diagram of a true differential amplifier schematic in Fig. 29.

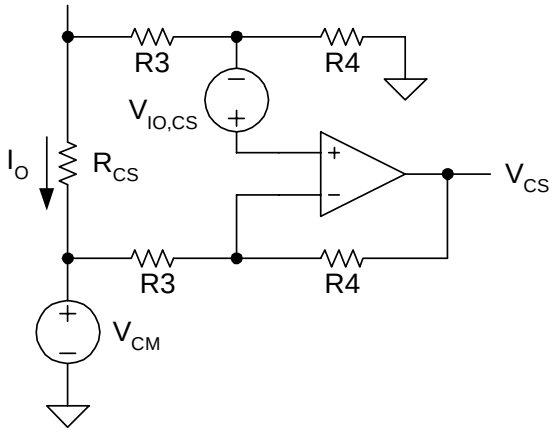

Fig. 29. Generalized current measurement circuit.

The two inputs of the high gain operational amplifier are at the same potential which voltages can be expressed as:

$$V_{CS} + (V_{CM} - V_{CS}) \cdot \frac{R4}{R3 + R4} =$$

$$(V_{CM} + I_O \cdot R_{CS}) \cdot \frac{R4}{R3 + R4} + V_{IO,CS}$$

After rearranging the equation for Vcs and carrying out the error analysis to determine the effect of resistor mismatch, the output voltage of the current sense amplifier can be found as:

$$V_{CS} = (1 + 2 \cdot \%R) \cdot G \cdot I_O \cdot R_{CS} +$$

$$(1 + G + 2 \cdot G \cdot \%R) \cdot V_{IO,CS} + \frac{4 \cdot G \cdot \%R}{G + 1} \cdot V_{CM}$$

where %R is the tolerance of the resistors in decimal format (0.01 corresponds to a 1% resistor) and G is the current sense gain defined as $G = \frac{R4}{R3}$. Four error components can be recognized by close examination of the equation. These errors are caused by the resistor mismatch around the amplifier, by the current sense resistor tolerance and by the input offset voltage of the amplifier. They can be calculated using the following equations:

$$\%E1 = \frac{4 \cdot \%R}{(G+1) \cdot I_O \cdot R_{CS}} \cdot V_{CM}$$

$$\%E2 = 2 \cdot \%R$$

$$\%E3 = \%R_{CS}$$

$$\%E4 = \frac{(1 + G + 2 \cdot G \cdot \%R) \cdot V_{IO,CS}}{G \cdot I_O \cdot R_{CS}}$$

Resistor mismatch around the amplifier allows a portion of the common mode voltage to appear at the output of the current sense amplifier. The first expression compares this voltage to the real current sense output to determine the error in percentages. This is probably the most significant error in the current sense circuit when the current sense resistor is not ground referenced. The equation shows a fixed voltage contribution to the current sense output which will result in a gradually decreasing percentage error as the load current increases. To minimize this error, it is desirable to increase the gain around the amplifier as the constant error voltage becomes a smaller percentage compared to the real signal. In other words, the full scale current sense voltage should be maximized. Even more important is to use very accurate resistors in this amplifier stage. For precise high side current sensing 0.1% resistors are desirable.

The second equation gives the gain error due to the resistor mismatch. This error is a constant percentage over the entire load range and it can be mitigated by using accurate resistors.

The tolerance of the current sense resistor is another error source impacting the accuracy directly. In addition to selecting a low tolerance current sense resistor, it is important to pay attention to the printed circuit board layout. It is imperative to use a Kelvin type connection where voltage drop on PCB copper traces are not part of the sensed signal.

The fourth component is the percentage error contribution of the gained-up input offset voltage with respect to the accurate current sense output signal. Since the gain of the current sense circuit can not be reduced due to other considerations mentioned earlier, the designer's only remedy to minimize this error is to chose a low offset amplifier.

$$\%E_{CS}(I_O) = \%E1 + \%E2 + \%E3 + \%E4$$

The worst case current sense error is the sum of the four error components and it is a function of the actual load current of the module. Both %E1 and %E4 errors go to infinity as the load current approaches zero due to Io appearing in the denominator of their respective equations.

The load share error amplifier of the active load share system compares two current sense signals to generate the load share error signal. The typical circuit implementation is pictured in Fig. 30.

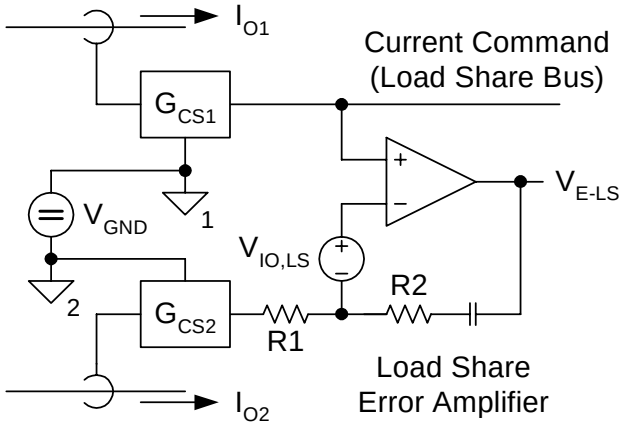

Fig. 30. Load share error amplifier circuit.

This circuit is a general purpose negative feedback amplifier similar to the voltage error amplifier which is used to regulate the output voltage of the power supply. The reference voltage level at the non-inverting input of the operational amplifier is taken from the load share bus which voltage corresponds to the desired average output current of the module. There are two load share specific concerns highlighted in Fig. 30.

One problem is related to the operation of the master module, which drives the load share bus. In this case the load share bus voltage and the current sense signal at the inverting input of the error amplifier are at the same potential and the output of the error amplifier is defined by the polarity of its input bias voltage. According to the offset polarity, the amplifier would be forced either to the maximum error level or to zero. Since the output voltage adjustment is proportional to the error amplitude, the maximum error signal would force the master module to the end of the adjustment range. This is not acceptable for two reasons: the output voltage might be out of tolerance and the slave modules would not have enough adjustment range left to achieve balanced current distribution. Accordingly, the input offset polarity and amplitude of the load share error amplifier must be pre-conditioned to ensure that the output voltage of the master module preserves its original output voltage set point. Since a minimum offset must be guaranteed for proper operation, the $V_{IO,LS}$ of this amplifier is significantly higher than the usual input offset of an operational amplifier and it is given in the data sheets of the integrated load share controllers.

The other issue is the voltage differential between the grounds of the current measurement circuits which is emphasized by the V_{GND} voltage source in Fig. 30. Since the current sense amplifiers are connected to the local grounds of the modules, any voltage between the respective grounds can cause additional error in current distribution especially at higher output currents due to resistive voltage drops in the ground connections. The obvious solution to eliminate this problem is the carefully designed ground system where the resistive voltage drops are kept at minimum.

Both of these effects influence the ultimate accuracy of the system. The accrued error at the error amplifier inputs can be easily analyzed based on the schematic diagram of Fig. 30. Until the load share error amplifier stays in its active linear operating mode, the input voltages are equal:

$$V_{CS1} = V_{CS2} + V_{IO,LS} + V_{GND}$$

From this equation the error can be determined as the ratio of the sum of V_{IO} and V_{GND} to the current sense signal:

$$\%E_{LS-EA} = \frac{V_{IO,LS} + V_{GND}}{V_{CS2}}$$

where V_{CS2} is a function of the output current according to:

$$V_{CS2} = \frac{V_{CS2,\max}}{I_{O2,\max}} \cdot I_{O2}$$

In this expression $V_{CS2,MAX}$ is the maximum or full scale current sense signal amplitude set by the gain of the current sense circuitry and $I_{O2,MAX}$ is the maximum output current of the module. Substituting V_{CS2} into the previous equation for error yields:

$$\%E_{LS-EA} = \frac{\left(V_{IO,LS} + V_{GND}\right) \cdot I_{O2,\max}}{V_{CS2,\max} \cdot I_{O2}}$$

This error term further accentuates the importance of maximizing the full scale load share bus voltage. While V_{GND} can be a current dependent component causing a fixed percentage error, $V_{IO,LS}$ is a constant and its effect is minimized if it is compared to a higher current sense signal. Also note that similarly to the effect of other error sources in the current sense circuit, the percentage error accumulated at the load share error amplifier diminishes as the output current increases.

The total error in an active load share system can be found as the sum of the current sense errors and the error amplifier's contribution:

$$\%E_{ALS} = 2 \cdot \%E_{CS} + \%E_{LS-EA}$$

Because the error amplifier compares two measured current sense signals, the measurement error, $\%E_{CS}$ had to be multiplied by two.

The last difficulty to consider with respect to the active load share technique is the stability of the additional negative feedback loop introduced by the load share error amplifier. Fig. 31 shows the addition of the load share control loop to the existing control functions of a power supply.

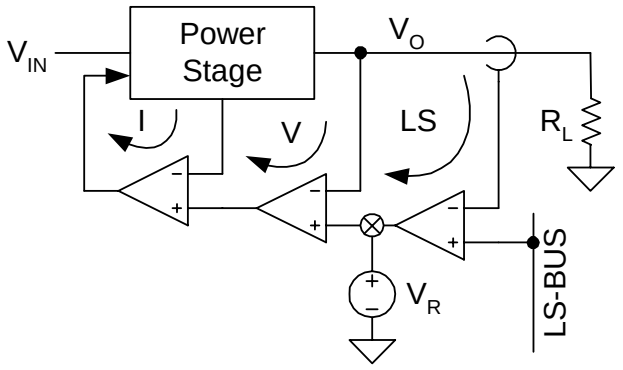

Fig. 31. Control loops in a power supply with active load sharing.

In this example three loops are utilized, an inner current loop, either peak or average current mode control, an output voltage regulation loop and finally an outside load share control loop. Since the load share loop is added to an existing voltage control loop interaction between the feedback systems must be avoided. Therefore, the crossover frequencies of the three loops must be well separated.

The primary concern for load sharing is to provide redundancy and increased long term reliability, i.e. aging, through balanced thermal stresses. Consequently, relatively slow acting corrective measures by the load share loop is completely acceptable. Since the performance of the voltage regulation loop is imperative to achieve precise output voltage regulation and fast transient response, it is desirable to maximize its gain bandwidth. The load share loop bandwidth then can be chosen such that it does not interfere with the operation of the voltage loop. It is usually ensured by designing the load share loop crossover frequency at least an order of magnitude lower than the voltage loop crossover frequency.

In order to compensate the load share error amplifier properly, the gain blocks of the load share loop must be identified.

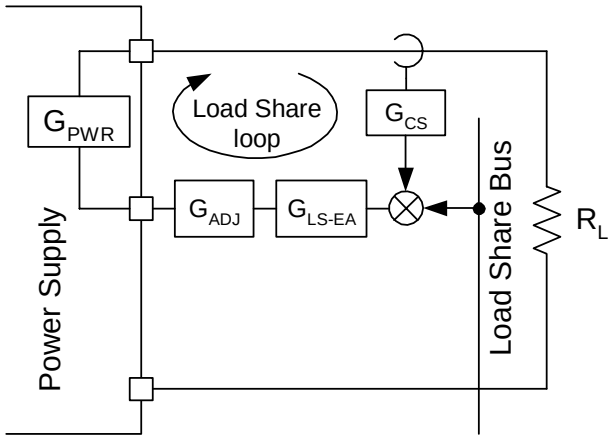

Fig. 32. Gain blocks representation in active current sharing control loop.

The control loop comprises of the current sense gain block, the load share error amplifier, the adjust gain block and the gain describing the response of the power supply to the control parameter provided by the load share circuit. Accordingly, the small signal closed loop transfer function of the load share controller is:

$$G_{LS}(s) = G_{PWR}(s) \cdot G_{CS} \cdot G_{LS-EA}(s) \cdot G_{ADJ}$$

The transfer functions of G_{CS}, G_{ADJ}, and G_{PWR} needs to be determined for the 0.1Hz to 10 kHz frequency range. In the majority of the designs the load share loop crossover frequency is expected to be within these frequency limits.

The current sense amplifier gain is selected to minimize power dissipation, in addition to the current sense and load share errors. The full scale load share voltage should utilize the full voltage swing capability of the operational amplifier. This is usually limited by the bias level and the input voltage range of the load share error amplifier. The gain of the current sense amplifier is constant in the frequency range of interest. Assuming a maximum allowable power dissipation (P_{CS}) for the current sense resistor dictated by efficiency considerations, the maximum value R_{CS} is given as:

$$R_{CS,MAX} = \frac{P_{CS}}{I_{O,MAX}^2}$$

If the full scale load share bus voltage is $V_{CS,MAX}$, the current sense gain is established as:

$$G_{CS} = \frac{V_{CS,MAX}}{I_{O,MAX} \cdot R_{CS}}$$

The next step is to calculate the adjust gain based on the maximum output voltage adjustment range, ΔV_O. Usually, the full useful output voltage swing of the load share error amplifier corresponds to the maximum adjustment allowed for the design. Accordingly,

$$G_{ADJ} = \frac{\Delta V_O}{\Delta V_{LS-EA}}$$

Notice the need for the transfer function between the load share adjust input and output current of the power supply. This parameter is usually not readily available especially when load share is added to systems utilizing parallel combination of off-the-shelf power modules. In these cases the transfer function must be measured and a matching arithmetical representation must be derived. Fig. 33 introduces the expected transfer function between the adjust input and the output voltage of the power supply.

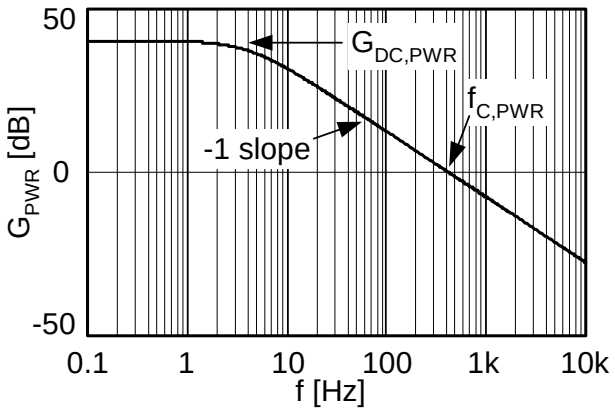

Fig. 33. Typical adjust / sense to output transfer function.

From the measured dc gain in dB ($G_{DC,PWR}$) and crossover frequency ($f_{C,PWR}$) the transfer function can be defined in algebraic form. The dominant pole is:

$$f_P = \frac{f_{C,PWR}}{10^{\left(\frac{G_{DC,PWR}}{20}\right)}}$$

and the real gain – not in dB – equals:

$$G_{0,PWR} = 10^{\left(\frac{G_{DC,PWR}}{20}\right)}$$

The transfer function in the complex frequency domain between the sense input and the output current can be written as:

$$G_{PWR}(s) = \frac{G_{0,PWR}}{1 + \frac{s}{2 \cdot \pi \cdot f_P}} \cdot \frac{R_{CS}}{R_L}$$

After obtaining the $G_{PWR}(s)$ transfer function, the procedure continues by calculating the desired compensation around the load share error amplifier. Placing the load share loop crossover frequency at least a decade lower than $f_{C,PWR}$ ensures the desired separation between the voltage feedback and load share control loops.

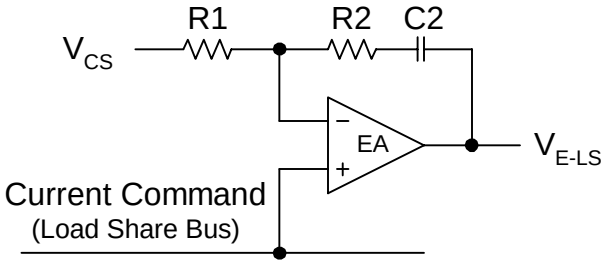

Fig. 34. Recommended load share error amplifier configuration.

Using $f_{C,LS} = 0.1 \cdot f_{C,PWR}$ as a design guideline, the required gain of the load share amplifier can be defined. At this time all other components in the closed loop transfer function are known and their combined gain can be calculated at the desired load share loop crossover frequency, $f_{C,LS}$. This defines the gain of the load share error amplifier at $f_{C,LS}$ as:

$$G_{LS-EA}(f_{C,LS}) = \frac{1}{G_{CS} \cdot G_{ADJ} \cdot G_{PWR}(f_{C,LS})}$$

Using the component references of Fig. 34 this gain can be set by R2 and R1 resistors according to:

$$G_{LS-EA}(f_{C,LS}) = \frac{R2}{R1}$$

To improve load share accuracy in steady state operation, the low frequency gain of the load share error can be increased by adding a pole to the feedback network. The pole can be placed at the desired load share loop crossover frequency or below which defines a minimum value for C2:

$$C2_{MIN} = \frac{1}{2 \cdot \pi \cdot f_{C,LS} \cdot R2}$$

To summarize the result of the load share error amplifier design procedure, a typical Bode representation of the complete system is given in Fig. 35.

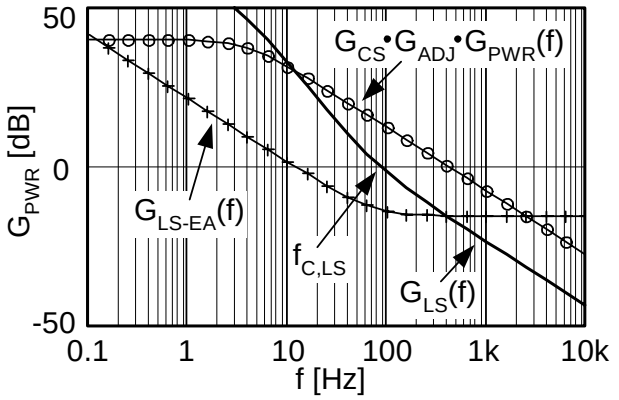

Fig. 35. Bode plot of the compensated load share control loop.

By closing the feedback loop around the load share error amplifier the active load share design procedure is completed. Since the active load share controller can be implemented in many different ways, some of the gain equations might have to be revisited as the circuit changes. For example, in integrated load share controllers the error amplifier is often implemented by a *gm* type amplifier instead of an operational amplifier shown in Fig. 34. These minor circuit modifications do not change the essence of the calculation method although they might result in a change of the actual numerical expressions.

IV. ACCURACY COMPARISON

In this final chapter the expected accuracies of the different load share techniques are calculated and compared. In order to fairly assess the expected performance of the systems a common power stage will be used for all the different load share techniques.

In these examples, two 12V input, 3.3V / 20A output, non-isolated modules provide 40A load current to a common load. The analysis will determine the load share accuracy at half load and full load and the maximum required current rating of the modules based on the current distribution error. The calculations can be easily adopted to any number of units, because the calculated maximum error always corresponds to the worst case situation. In worst case, the two modules at the opposite extreme tolerance points are compared and all the other modules must fall within the calculated error band.

The generalized power stage and its parasitic elements are given in Fig. 36.

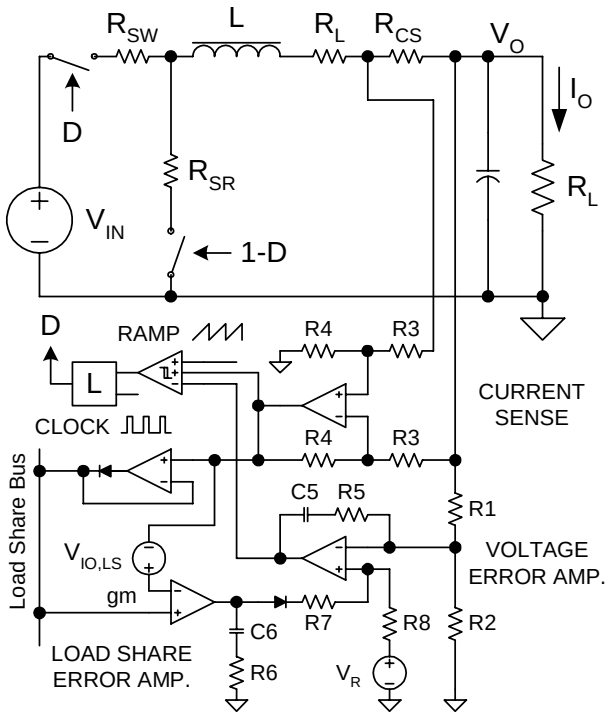

Fig. 36. Universal circuit diagram for accuracy calculations.

To carry out the calculations the following numerical values are assumed:

Operating Parameters		
Parameter	**Value**	**Tolerance**
V_{IN}	12V	
$V_{O,NOM}$	3.3V	+/-3%
V_{BIAS}	5V	
V_{OH}	4.5V	
ΔV_{EA}	3.8V	
V_R	1.25V	+/-0.5%
V_{CL}	0.15V	+/-1%
$I_{LOAD,MAX}$	40A	
$I_{O,MAX}$	20A	
F_{SW}	200kHz	
D	0.275	

Controller characteristics		
Parameter	**Value**	**Tolerance**
V_{CM}	3.3V	
$V_{IO,CS}$	+/-300µV	
$V_{IO,EA}$	+/-1.5mV	
$V_{IO,PWM}$	+/-15mV	
$V_{IO,LS}$	30mV	+/-15%
V_{GND}	+/-5mV	

Component Values		
Label	**Value**	**Tolerance**
L	3µH	+/-10%
R_{IND}	0.5mΩ	
R_{LOAD}	165mΩ	
R_{SW}	10mΩ	
R_{SR}	5mΩ	
R_{CS}	6mΩ	+/-1%
ALL RS		+/-0.1%

A. Calculating feedback divider and set point accuracy

The first step is to calculate the output voltage set point and its accuracy. After selecting R2=10kΩ, R1 can be calculated.

$$R1 = R2 \cdot \frac{V_{O,NOM} - V_R}{V_R}$$

$$R1 = 10k\Omega \cdot \frac{3.3V - 1.25V}{1.25V} = 16.4k\Omega$$

which value is available from the E-192 (0.1%) resistor value series. Accordingly the output voltage can be set to exactly 3.3V. The tolerance of the set point is:

$$\%E_{SET} = \%E_{VR} + \frac{V_{IO,EA} + V_{GND}}{V_R} + \frac{2}{1 + \frac{R2}{R1}} \cdot \%R$$

$$\%E_{SET} = 0.005 + \frac{0.0015 + 0.005}{1.25} + \frac{2}{1 + \frac{10}{16.4}} \cdot 0.001 = 0.011$$

Based on the calculated 1.1% set point accuracy, the output voltage will fall in the $3.262V<V_O<3.338V$ range.

B. Defining the maximum output impedance in droop current sharing

To minimize the load share error using the droop technique it is desirable to maximize the output impedance of the power supplies. For this calculation the output error budget must be considered. Fig. 37 shows the allowable output voltage window based on the output voltage specification.

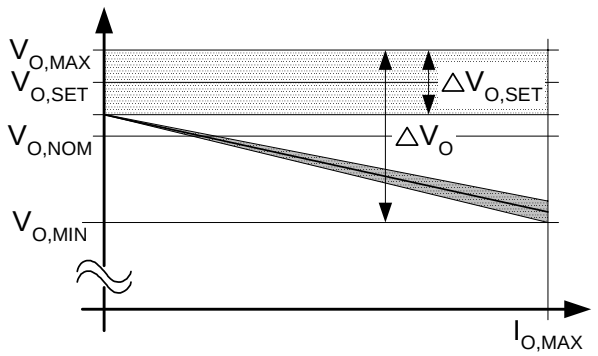

Fig. 37. Output voltage regulation budget.

As the graph indicates, the output voltage should be set to the highest initial value which still guarantees that the output stays within the regulation window considering the set point tolerance. Accordingly, the maximum value of the output impedance is:

$$R_{O,MAX} = \frac{\Delta V_O - \Delta V_{O,SET}}{I_{O,MAX}}$$

$$R_{O,MAX} = \frac{0.198V - 0.076V}{20A} = 6.124m\Omega$$

To account for set point resolution and component tolerance errors R_O= 6mΩ output impedance is selected for the design.

It is important to notice that droop method only works if $\Delta V_{O,SET}$ is less than half of the total output voltage window, ΔV_O. Otherwise, there is no common output voltage level which would cross the two worst case load lines simultaneously. That means one of the supplies could go into current limit before the other one would contribute to the load current. Consequently, it is necessary to set the output voltage very precisely when the droop load share technique is considered. That also allows a higher module output impedance which further improves the load share accuracy of the system.

C. Calculating current sense accuracy

When the current sense circuit is designed the goal is to fully utilize the available signal amplitude at the output of the current sense amplifier in Fig. 36. The current sense gain is then limited by the available voltage swing at the output of the current sense amplifier and the maximum voltage across the sense resistor.

$$G_{CS} = \frac{R4}{R3} = \frac{V_{OH}}{I_{O,MAX} \cdot R_{CS}}$$

$$G_{CS} = \frac{4.5V}{20A \cdot 6m\Omega} = 37.5$$

After this gain is finalized, the current sense error can be calculated. There are four error components; common mode voltage, input offset, gain and sense resistor errors as explained with respect to Fig. 29. Since some of the errors are the function of the module's output current, the current measurement error can not be characterized by a single number. Using the numerical values of the example circuit the result is given in Fig. 38.

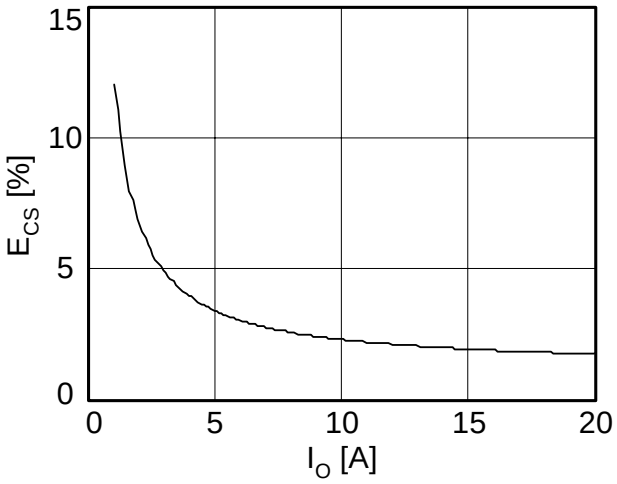

Fig. 38. Current sense error as a function of output current.

At light load accurate current sensing is rather difficult because the useful signal becomes very small. On the other hand, input offset and common mode voltage errors are independent of the load current therefore their effect start dominating the measurement result. As a result the error increases exponentially at lower current level. While the percentage error is large, the current difference among the modules remains relatively constant and in most cases negligible.

D. Current limit accuracy example

Although sharing the load current with power supplies operated in their current limit mode is really not practical, the analysis of the current limit accuracy can be useful to determine stresses and minimum margins during the design procedure. The 150mV current limit reference allows I_{PK}=25A peak current across the 6mΩ current sense resistor. The output inductor's ripple current was designed for $4A_{P-P}$ therefore the nominal short circuit current is I_{CL}=23A.

To find the tolerance of this current value four error components must be determined. The first one is the tolerance of the current limit reference itself which is given in the controller characteristics table. In integrated PWM controllers the current limit reference is usually less accurate than the voltage reference because the trimming is performed at the voltage reference.

$$\%E_{Vcl} = 0.01$$

The next error term is related to the input offset of the PWM or current limit comparator. Depending on the particular implementation, any of these comparators can be used in current limit operation. This offset is listed as $V_{IO,PWM}$ in the table and its effect on the current limit accuracy is:

$$\%E_{Vio,pwm} = \frac{V_{IO,PWM}}{I_{PK} \cdot R_{CS}}$$

$$\%E_{Vio,pwm} = \frac{0.015V}{25A \cdot 6m\Omega} = 0.1$$

Since the current limit circuit uses the peak current information, the effect of the output inductor tolerance on the peak to average current error must be considered also.

This error is calculated as:

$$\%E_L = \frac{V_{IN} \cdot D}{2 \cdot L \cdot I_{CL} \cdot f_{SW}} \cdot \%L$$

$$\%E_L = \frac{12V \cdot 0.275}{2 \cdot 3\mu H \cdot 23A \cdot 200kHz} \cdot 0.1 = 0.012$$

Lastly the tolerance of the current sense resistor has to be taken into account. It is listed in the component table:

$$\%E_{Rcs} = 0.01$$

The worst case error than can be found as the sum of the four error components which gives a total current limit tolerance of 13.2%. This accuracy number clearly explains the common design practice, where the current limit is usually placed 10% to 20% above the expected highest load current value.

E. Case studies

The following accuracy calculations are obtained from the equations derived in the previous part of the paper. Due to the tedious nature of the numerical substitutions the details of the calculations are not shown. The descriptions, assumptions and final load share accuracy results are summarized in the table below.

Case #	Technique	Comments / Assumptions	Error [%]		$I_{O,MAX}$ [A]
			Half load	Full load	
1	Distributed duty ratio	Assumes 20ns (ΔD=0.004 or 1.4% of D_{NOM}) timing mismatch	18.6	9.3	21.9
2	Distributed error signal	Error signal is divided down locally to PWM comparator	20.7	10.8	22.2
3	Droop with series resistor	Using R_{CS} as the droop resistor, placed outside the feedback loop	65.1	33.1	26.6
4	Droop w/ current ffwd	Using R_{CS} inside the feedback loop to measure output current	65.5	33.5	26.7
5	Droop w/ limited gain EA	Using R_{CS} for peak current mode control and current measurement	55.9	28.6	25.7
6	Active current share	Automatic master/slave method, parameters based on UCC39002	6.1	4.3	20.9

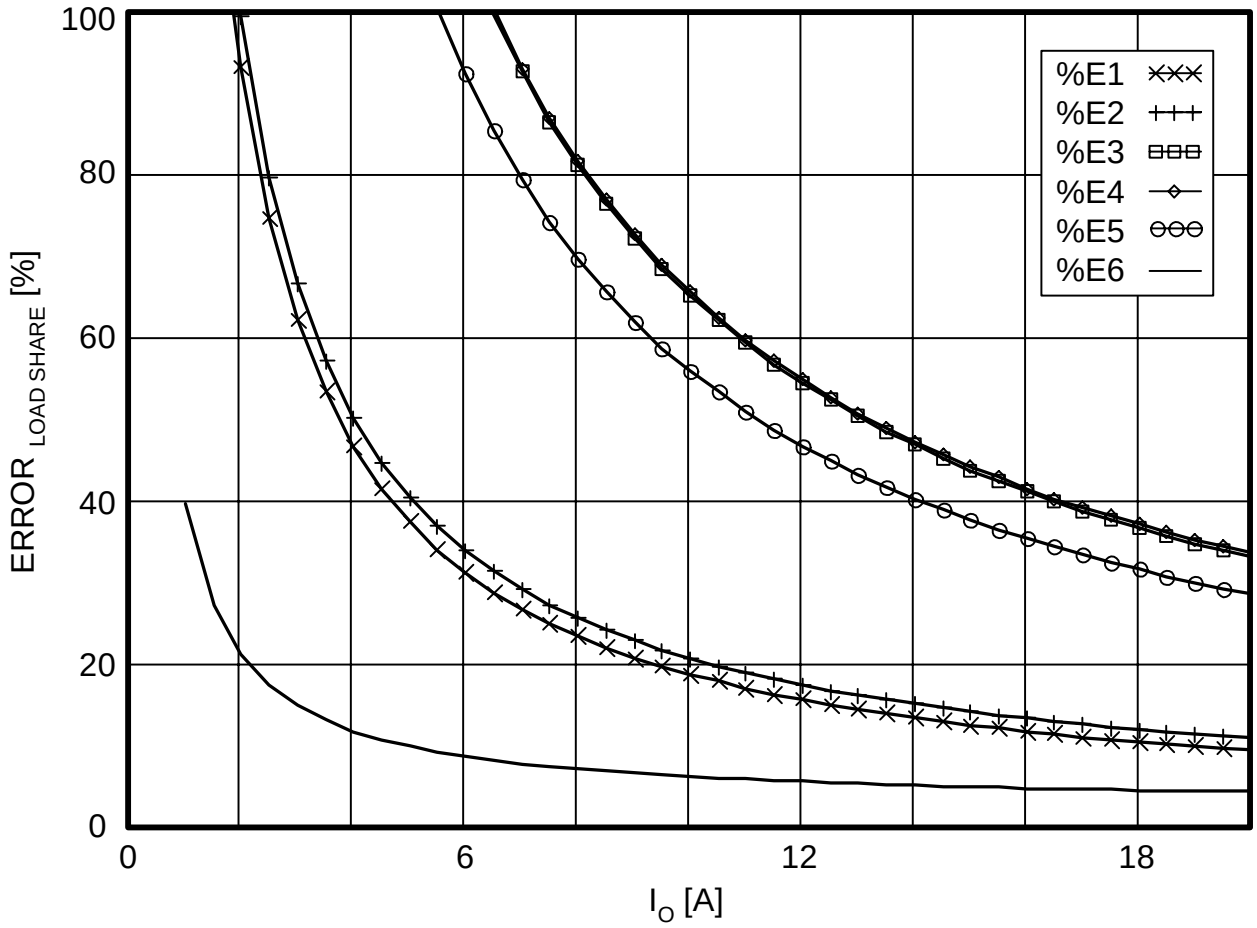

Fig. 39. Current share errors as a function of the module's output current.

As it could be seen in Fig. 38 earlier, the current share errors vary significantly by the output current. For completeness, Fig. 39 shows the total load share errors for the six examples listed in the table.

The trends clearly show that at light load accuracy suffers independently from the selected technique due to various fixed error contributions which are getting larger and larger compared to the current signal as the load decreases. The active load share technique is the one which maintains the highest degree of accuracy at relatively light load. The next group of curves offering medium accuracy correspond to the parallel power stage approaches where either the duty ratio or the error signal is distributed among the parallel connected circuits. The disadvantages are the lack of true redundancy and modularity and the sensitivity to single point failure. In addition, distribution of the sensitive error signal or the high speed PWM command with reasonable accuracy might be troublesome in larger systems. The simplest droop method does not require any communication between the modules, but it is extremely sensitive to component tolerances especially to set point accuracy of the output voltage. Quite often the droop load share technique requires less than 0.5% initial voltage set point accuracy. In most low voltage applications – 2.5V and below – the droop method imposes impractical accuracy requirements.

V. SUMMARY

This paper has strived to give a detailed overview of the most fundamental load share principles and their applications for parallel power processing solutions. The intricate effects of circuit parameters and parasitic elements were outlined. The methods used in the analysis can be applied to evaluate other load share circuits.

Some of the calculations needed to analyze the load share performance have value in general circuit design practice to better understand the effect of component tolerances on output voltage regulation and current limit accuracy in power supplies.

Additional information of many different load share implementations are discussed in various application notes from Texas Instruments and in the literature. Many of the most recommended papers are listed in the reference section.

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