Under the Hood of Flyback SMPS Designs

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ABSTRACT

A basic review of the flyback switching topology will be presented with an emphasis on not-so-obvious design issues, such as effects of parasitics, fault protection, and EMI mitigation. Modeling and analysis will be demonstrated and compared with physical hardware measurements. A major subtopic will be the operation and characterization of the flyback transformer — considering leakage inductance, cross-regulation, parasitic capacitance, and other performance-defining parameters.

I. INTRODUCTION

Given its simplicity, ease of design and low cost, the flyback converter is probably the most popular power-supply topology for low-power applications. Its transformer combines the actions of an isolating transformer and an output inductor into a single element, while being capable of providing multiple voltage outputs. For many designers, however, the flyback topology is synonymous with low performance, low efficiency and poor cross-regulation. To operate this topology to its full potential, many of its not-so-obvious subtleties need to be well understood.

This topic addresses a few basics of the flyback topology, and then goes into details regarding the following subjects:

- Understanding the flyback transformer and its impact on power-supply performance—The effects of leakage inductance, cross-regulation, parasitic capacitances, and winding strategy as it affects cross-regulation, short-circuit behavior, and efficiency.
- Flyback power-supply current limiting—The influence of parasitics and feedforward.
- EMI and line rejection—Minimizing EMI in flyback applications and the impact of feedforward on line rejection.
- Snubbers and clamp circuits—Resistor-capacitor-diode (RCD) clamp, a non-dissipative clamp, and secondary-side snubbers.

For most of these subjects, mathematical models are used during analysis. Test results are also provided for a 48-V to 5-V, DC/DC-converter design with the TPS23754 flyback controller, switching at 250 kHz and capable of powering a 0- to 25-W load.

II. FUNDAMENTALS OF FLYBACK POWER-SUPPLY DESIGN

A. Transfer of Energy

A flyback converter operates by first storing energy from an input source into the transformer while the primary power switch is on. When the switch turns off, the transformer voltage reverses, forward-biasing the output catch diode(s) and delivering energy to the output(s).

With a flyback topology, an output can be positive or negative (defined by a transformer polarity dot). There are two basic energy-transfer modes of operation. The first one is continuous conduction mode (CCM), in which part of the energy stored in the flyback transformer remains in the transformer when the next ON period begins. The second mode is discontinuous conduction mode (DCM), in which all of the energy stored in the transformer is transferred to the load during the OFF period.

Critical conduction mode (CRM) is a third mode, also called transition mode (TM), which is just at the boundary between DCM and CCM,

occurring when the stored energy just reaches zero at the end of the switching period.

Figs. 1 and 2 illustrate CCM, DCM, and TM operation. Fig. 3 illustrates the current flow in CCM and DCM operation.

With DCM operation, when the primary MOSFET turns on, the primary current starts at zero and rises to a peak value that can be more than twice the peak current in a comparable CCM application. At turn off, the ampere-turns transfer to the secondary and the secondary current decreases to zero where, it remains until the beginning of the next switching cycle. A flyback transformer designed for DCM operation requires a smaller inductance value than one designed for CCM operation, since the current ripple (ΔI_L) is much higher. In some applications, lower inductance may result in a physically smaller transformer; assuming the efficiency and thermal performance remain acceptable.

TM operation is similar to DCM except that the primary MOSFET turns on at the moment the drain voltage is at its minimum level. This timing offers minimum turn-on loss and a more efficient operation, however, the switching frequency is variable.

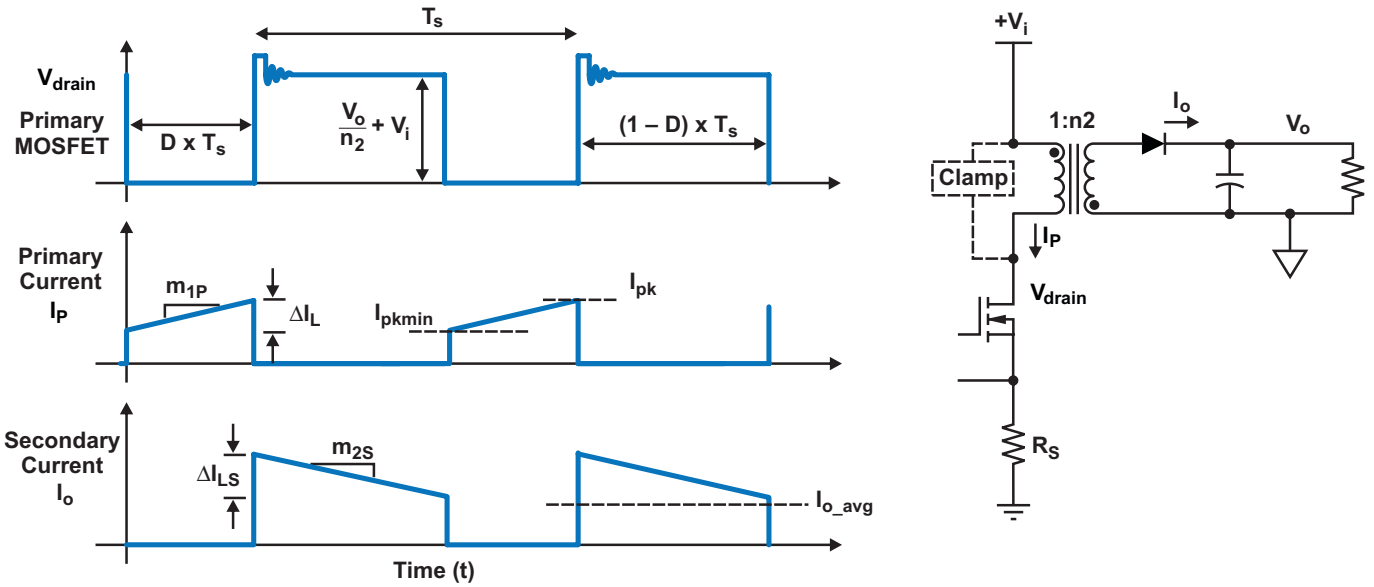


Fig. 1. Operation in CCM.

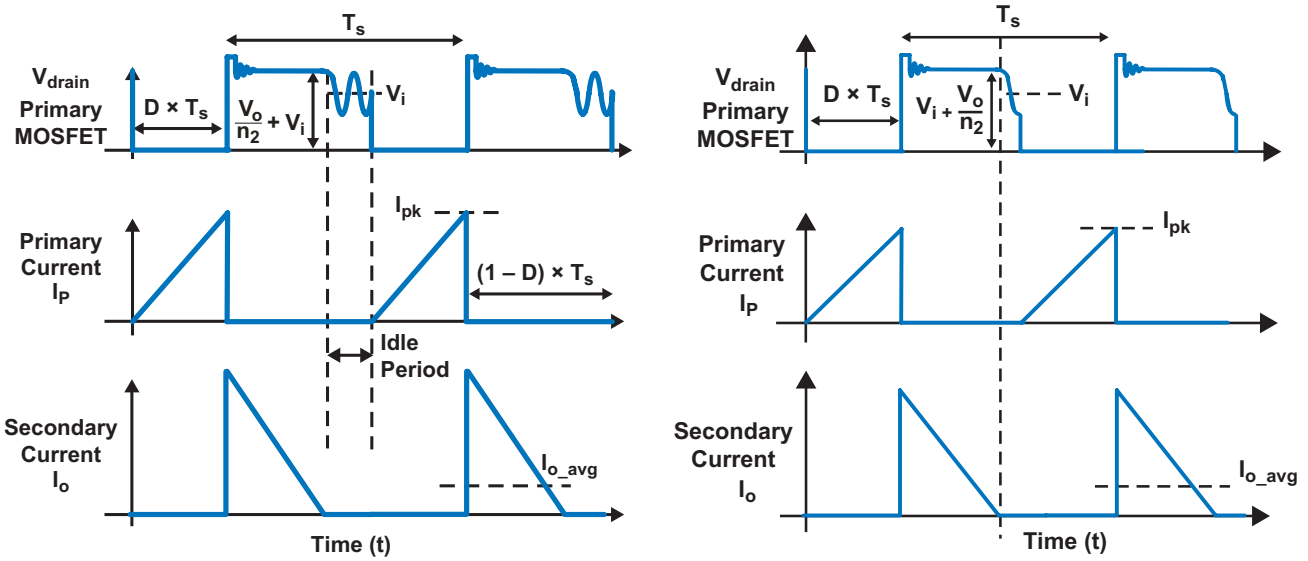


Fig. 2. Operation in DCM (left) and TM (right).

With CCM operation, the inductance value is large and the ripple component of the current and magnetic field is relatively small. The following limits are a good working compromise for acceptable primary peak current.

$$35\% \le \frac{I_{pk\,min}}{I_{pk}} \le 50\%$$

This can also be used to define an appropriate trade-off between efficiency and transformer size.

Neglecting the losses while the primary MOSFET is on (see Fig. 1), the primary current increases at a rate defined as

$$m_1 = \frac{\Delta I_L}{D \times T_S} = \frac{V_i}{L}, \quad (1)$$

where V_i is the input voltage, L is the inductance value measured at the primary of the transformer, I_L is the current circulating through the primary (see I_P in Fig. 1), and T_S is the time period of one switching cycle.

Following the same assumptions, while the primary MOSFET is off and the transformer current has been transferred to its secondary winding, the secondary current decreases at a rate defined with Equation (2) unless it becomes discontinuous:

$$m_{2S} = \frac{\Delta I_{LS}}{(1-D) \times T_S} = \frac{V_o}{L \times {n_2}^2}, \quad (2)$$

where V_o is the output voltage, $n_2 = N2/N1$ and I_{LS} is the secondary magnetizing current (see I_o in Fig. 2) .

Note that the coupling between the primary and secondary sides of a flyback transformer is imperfect because there is leakage inductance between them. During commutation from primary to secondary, the leakage energy cannot be directly transferred to the secondary and consequently must be absorbed. Without a clamp circuit, the only path the leakage-inductance current can circulate is by charging the parasitic drain-to-source capacitance of the MOSFET. If precautions are not taken, the MOSFET switch can be destroyed by voltage breakdown. Fig. 3 shows a generic clamp circuit example. Later in Section VI, several clamp circuits are presented and explained.

Note the discontinuous nature of the current on each side of the transformer, in CCM, DCM, and TM. This is a fundamental difference when compared to other transformerless topologies like buck or boost. The high ripple current on both sides of the transformer directly impacts the output voltage ripple, the efficiency, and the differential-mode conducted EMI.

Also, although there is current discontinuity on both sides of the transformer, operating in CCM generally results in better efficiency than operating in DCM. The higher rms current in DCM is one reason supporting this fact, as it means a higher dissipation in the MOSFET, the

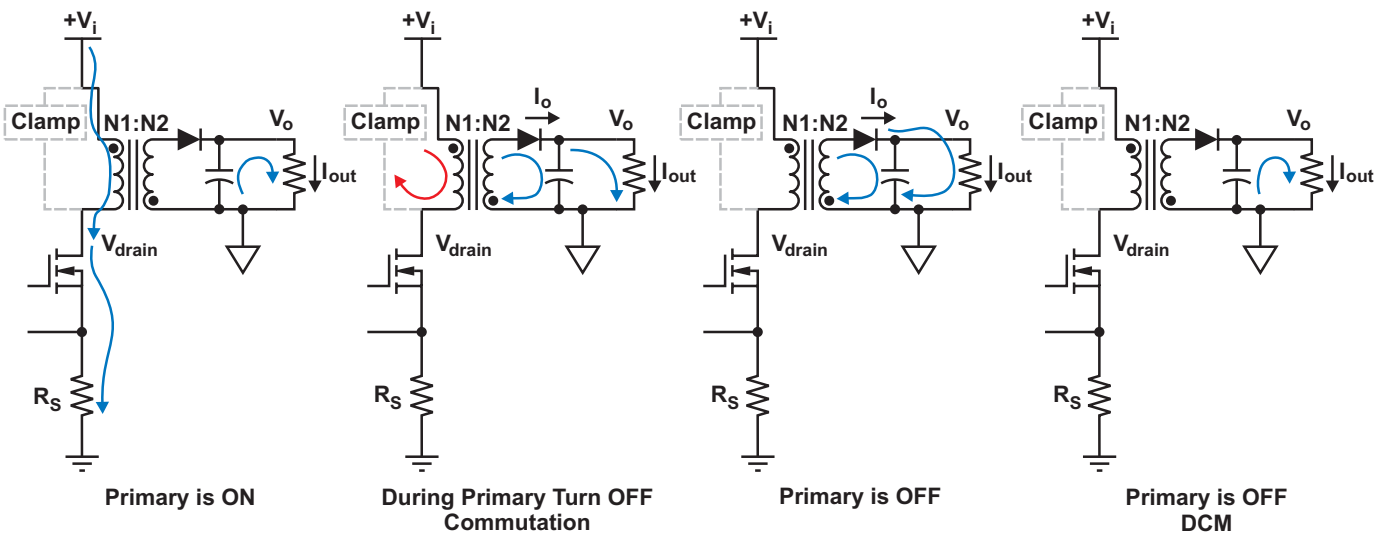


Fig. 3. Current flow in the flyback power stage.

primary and secondary capacitors, and the primary clamp. However, because the inductance value is lower for DCM operation, a transformer that is the same physical size may have less conduction loss for DCM operation than if it was designed for CCM operation, even if its rms current is higher. In some AC-line applications and operating conditions, TM operation may be able to provide similar or even better efficiency than CCM. Core loss must also be considered when operating in DCM (and TM), given the large AC component of the magnetic field. CCM operation usually corresponds to a lower AC magnetic field; thus, the main limitation when designing the transformer becomes core saturation rather than core losses.

While in DCM, transferred energy is dictated by ON time, input voltage, and inductance value. There is always a complete energy transfer during every cycle, defined by:

$$P_{DCM} = \frac{V_i^2 \times D^2}{2L \times Freq}, \quad (3)$$

where P_{DCM} is the load power while in DCM, L is the inductance value measured at primary of the transformer, D is the control-switch duty cycle, and Freq is the switching frequency.

This also means that in DCM, the following duty-cycle equation depends on the load current and input voltage:

$$D_{DCM} = \sqrt{\frac{2P_{DCM} \times L \times Freq}{V_i^2}}. \quad (4)$$

Conversely, in CCM, the duty-cycle equation is:

$$D_{CCM} = \frac{V_o}{n_2 \times V_i + V_o}. \quad (5)$$

B. Control Aspects

One characteristic of the flyback topology is that the energy is delivered to the load only during the OFF time of the control switch; the effect of any control action during the ON time is delayed until next switch turn off. For example, in response to a step increase in load that causes a decrease in output voltage, the controller increases the ON time to increase the stored energy in the transformer. Increasing the ON time in fact decreases the OFF time. If there is CCM operation, the energy delivered to the load during the first few cycles decreases, and the initial reaction results in a larger output voltage drop. The return to regulation is reached only after the energy from longer ON-time is transferred to the load over several cycles. In small-signal-analysis modeling, this behavior is referred to as a right-half-plane zero (RHPZ). With RHPZ, the phase decreases with increasing gain, which must be considered when defining control-loop compensation.

Applicable to the test circuit used later in this document (CCM operation), Fig. 4 illustrates the influence of input voltage and output load current on the RHPZ frequency. The general rule for converters regarding RHPZ is to design at the lowest input line voltage and at the maximum load, restricting the bandwidth of the control feedback loop to about one-fifth the RHPZ frequency. The RHPZ equation is:

$$f_{RPHZ} = \frac{(1-D)^2 \times V_o}{2\pi L \times D \times I_{out} \times n_2^2}. \quad (6)$$

Even in DCM operation, RHPZ exists, but it is usually not a problem, normally exceeding half of the switching frequency.

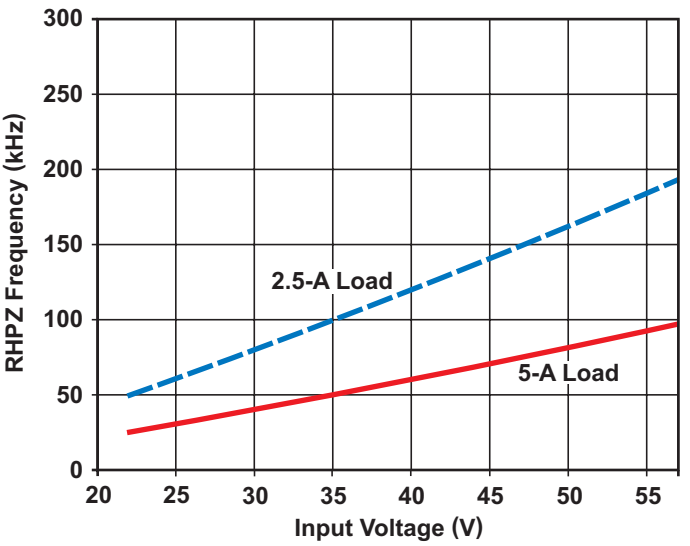


Fig. 4. An example of the influence of input voltage and load current on RHPZ frequency.

The two most popular ways of controlling the operation of a flyback topology are voltage-mode control (VMC) and peak current-mode control (CMC). CMC uses the magnetizing current to define the duty cycle, while VMC does not. When operating in CCM, a design using VMC has a relatively low-frequency double pole due to the transformer's inductance and output capacitor. Consequently, it is more difficult to compensate than peak-CMC, which basically consists of a current source driving the same capacitor. Conversely, when using peak-CMC while operating in CCM, slope compensation is necessary to avoid subharmonic oscillation when the operating duty cycle exceeds or even gets near 50%. This is usually accomplished by the addition of an external ramp to the current-feedback signal, creating a composite signal. A typical slope-compensation circuit is described later as shown in Fig. 20.

C. Summary of Fundamentals

Table 1 lists the advantages and disadvantages of CCM, DCM, and TM operating modes.

More information about the basic aspects of flyback power-supply design can be found in previous TI Power Supply Design Seminar literature. See References [1] and [2], as well as the second topic of this seminar, Incorporating Active-Clamp Technology to Maximize Efficiency in Flyback and Forward Designs.

TABLE 1. COMPARISON BETWEEN CCM, DCM, AND TM FOR A FLYBACK POWER SUPPLY

Operating Mode	Advantages	Disadvantages
CCM	• Small ripple and rms current • Lower MOSFET conduction loss • Lower primary MOSFET turn-off loss • Low core loss • Better cross-regulation • Lower capacitor dissipation • Smaller EMI filter and output filter • Constant switching frequency	• Slope compensation required at higher duty cycles (Peak CMC) • Diode reverse-recovery loss • Higher voltage stress for secondary diodes • RHPZ • Synchronous-rectifier snubber loss • Low light-load efficiency
DCM	• No diode reverse recovery loss • Slope compensation not required in CMC* • No RHPZ problem* • Lower inductance may allow smaller transformer size • First-order system even in VMC* • Constant switching frequency	• Large ripple and peak current • Higher MOSFET conduction loss • Higher core loss • Higher primary MOSFET turn-off loss • Higher capacitor dissipation • Higher MOSFET voltage stress • Large EMI filter and output filter
TM (CMC)	• No diode reverse-recovery loss • Soft turn-on switching possible—MOSFETs with lower $R_{DS(on)}$ can be used • No secondary snubber loss • Slope compensation not required • No RHPZ problem • First-order system • Transient response • Lower inductance may allow smaller transformer size	• Large ripple and peak current • Higher core loss • Higher primary MOSFET turn-off loss • Higher MOSFET conduction loss** • Higher capacitor dissipation • Large EMI filter and output filter • Variable switching frequency • Primary MOSFET voltage stress may be higher

*Valid only if DCM operation is maintained in all conditions of load current and input voltage.

**If TM is combined with soft switching, a larger and more efficient MOSFET could be selected for the primary switch to substantially reduce its conduction loss.

III. Understanding the Flyback Transformer and Its Impact on Power-Supply Performance

A. Review of Fundamentals

The flyback transformer stores energy before transferring it to the load; consequently, it behaves differently than a common transformer. Its design is similar to an inductor and a great part of the energy is stored in a gap. More importantly, the current does not flow in both primary and secondary windings at the same time, which is a major difference from a forward transformer. There is also usually more than one secondary winding, which makes a difference when compared to a normal coupled inductor. This section will focus on the flyback transformer and its parasitic parameters. The analysis includes the impact of leakage inductance on the cross-regulation of multiple outputs and the converter's short-circuit behavior.

B. Leakage Inductance

The leakage inductance between two transformer windings is a measure of the energy stored in the leakage flux, which is the portion of the field produced by one winding that is not coupled to the other winding.

The current in a flyback transformer does not circulate in the primary and secondary windings at same time. So, the definition of leakage inductance in a flyback transformer applies only during the commutation of the primary power switch. When the power switch is turned off, the energy stored in the transformer should then be supplied by the secondary winding(s). The amount of energy that cannot be immediately supplied is the leakage energy.

For example, a two-winding transformer can be modeled using the "cantilever" circuit representation as shown in Fig. 5. The total leakage reactance has been moved to the secondary side of the transformer. The corresponding transformer construction is also shown with the primary winding closer to the center gap. The leakage inductance shown connected in series with the secondary keeps the currents from changing too rapidly by generating a voltage during commutation.

When the MOSFET switch is turned off, L_{leak2} will oppose any secondary current increase from zero, and any reduction of the primary current (I_P), by generating the voltage V_{leak2} as shown in Fig. 5. In addition, the magnetizing inductance will oppose any reduction of magnetizing current by generating a voltage (V_{mag1} and V_{mag2}), which is limited by the clamp-circuit voltage (V_{clamp}). V_{clamp} is usually substantially higher than the reflected output voltage, so the magnetizing-flux rate of decrease will be higher during commutation than during the rest of the OFF period.

The leakage voltage when the switch is turned off can be approximated as:

$$V_{leak2\_off} = \frac{N2}{N1} \times V_{clamp} - V_D - V_{out}. \qquad (7)$$

Even when a synchronous rectifier is used, it is normally activated only after the transition has been completed. The V_D voltage then represents the initial voltage across the rectifier's body diode. Any energy transfer to the secondary will begin at the moment the clamp voltage reaches the secondary voltage reflected to the primary side.

Transformer leakage impacts a flyback power supply in many ways:

- Voltage spikes on power switches during commutation, requiring the use of snubbers or clamp circuits.
- Voltage spikes on secondary power rectifiers at primary switch turn on, often requiring the use of snubbers. (This is not shown in Fig. 5 but will be discussed later in the section about snubbers.)
- Efficiency decreases unless the leakage energy is recycled.
- Cross-regulation is strongly affected.
- Loss of volt-seconds during commutation to secondary windings requires a higher duty cycle than expected. With compensation coming from the voltage feedback loop, effects include a higher average magnetizing current, lower efficiency, and a lower output-load current limit. However, it is possible to minimize these effects and speed up the energy transfer with a higher voltage across the primary winding during commutation, at the price of increasing the voltage stress on the primary power switch as

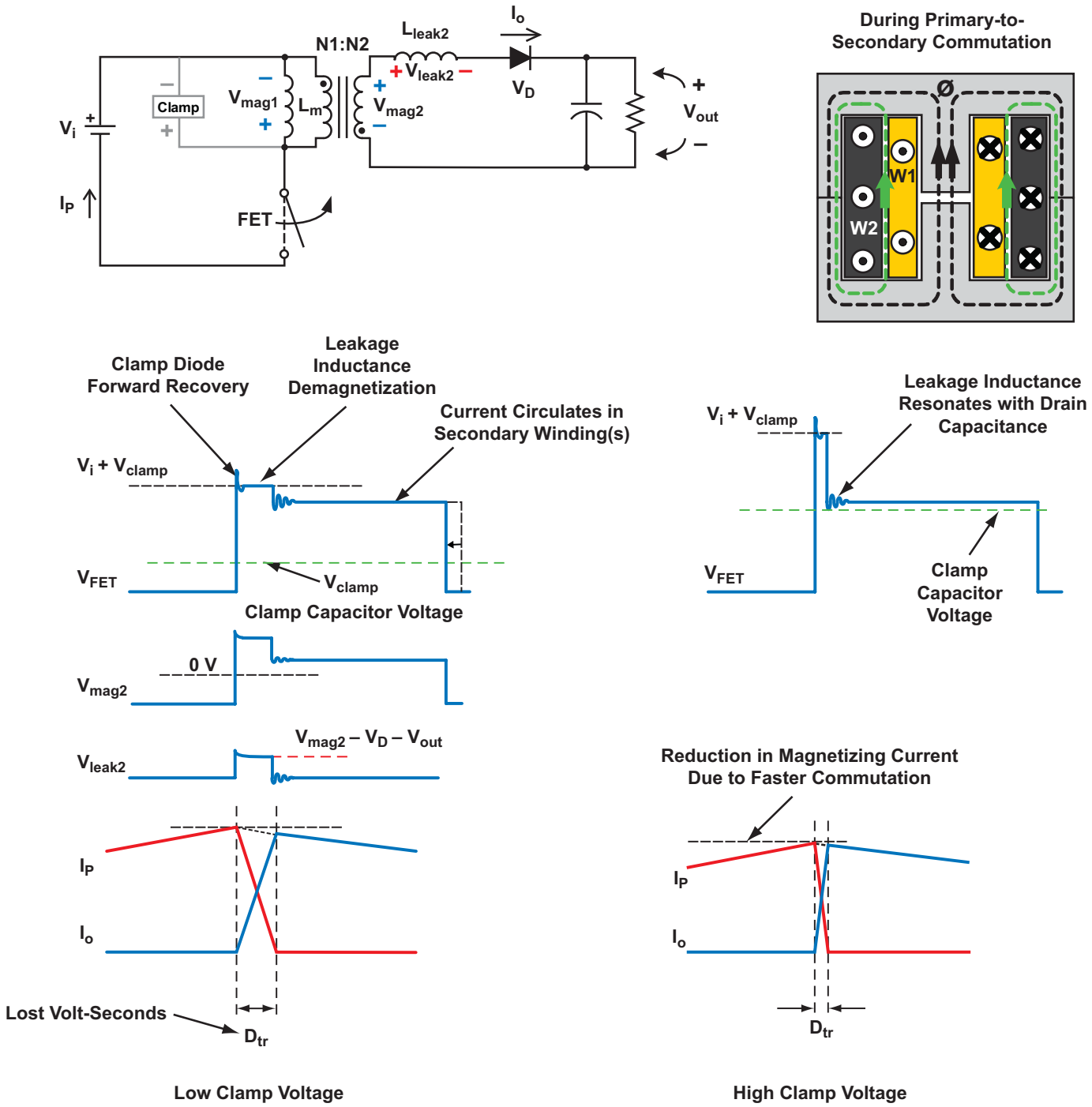


Fig. 5. Effects of flyback-leakage inductance at primary turn off and the impact of clamp voltage.

shown in Fig. 5. Note that a higher clamp voltage may degrade cross-regulation performance.
- Leakage inductance influences the rate of current rise during commutations, which could in turn influence the gate-drive strategy if a synchronous rectifier is used.
- Higher radiated EMI from the transformer.

Leakage inductance between a primary and secondary winding can be minimized with a better physical coupling between them. The following design rules can help to achieve this:
- Minimize the separation between the primary and main secondary windings.
- Interleave the primary and main secondary.
- Select a core with a long and narrow window. This increases the field length, minimizing the flux density between primary and secondary windings and reducing the number of layers. An additional benefit is lower AC winding losses.

Note that leakage inductance is a function of winding geometry, the number of turns, and the spacing between the primary and the secondary. Leakage inductance is independent of the core material and it will not be reduced by having the winding tightly coupled to the core.

C. Cross-Regulation

Theory of Operation

The multiple-output flyback converter is a popular topology because of its simplicity and low cost. If perfect coupling between windings was possible, the output voltages would be directly defined by their respective turns ratio to the winding supplying the regulated output. Unfortunately, perfect winding coupling is impossible and the coupling operation is very complex, which often results in poor cross-regulation.

There are a few known models for cross-regulation analysis. For example, cross-regulation analysis using the extended cantilever model [3] is quite complex but has advantages such as geometry independence and its parameters can be directly measured. On the other hand, the physical model (also called the "Ladder" model) shown in Fig. 6 is based on the fact that the transformer windings cannot all be equally well coupled to the energy-storage gap because of physical separation between them. Also, additional amounts of magnetic energy are stored between the windings and are represented as leakage inductances. Although not applicable to any transformer geometry, this model is a good tool to help understand how most of the common flyback-transformer geometries work. The circuit representation in Fig. 6 is only applicable to the transformer-winding stackup shown. A more complex circuit representation will be needed if interleaving is used or if multiple secondary windings are wound simultaneously (multifilar). Also, this model does lack accuracy when evaluating lightly-loaded secondary outputs.

During commutation, the magnetizing flux (ϕ_m) in the gap decreases, which induces current into the secondary windings. This induced current helps maintain the magnetomotive force (MMF) in the gap. The rate of flux decrease (including leakage) within each secondary winding is limited by its output voltage, following the equation:

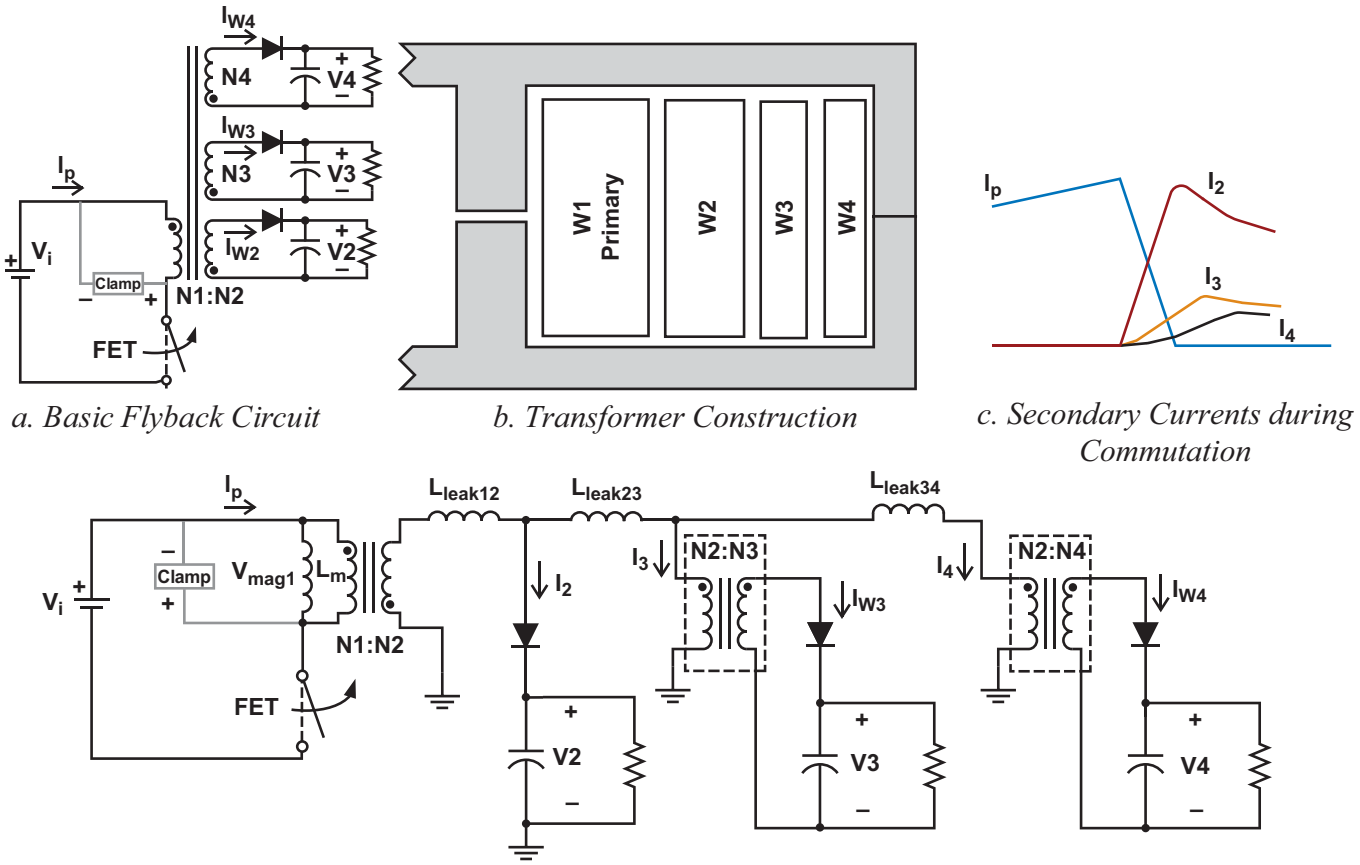
$$e = -N \times \frac{d\phi_m}{dt}, \tag{8}$$

where N is the number of turns of a winding and e is its induced voltage.

For example, once the primary voltage exceeds W2's reflected voltage, W2's current increases and in turn generates an increasing flux. Because of leakage flux between W1 and W2, the primary voltage goes up until the clamp voltage is reached. This defines a limit on $d\phi_m/dt$ in the gap.

The main secondary winding (W2), being next to the primary (W1), dictates the $d\phi/dt$ that the outer windings will see during commutation. With W3 and W4 located after the main output winding, the generated winding voltage is lower than would be expected if there was no leakage at all. The net effect shown in Fig. 6 is that when the main switch is turned off, the current commutates progressively from near-to-remote secondary windings.

However, if interleaving was used such that half of W1 is next to the low-power secondary windings, part of the flux of W1 would not be sensed by W2, but it would be sensed by the lower-power secondary windings, thereby increasing the voltage induced into these windings.



a. Basic Flyback Circuit *b. Transformer Construction* *c. Secondary Currents during Commutation*

d. Transformer Physical Model

Fig. 6. Flyback cross-regulation in a physical-based model with idealized secondary-current waveforms (All outputs are at full load; winding-resistance and parasitic-capacitance effects not included).

In the model shown, when all leakages are moved to W2's side of the transformer, L_{leak12} corresponds to the leakage inductance between W2 and W1, while L_{leak23} and L_{leak34} correspond to the leakage between W2 to W3 and W3 to W4, respectively.

Ringing Caused by Leakage Inductance and Parasitic Capacitance

There is one behavior of the flyback transformer that most existing models fail to predict accurately—the light-load operation of auxiliary windings while the main output is fully loaded.

When the main switch turns off, the primary current causes the voltage to rise very quickly when the main output is heavily loaded. Due to transformer leakage inductance and parasitic capacitance (winding and diode), the secondary voltage tends to ring. If the auxiliary output is fully loaded, this ringing is clamped. However, at light load, this ringing begins to charge up the output storage capacitor to the ringing-voltage overshoot through the output rectifier, which blocks return of the energy. At light load, this results in a much higher auxiliary output voltage, which can sometimes even exceeding twice its nominal value. This effect generally becomes worse as the primary clamp voltage gets higher.

Common to flyback power supplies, the light-load cross-regulation problem can be mitigated, but not eliminated, by minimizing leakage inductance between secondary windings. It also helps to locate the highest-power secondaries closest to the primary. Other solutions to deal with this problem include the use of a post regulator, a series resistor, or a minimum load. Some solutions involve minimizing the effective winding capacity. See Reference [18] for details.

Operation with Combined Effects

Corresponding with Fig. 6, Fig. 7 shows an example of the first three phases during commutation from primary to secondary. For descriptive purposes, it is assumed that W2 is the high current winding, I_{2_pk} is not high enough because L_{leak21} is too large, and W4 receives too much energy during the commutation because of ringing at light load. W3 and W4 are low-current auxiliary secondary windings.

Unlike a forward transformer, in a flyback transformer, both the primary and secondary windings simultaneously produce a flux only during the commutation periods; this flux is the magnetizing flux. Another difference is that during commutation periods, the flux created by each winding within the gap is in the same direction because the windings all try to maintain the magnetizing flux while the primary-winding current is ramping down. Consequently, the flux lines created in the spacing (leakage) between the windings are opposing each other. Note that the amplitude of the leakage flux along a specific path is proportional to $\Sigma(N \times I)$ and the spacing between the two layers, and it is inversely proportional to dimension L of the window area shown in Fig. 7.

As mentioned before, during commutation, a decrease of magnetizing flux (ϕ_m) induces a rising current in the secondary windings. Due to leakage between W1 and W2, the primary voltage goes up until the clamp voltage is reached, which defines a limit on $d\phi_m/dt$ in the gap. The lower the clamp voltage, the lower the induced voltage in the secondary windings, and the softer the di/dt in them will be. If there was no primary clamp circuit, the commutation to W2 secondary would be instantaneous, but the MOSFET would be destroyed by voltage stress.

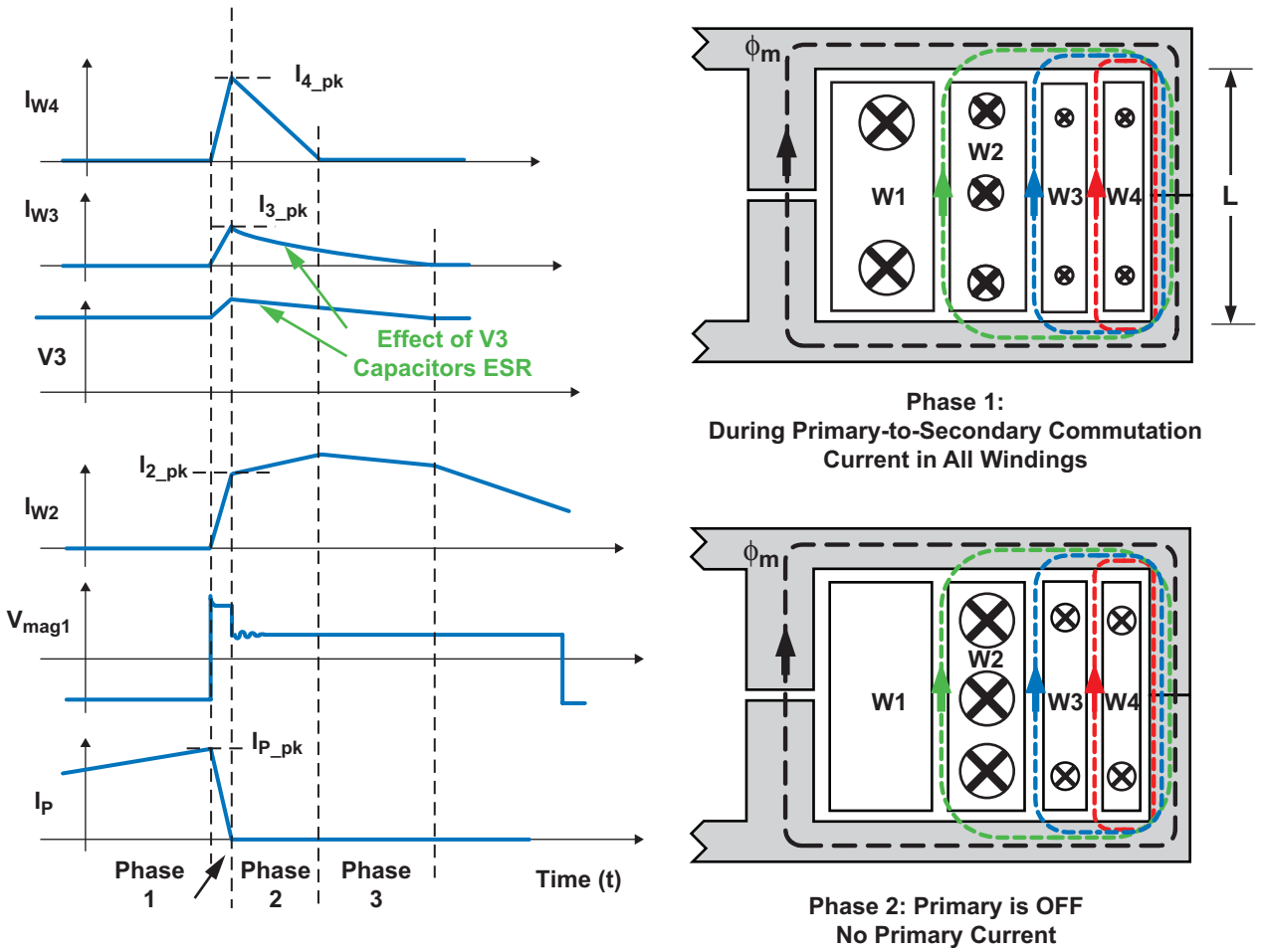


Fig. 7. Cross-regulation phases at primary-switch turn off.

At the end of phase 1, the sum of the reflected secondary currents is equal to total magnetizing current:

$$I_{P\_pk} = n_2 \times I_{2\_pk} + n_3 \times I_{3\_pk} + n_4 \times I_{4\_pk} \quad (9)$$

where I_{x_pk} and n_x are respectively the current at end of commutation interval and the primary-to-secondary turns ratio for secondary winding number x.

From phase 2 and for the rest of the (1 – D) period of the switching cycle, the secondary currents increase or decrease at rates that depend on differences between the reflected output voltages. It is assumed in this example that I_{4_pk} has become too high and V4's output capacitor received too much energy during phase 1. At beginning of phase 2, a portion of magnetizing flux is coming from W4 and it starts decreasing at a rate defined by W4's voltage. Also, W2's contribution increases to maintain the magnetizing flux in the gap. During that time, I_{W4} goes down until it crosses zero and stops decreasing because of the diode. If an output is very lightly loaded, its voltage will increase significantly during commutation. This means a much steeper (faster) current decrease after phase 1.

The load at each output can greatly affect cross-regulation. The output-capacitor ESR also has non-negligible impact since it changes the slope as the current decreases. With lower current, the ESR voltage and the voltage across the leakage inductance will be lower, which means a lower di/dt. The waveforms for V3 and I_{W3} in Fig. 7 demonstrate this concept.

The change in slope of I_{W2} when I_{W4} crosses zero can be explained with the following equation:

$$H \times \delta = \frac{\phi_m}{A \times \mu} \times \delta = \sum (N \times I), \quad (10)$$

where H is the magnetic field, δ is the core gap, ϕ_m is the magnetizing flux, A is the core cross-section, μ is the gap permeability, and N × I is the ampere-turns of a winding. Equation 10 shows that a falling magnetizing flux (ϕ_m) corresponds to a falling magnetizing current which is shared between all active windings.

Obviously, operating the main output in CCM (using a synchronous rectifier is one example) guarantees that V_{mag1} is maintained during the (1 – D) period, helping to achieve better cross-regulation.

How Cross-Regulation Can be Optimized

Ideally, the initial rising current rate would be proportional to the amount of current the load needs, but in practice this is difficult to achieve. The current reached in each winding at the end of commutation depends on leakage inductances and other parasitics.

Good cross-regulation entails maintaining good control of auxiliary output voltages in spite of load variations at each output, as well as controlling the main regulated output. Other benefits of good cross-regulation related to efficiency include:

- Operation closer to CCM resulting in lower rms current and lower power dissipation in the output capacitors' ESR.
- Lower gate-drive losses are realized because the voltage rail that provides gate drive for power switches becomes more stable for all load conditions.

Also, limiting the initial energy delivered to the V_{DD} auxiliary rail can offer better protection by allowing the controller to more easily reach hiccup mode during a short-circuit event.

Various winding strategies can be considered in order to achieve acceptable cross-regulation. Here are some general design guidelines:

- The load range for each secondary output must be well known. The worst case for an auxiliary secondary output is when it is lightly loaded while the main output is fully loaded.
- The winding of the output with the widest load range (usually the regulated output) should have the best coupling to the primary, which means it should have the smallest leakage inductance to the primary.
- The leakage between all secondary windings should be minimized.

Fig. 8. Winding placement can affect leakage.

- Minimizing the leakage inductance of low-current, auxiliary secondary windings to the primary is not a good strategy. Larger leakage inductance to the primary helps limit the energy delivered to these windings during commutation by increasing their CCM load range and improving their cross-regulation (see Fig. 8).
- Leakage inductance is influenced by winding placement on the bobbin. The winding stackup (W4 compared to W3 in Fig. 6) defines how close each secondary winding is to the primary. It is usually a good practice to spread a winding over the full width of the bobbin for better coupling.
- Winding more than one auxiliary secondary simultaneously using a multifilar technique usually provides better cross-regulation control.
- Operate the main output in CCM. This output voltage then defines the magnetizing voltage (V_{mag}) during the total cycle.
- Try to operate the secondary auxiliary outputs close to the boundary between CCM and DCM. This ensures that enough energy—but not too much—is delivered to each. One way to accomplish this is by adding some series impedance and/or enough load current at minimum load.
- When secondary windings share the same ground and a similar polarity, AC or DC stack is another alternative to improve cross-regulation. (See Fig. 9.)
- Leakage inductance can vary from one production unit to the next. For predictable cross-regulation, some maximum leakage inductances need to be specified and controlled. For example, main output to primary, as well as between secondary windings.

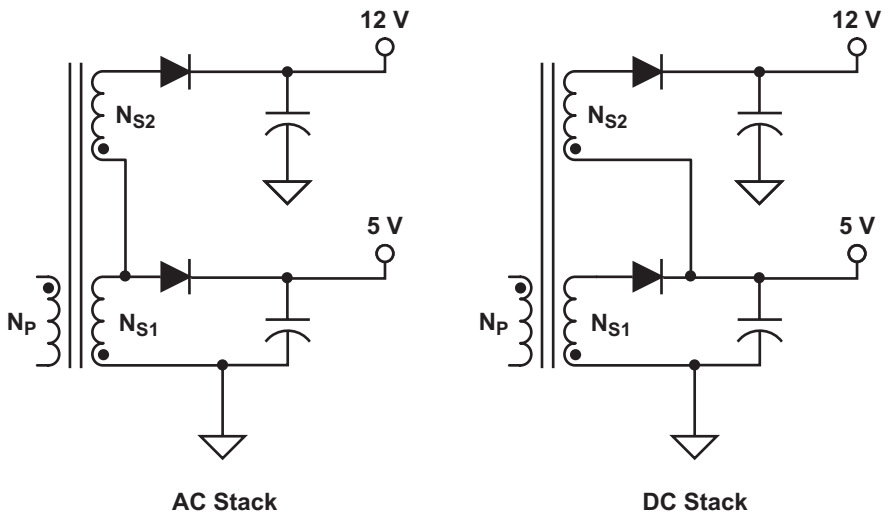


Fig. 9. AC and DC stack.

Other parameters can have an impact on cross-regulation, including:

- Primary clamp voltage. A higher voltage means a faster commutation and a stronger ringing effect. The current shared between secondary windings during commutation is more dependent on transformer parasitics and has less tendency to follow the load level of each output. This means a stronger influence from leakage inductances and parasitic capacitances on the initial peak current reached, and consequently worse cross-regulation from load variations. Note that with an RCD clamp circuit, the clamp voltage normally increases when the input current is higher, which when combined with a higher magnetizing energy may worsen cross-regulation.
- Forward recovery of output diodes. Using a diode with a faster turn on will result in more energy delivered to its output, resulting in a higher output voltage at a light load. Diode parasitic capacitance also has some impact on the result.
- A synchronous rectifier (if used on the main output) may be off during the commutation from primary to secondary, with current circulating through the body diode. This results in more energy delivered to the other windings, since the reflected voltage is higher during commutation. Energy is also lost while the body diode conducts.
- Where tighter control is required and where the load range is limited, a low-value resistor may be inserted in series with the diode (before the capacitor). Using a resistor constitutes an acceptable trade-off, with a resistance value high enough to limit the amount of energy delivered to the output capacitor during commutation and low enough to mitigate its impact on DC voltage droop and efficiency. This solution is often used for the controller's V_{DD} voltage.
- When all else fails, a dummy load may be needed to limit the maximum voltage of lightly loaded windings.

Cross-Regulation's Impact On Short-Circuit Behavior

Short-circuit protection for a multioutput flyback power supply poses many challenges. When relying solely on the primary current limit, the output current of a flyback power supply can become quite high during a short circuit. The wire used for the main output winding is usually selected so that it is tolerant to strong overloads until a hiccup mode is reached. But for a low-current auxiliary output (see W3 and W4 in Fig. 7), the winding wire size is usually very small. When a strong overload or a short circuit occurs at this output, particularly while the main output is lightly loaded, most of the power capability of the power supply is available. Thus, the winding dissipation of the output can become very high in spite of the primary current limit, with potentially catastrophic results.

Some power supplies rely on the collapse of the voltage rail used to power the controller during a short circuit. However, this technique lacks accuracy and is often unreliable. One reason is that because of the leakage inductance and parasitic capacity, not all the transformer energy is delivered to the short-circuited output. Some energy is still delivered to the auxiliary output powering the controller and since the consumption on that rail is usually low, the delivered energy can be high enough to keep the controller alive indefinitely.

A much better way is to have short-circuit detection for each output. For example, the use of a single, summing-current transformer is a relatively simple solution. Note that in the particular case where the auxiliary output powering the controller is short-circuited, an undervoltage lockout condition will simply disable the controller.

D. Test Results: Cross-Regulation

To illustrate the effect of winding strategy on cross-regulation, various flyback transformers were designed, built, and tested on a modified evaluation module (EVM) based on the TPS23754 controller. For oscilloscope measurements, current transformers with sensing circuitry were built and

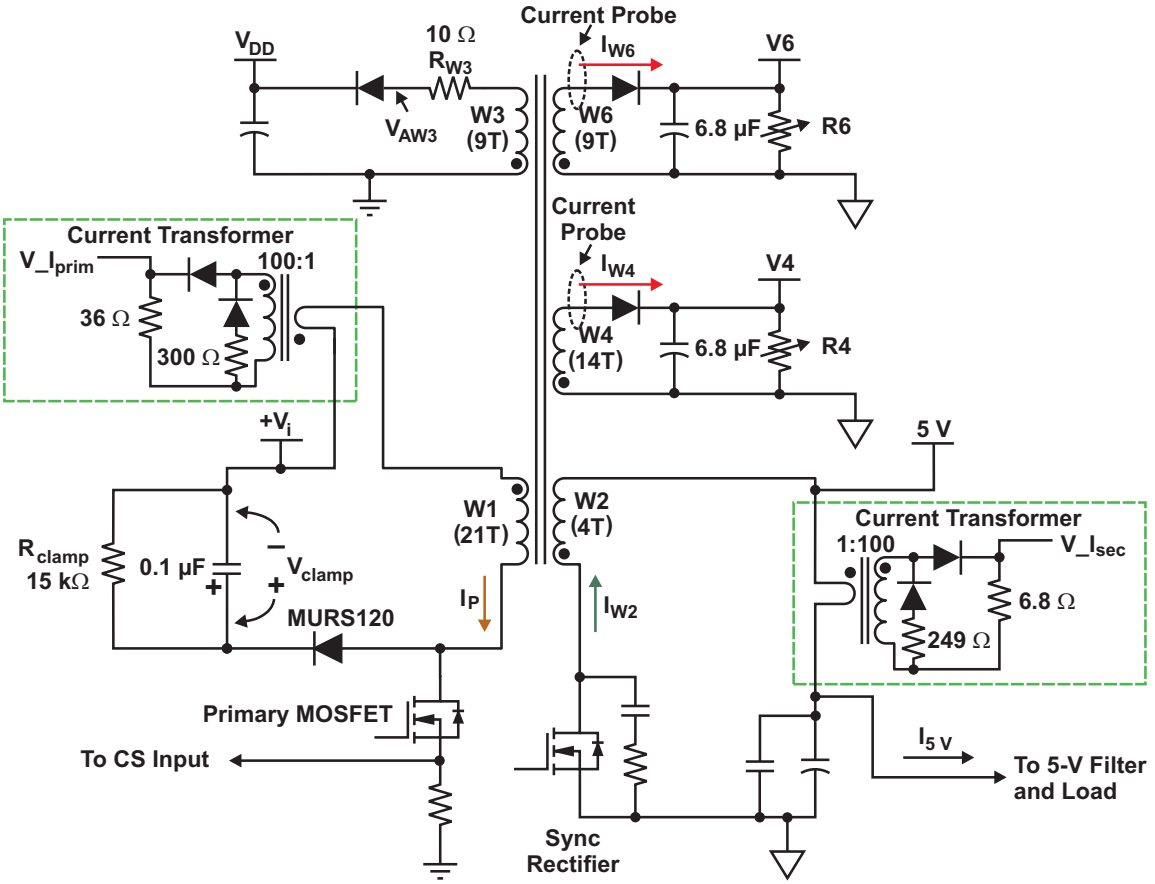


Fig. 10. Cross-regulation test circuit using an RCD clamp and current-sense transformers.

inserted in series with the primary and secondary windings, with care taken to limit wire lengths and loops to ensure minimum impact on the operation of the circuit. Standard current probes were also used for the auxiliary (low-current) secondary windings (see Fig. 10).

The basic operating conditions were:

- Input voltage: 48 V
- 5-V output load: 0 A to 5 A
- Auxiliary outputs: V6 (10 V at 0 to 140 mA) and V4 (18 V at 0 to 200 mA)
- Switching frequency: 250 kHz

The transformer's magnetizing inductance (L_{mag_pri}) seen at primary is nominally 70 µH. The core size used was EFD20/10/7. Note that multifilar (side-by-side) wires were used for both the primary (4 wires #30) and W2 secondary (3 x 4 wires #30), for better coupling and efficiency. Also, the primary winding (W1) uses two series-connected layers (see Figs. 10 and 11).

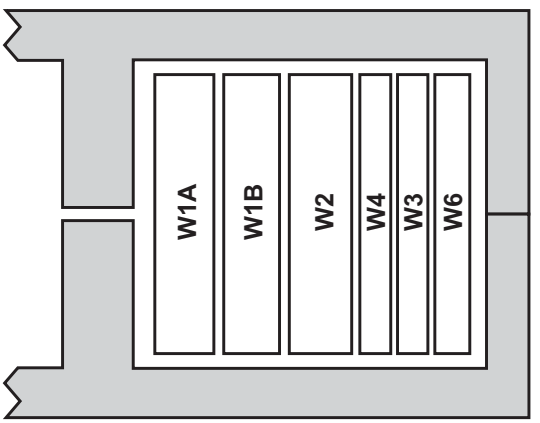
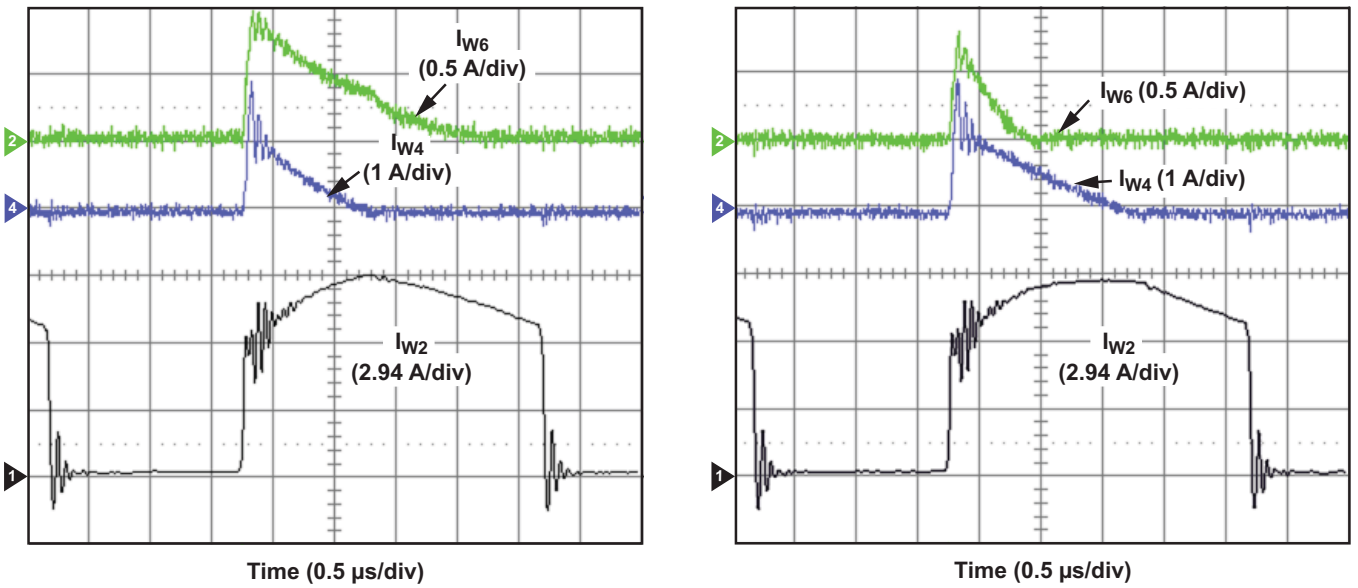


Fig. 11. Transformer winding stackup.



a. V6 at 1.6 W and V4 at 2.5 W.

b. V6 at 0.5 W and V4 at 3.6 W.

Fig. 12. Current waveforms of secondary windings with I_{5_V} = 5 A.

Cross-Regulation Tests:

As an example, the transformer's leakage inductance chosen was: L_{leak21} = 43 nH (see Fig. 11). Fig. 12 show what happens, while the loads at V4 and V6 are changed. The main output is highly loaded which explains why W4 and W6 are operating in DCM even if they are noticeably loaded. The V_I_{sec} output level is proportional to the current through the main secondary (W2) as shown in Fig. 10. Note that W2's current falls more steeply when W4's and W6's current cross zero. As previously explained with Equations (8) and (10), the dϕ/dt, reflected as a di/dt, is shared between the active windings since

$$H \times \delta = \Sigma(N \times I).$$

Fig. 13 shows the initial rise of currents with 0.5 W and 3.6 W loads at V6 at V4, respectively. It is clear that W2's current rises first.

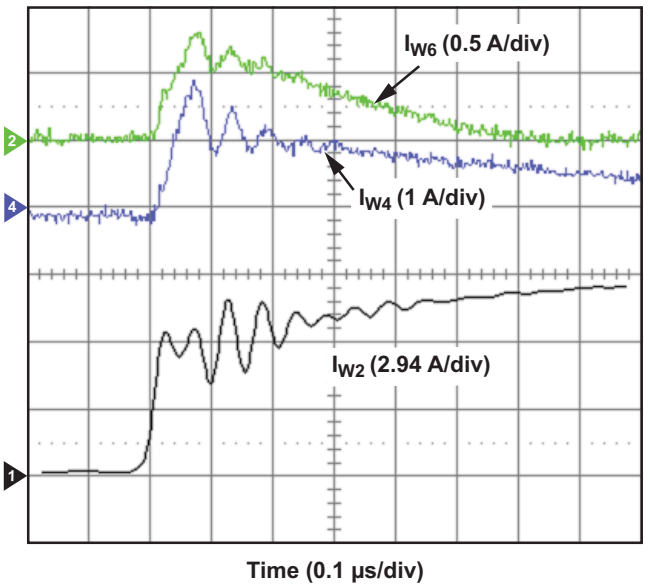
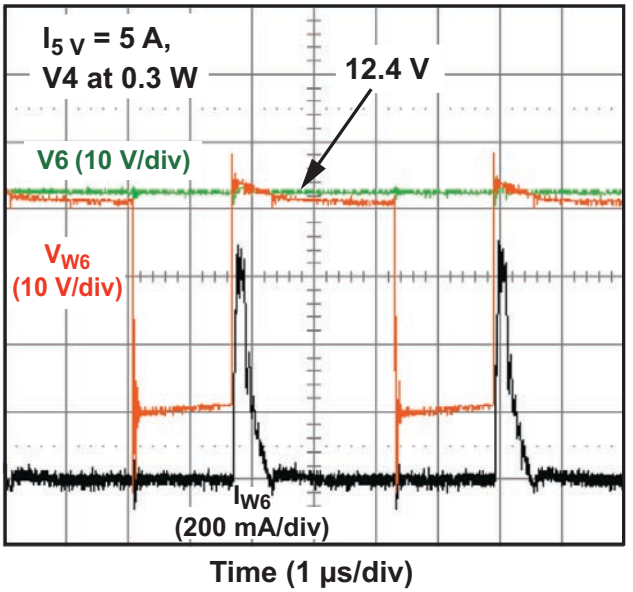
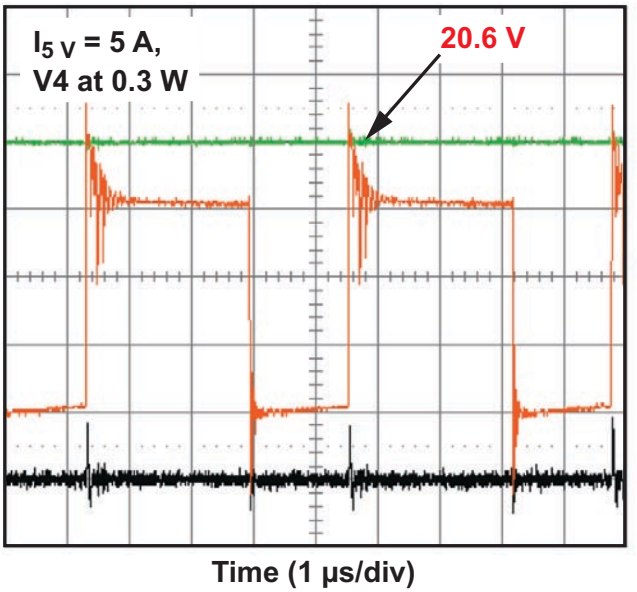


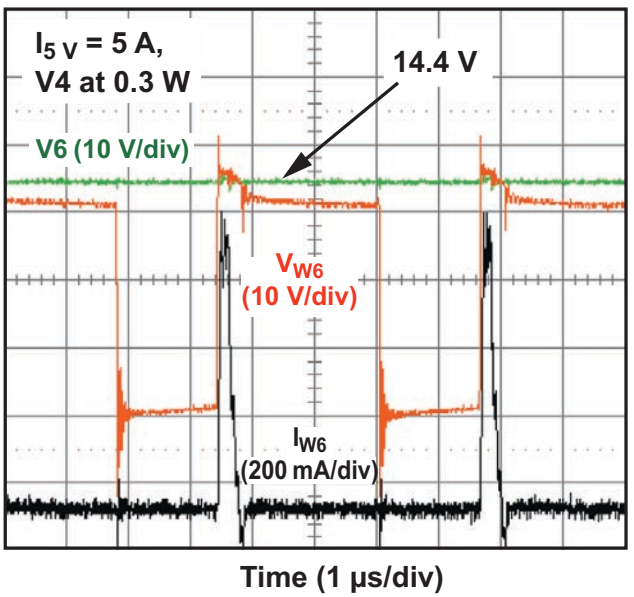
Fig. 13. Current waveforms of secondary windings with I_{5_V} = 5 A, V6 at 0.5 W, and V4 at 3.6 W.



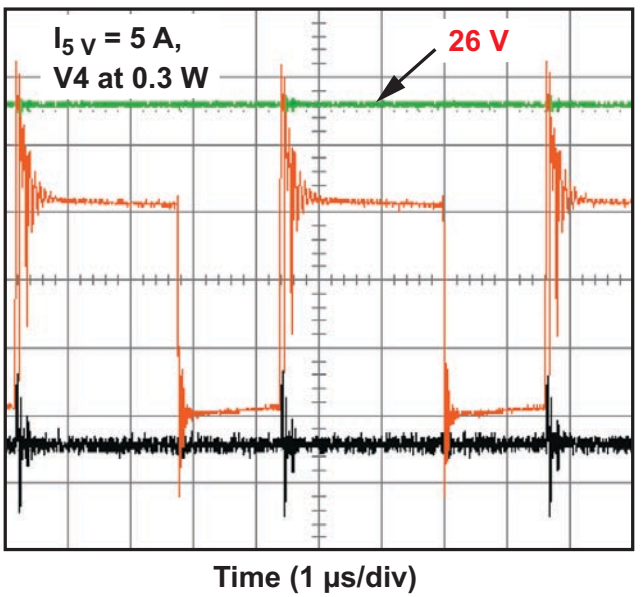
a. With V6 at 0.5 W and V_{clamp} = 70 V.



b. With V6 less than 5 mW and V_{clamp} = 70 V.



c. With V6 at 0.5 W and V_{clamp} = 83 V.



d. With V6 less than 5 mW and V_{clamp} = 83 V.

Fig. 14. Cross-regulation changes caused by clamp-voltage and load variations with a lightly loaded auxiliary.

Fig. 14 shows what happens when an auxiliary output (V6) is lightly loaded while the main output (V2) is fully loaded. The V6 output more than doubles as its load current decreases. Also, the RCD clamp resistor was changed to show the effect of primary clamp voltage on cross-regulation — the higher clamp voltage also causes poorer cross-regulation.

Output Current Overload Tests:

The reaction of the power supply to current overloads on various outputs was tested with the same transformer described earlier. A worst-case test condition was established with the main 5-V output unloaded, the load resistance at V6 was decreased down to 1 Ω (not low enough to result in a V_{DD} UVLO), and the load current exceeded 3 A.

Fig. 15 shows that even with a 1-Ω load at W6, there was enough energy delivered to the V_{DD} output to maintain switching, V_{AW3} is the voltage measured at the anode of W3's series diode. The duty cycle is still fairly high because the 5-V output does not collapse, allowing the down-slope of magnetizing current during (1 – D) to remain strong.

The problem is that leakage inductance and the ringing effect previously described prevents W6 from taking all of the transformer energy. W3 has in fact a better coupling to the primary than W6. In this case, the best solution is individual-output overcurrent protection.

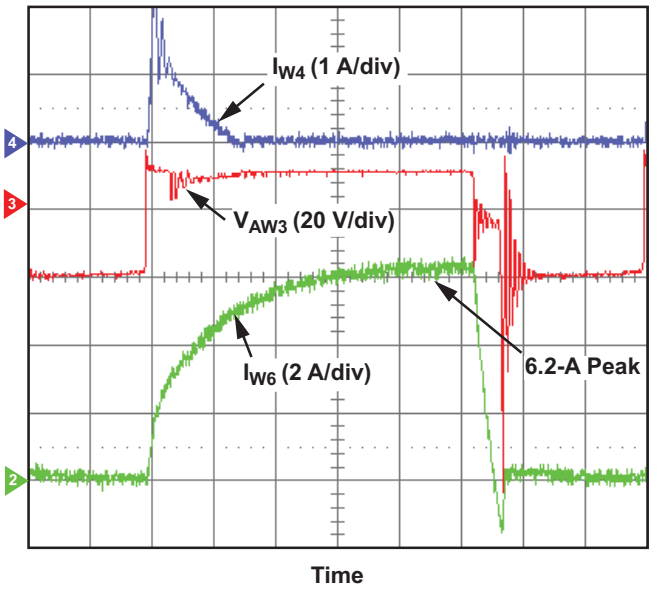


Fig. 15. Strong V6 overload (R6 = 1 Ω) with V4 at 2.5 W and 5 V at zero load.

E. Transformer Impact on Efficiency

Transformer design plays a crucial role in the efficiency of a flyback converter. For example, efficiency can be improved by minimizing high-frequency conduction losses—commonly identified as "skin-effect" and "proximity-effect" losses. Skin effect is the tendency of a high-frequency AC current to distribute itself within a conductor so that the current density near its surface is greater than at its center. Proximity effect is when an AC current in a conductor induces eddy currents in adjacent conductors.

Wire type and size has a great influence on these characteristics. "Litz" wire (made of multiple strands woven in a pattern to reduce high-frequency loss) usually provides the best performance, while multifilar wound strands, when carefully defined, can provide acceptable results. The strategy used in stacking winding layers also influences proximity-effect losses. Sometimes, evaluating the trade-off between proximity-effect losses and DC resistive losses can determine the number of strands for a minimum-loss winding.

Predicting proximity-effect losses for a flyback converter is not trivial; it requires validation through lab testing, since the current does not circulate in the primary and secondary windings at same time. One prediction method entails using the α-parameter graph (see Fig. 16).

In Fig. 16, Q′ is proportional to the power dissipation in a layer and at a single frequency. It is normalized to the dissipation associated with a DC current in a one-skin-depth thick layer. Also in

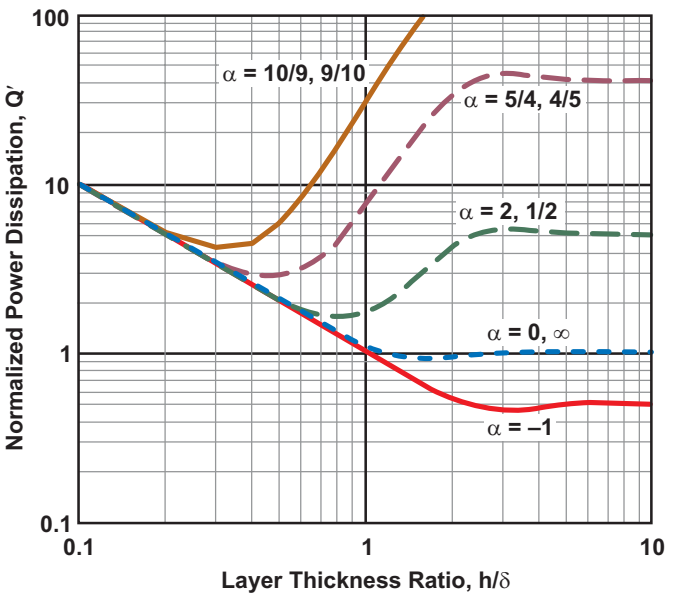


Fig. 16. Normalized power dissipation per layer versus effective layer-thickness ratio.

Fig. 16, δ represents the skin depth of the conductor at the frequency considered. The h parameter is the effective layer thickness (assuming round wires) and it can be estimated with the equation:

$$h = 0.83 \times d \times \sqrt{\frac{d}{d_o}}, \quad (11)$$

where d is the wire diameter and d_o is the center-to-center wire spacing.

The α parameter for a layer is the ratio the tangential H-field's AC component on one side of the layer to the H-field's AC component on the other side, at the frequency considered:

$$\alpha = \frac{H_{t\_sideA}}{H_{t\_sideB}}. \quad (12)$$

For each α value, an optimum thickness exists at which power dissipation is minimal. The winding strategy and number of layers directly affect α. Having α = 0 or ∞ usually minimizes the AC copper loss related to the fundamental and the harmonics. One strategy against proximity-effect loss is to select a core shape that will minimize the number of layers. For more details on AC winding losses, see References [4], [5], and [6].

Other factors affecting efficiency are:

- Cross-regulation performance. For example, the auxiliary rail used to power the controller has a direct impact on the gate-switching losses. Also, poor cross-regulation can result in excessive rms current in low-power secondary windings and in their output capacitors' ESR.
- High leakage between the primary and main secondary windings means more energy lost in clamps and snubbers.
- CCM operation usually provides better efficiency (lower conduction and core loss) than DCM.
- The effect of fringing flux from a gap. In a flyback transformer, it's better (although maybe not always practical) to keep the windings away from the fringing field associated with discrete gaps.
- The transformer turns ratio, which must be carefully defined for an optimum duty cycle and high efficiency. Fig. 17 shows that there is an optimum duty cycle for which conduction losses can be minimized. The squared primary current is multiplied by a factor of 20 and then compared to the squared secondary current. The 20x factor, which is arbitrary, assumes that resistance in the primary circuitry, including transformer winding and MOSFET, is 20x higher than in the secondary circuitry. The full input voltage range should be considered during this analysis.

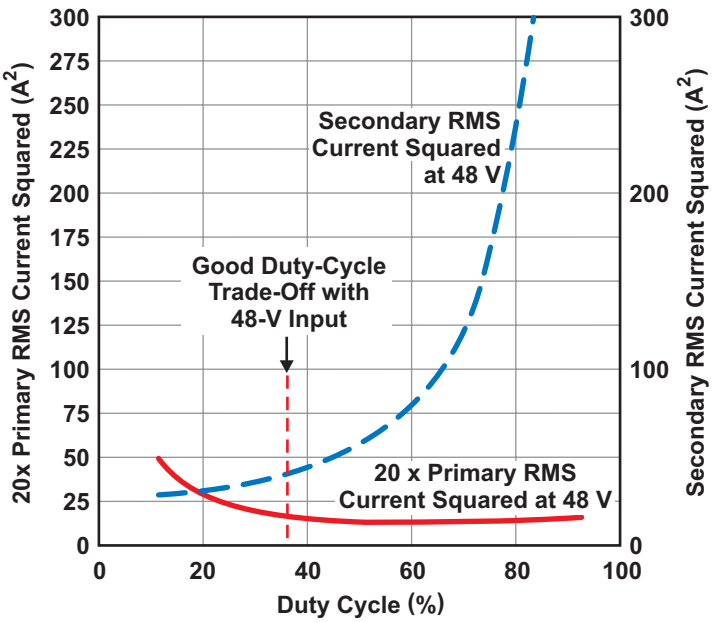
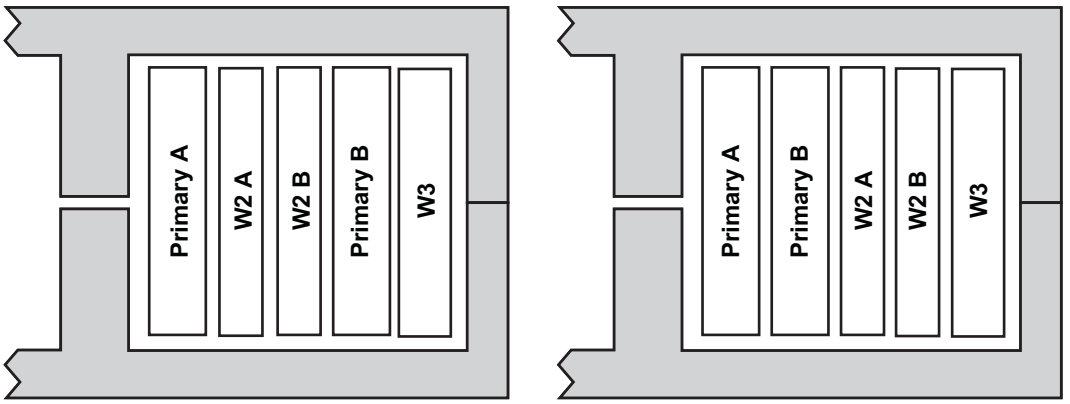


Fig. 17. Effects of operating duty cycle on conduction loss.



a. Transformer 2xW2 (Interleaved).

b. Transformer 2xW2_NI (Not Interleaved).

Fig. 18. Flyback transformers used for efficiency tests.

Efficiency Test Results

To illustrate the effect of winding strategy on efficiency, two additional flyback transformers were designed, built, and tested on the modified EVM described previously. For high accuracy, the transformer was installed with very short connections using surface-mount terminations. The basic operating conditions remained the same, except there was only one main 5-V output.

These two flyback transformers, built by Coilcraft, are shown in Fig. 18. Both have a 70-µH nominal inductance and use the same wire types and cores. The only difference between the two is that one is built using interleaving (2xW2). The W2 winding was built on two layers, resulting in lower leakage inductance and better efficiency when interleaving is used. The measured leakage inductance (L_{leak21}) is 21 nH for the 2xW2 and 47 nH for the 2xW2_NI.

Fig. 19 illustrates the effect of interleaving on efficiency. In both cases, a basic RCD clamp circuit was used with a 15-kΩ resistor. It clearly shows an improvement exceeding 1% at peak output power. Efficiency while using the 2xW2 configuration can get even better than shown. Because a higher clamp voltage can be used, the peak drain voltage at the primary MOSFET is 20 V lower with interleaving. Two reasons explain this improvement. First, the leakage energy is lower. Second, interleaving results in a lower proximity-effect loss as previously shown in Fig. 16.

F. Summary of Flyback Transformers

The flyback transformer is a critical component of a flyback power supply. Power-supply designers need to have a thorough understanding of how to control and take advantage of transformer parasitics for optimum converter performance and cost.

Here is a summary of the recommended design guidelines:

- Minimize the leakage inductance from the primary winding to the main (high-current) secondary winding. This may include minimizing the separation between each, interleaving, and

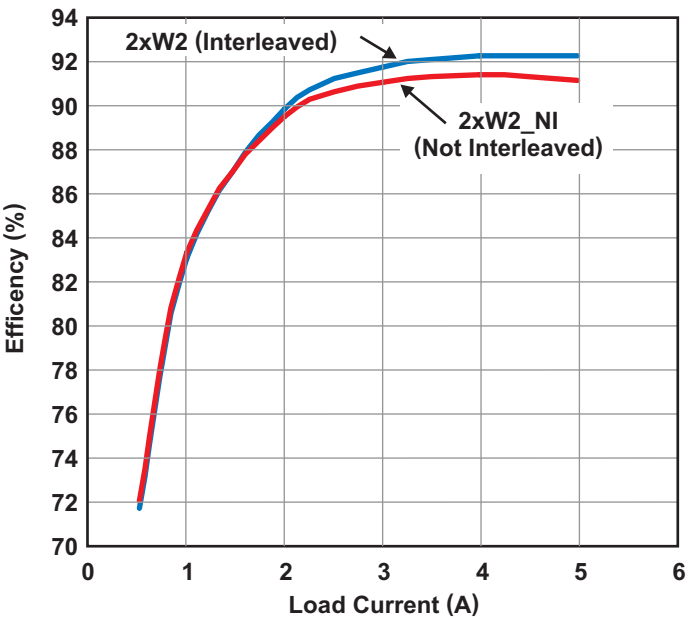


Fig. 19. Effect of interleaving on flyback efficiency.

using a core with a long and narrow window for a minimum number of layers (this also reduces proximity-effect losses).

- Minimize the leakage between the main secondary winding and the auxiliary winding used for controller feedback. However, do not minimize the leakage inductance from the primary winding to this auxiliary winding. When necessary due to ringing effect, insert a low-value resistor in series with the auxiliary winding.
- In applications with additional outputs without a post regulator:
  - Minimize the leakage between all secondary windings.
  - Consider winding all auxiliary secondaries simultaneously using a multifilar technique.
  - Do not necessarily minimize the leakage from primary to these additional low-current auxiliary windings; instead, optimize the winding strategy for better cross-regulation performance.
  - Try to operate these outputs close to the boundary between CCM and DCM for better cross-regulation.
  - Operate the main output in CCM for better cross-regulation; one way is to use a synchronous rectifier (also good for efficiency purposes).
  - If the regulation at light load is still inadequate, consider using a dummy load.
  - Do not assume that the main flyback controller will automatically protect against a short-circuit at the auxiliary outputs. When necessary, consider using dedicated short-circuit detection for these outputs.
- The primary clamp voltage has an impact on cross-regulation. Decreasing the clamp voltage usually improves cross-regulation for lightly-loaded auxiliary outputs. However, as will be explained in sections IV and VI, other factors must be considered when defining the optimal clamp voltage.
- Consider using multifilar (side-by-side) or Litz wires when necessary for optimal efficiency.
- The transformer turns ratio has a direct impact on operating duty cycle and efficiency.
- Always test the transformer performance in a real test circuit in order to validate the analyses and optimize the design.

IV. Analysis of Flyback Power-Supply Current Limiting and Influence of Parasitics

A. Current-Limiting Options

A power-supply's current-limiting characteristic determines the maximum power available at its output, beyond which the output voltage falls out of regulation. It is also used to predict the output current in overload situations like a short-circuit, in which case the current may be significant.

Understanding the behavior of the current-limiting characteristic, including the influence of parasitics and operating conditions for a flyback topology, is not trivial. If incorrectly applied, two things could happen. First, the power supply might fail to deliver its rated output power in some operating conditions, being unable to maintain its output voltage even if the current demand was within the power-supply specification. Second, unexpected component overstress (inside the power supply and/or load) might occur during overload or short-circuit, with consequences to system reliability.

This section explains the current-limiting mechanisms of a flyback power supply and provides a method for predicting current-limiting operation. Appendix A provides supporting derivations for a better understanding of the equations presented in this section.

A fundamental difference between CMC and VMC is that CMC uses primary current feedback as well as output voltage to define the duty cycle, meaning that current feedback is part of the control loop. There are in fact two control loops: one is the inner current loop and the other is the output voltage-regulating control loop. With CMC, there can be inherent cycle-by-cycle current limiting. This section will show how to build a detailed model applicable to a flyback power supply operating with peak CMC in CCM with a fixed frequency.

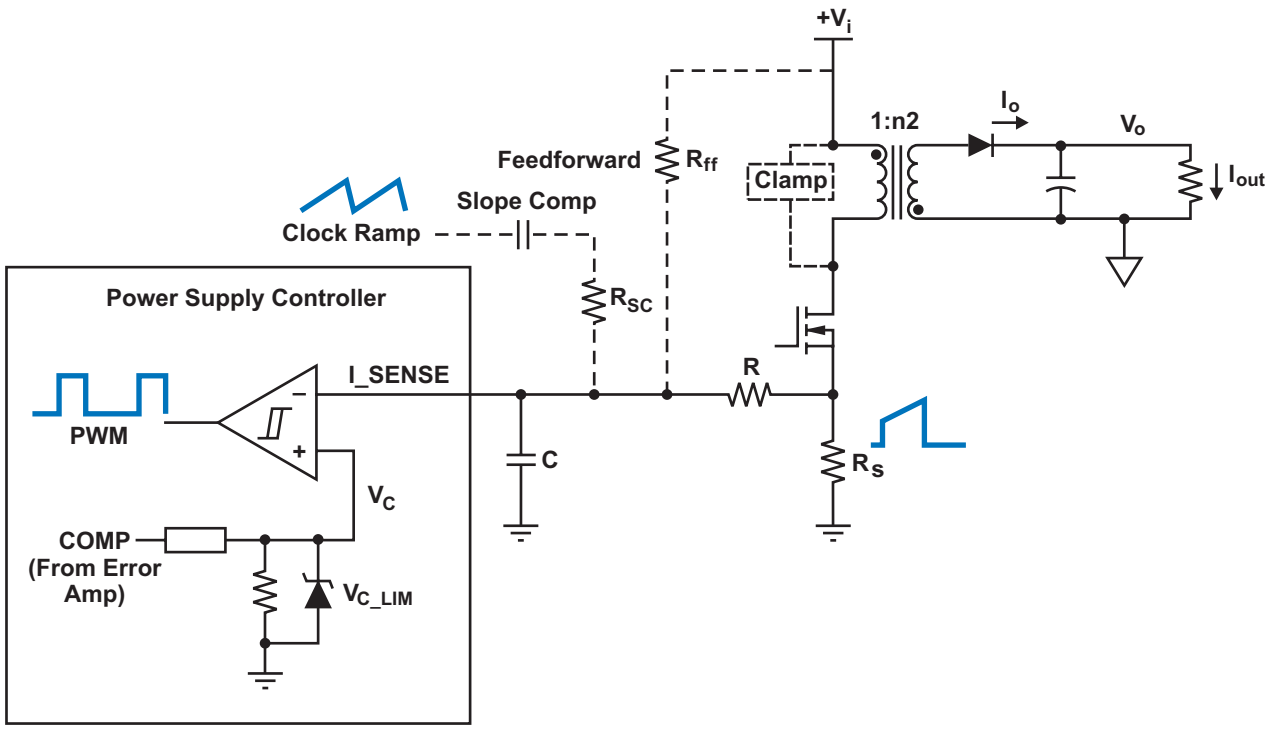


Fig. 20. Typical current feedback network of a flyback power supply.

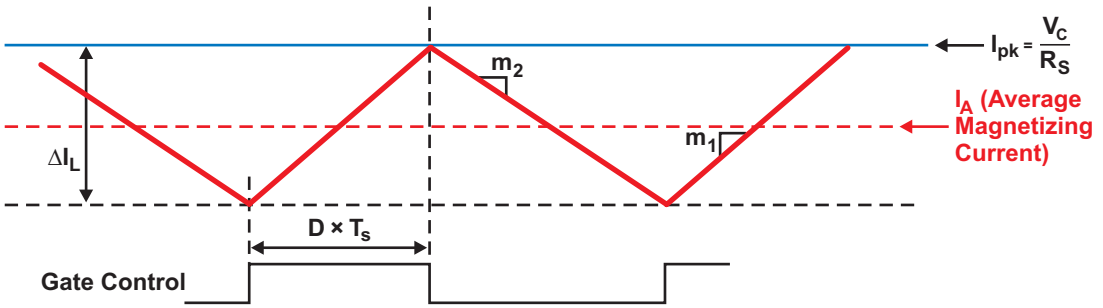


Fig. 21. Peak CMC law: No parasitic or filter delays, no slope compensation, and no feedforward.

Fig. 20 illustrates basic current-feedback circuitry for a flyback power topology using slope compensation (through R_{sc}), with a single comparator used for both CMC and current limiting (similar to UC3843). The RC filter shown eliminates nuisance noise from the current-feedback signal. One typical noise source is the gate charge current when the control switch is turned on. Another technique not shown here is leading-edge blanking, which simply maintains the current-feedback signal at 0 V for a brief period of time when the switch is turned on.

In such a configuration, the voltage (V_C) cannot exceed a maximum voltage (V_{C_LIM}) set by the zener diode in Fig. 20, which controls the peak-current limit. The feedforward resistor (R_{ff}) provides multiple advantages for constant power limit and better line rejection.

Fig. 21 is a very simplified representation of CMC operation with a fixed switching frequency, without any delays or slope compensation.

One characteristic of the flyback topology—particularly in CCM—is that for a predefined current limit, the output current during

short-circuit can reach a much higher value than the output load-current limit, which is the load-current level at which the output voltage begins to fall. This can be explained as:

$$I_{out} = I_{o\_avg} = \frac{I_A}{n_2} \times (1 - D), \quad (13)$$

where I_{out} is the output load current (assumed to be constant), n_2 = N2/N1, and I_A is the average magnetizing current when measured at the primary.

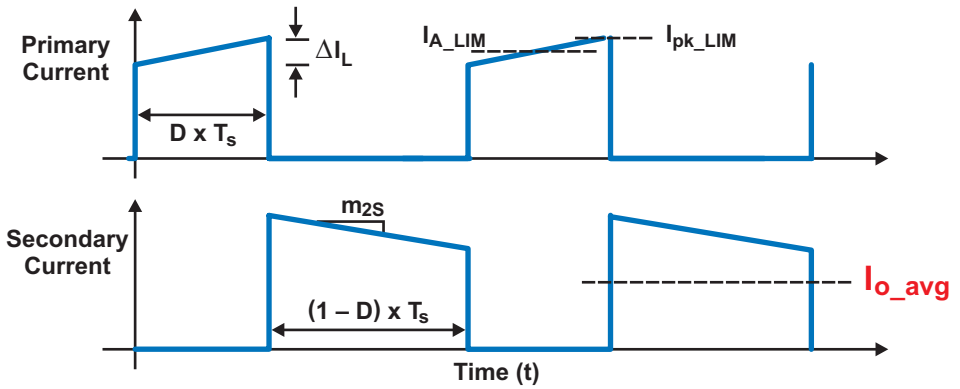
Neglecting the diode (or synchronous rectifier) forward voltage drop, a first approximation of the magnetizing current downslope can be expressed as:

$$m_2 = \frac{\Delta I_L}{(1 - D) \times T_S} \approx \frac{V_o}{n_2 \times L}, \quad (14)$$

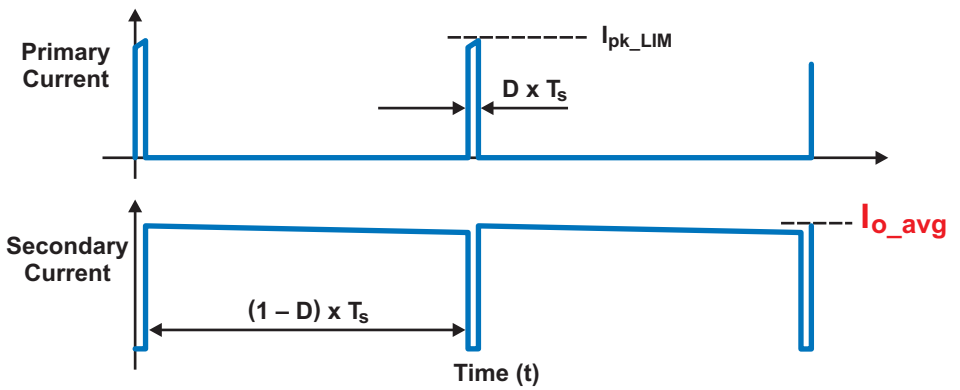
where ΔI_L is the peak-to-peak value of the magnetizing current when measured at the primary during a switching cycle, L is the magnetizing inductance detected at the primary, and D is the control-switch duty cycle. If the load current is exactly at the output load-current-limit threshold, the duty cycle is still defined by the regular equation, which also defines (1 – D).

$$D = \frac{V_o}{n_2 \times V_i + V_o} \quad (15)$$

With a shorted output, however, V_o falls close to zero, which according to Equation 14 reduces the downslope to a very small number and drives the duty cycle to its minimum value (usually determined by delays through current-sense filtering or leading-edge blanking). With a minimum D, (1 – D) approaches unity, increasing the average magnetizing current and allowing the output current to increase to more than twice the value defined by the onset of current limiting (see Fig. 22). For better prediction accuracy, V_o should include the voltage drop of output series elements, including the rectifier (or synchronous rectifier) and output filters.



a. Just at Current Limit.



b. Output short-circuited.

Fig. 22. Output load current from overload to short circuit.

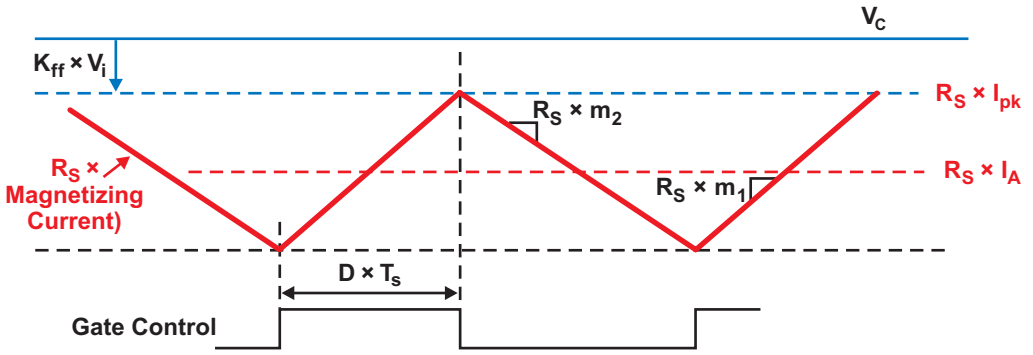


Fig. 23. Peak CMC law: no parasitic or filter delays, no slope compensation, but with feedforward.

A second characteristic of this topology and operating mode is that the output load-current limit is highly dependent on the DC input bus voltage. At a higher bus voltage, the duty cycle gets lower, which means that the magnetizing energy is transferred to the load for a higher proportion of a cycle. Regular power supply controllers have a fixed-peak current-limit threshold based on primary current measurement. The threshold remains the same regardless of the input bus voltage, which indicates an identical magnetizing current at the moment of turn off. Exactly at the peak current-limit operating point, the average current provided to the load depends mainly on the duration of the (1 – D) period; at a 56-V input voltage, the available load current before reaching the current limit is significantly higher (50% is common) than at a 24-V input.

This can be explained with a simplified equation based on Fig. 21:

$$I_A = I_{pk} - \frac{m_2 \times (1-D) \times T_s}{2} = \frac{V_C}{R_S} - \frac{m_2 \times (1-D) \times T_s}{2}, \quad (16)$$

where T_s is the switching period, R_S is the current sense resistor value, and V_C with R_S defines the peak current-limit-voltage threshold.

Also, when in current limit and referring to Equations (13) through (16), the output load current I_{out_LIM} is shown by Equation (17) below, where I_{A_LIM} is the average magnetizing current limit at the primary and V_{C_LIM} is the peak current-limit-voltage threshold (maximum V_C value). If a lower inductance value is selected for a higher current ripple, the peak current-limit threshold (I_{pk_LIM}) may need to be increased.

Impact of Feedforward

When combined with peak CMC, a feedforward technique allows the maximum power output to be maintained relatively constant over a wide input-voltage range, thereby lowering the cost of components that would otherwise have to handle excessive power at high input voltages.

Fig. 23 shows the impact of the feedforward resistor (shown in Fig. 20) on the current-limit threshold. In this and subsequent illustrations, the feedforward contribution ($K_{ff} \times V_i$) is subtracted from the error amplifier's output V_C so that it becomes easier to define the duty-cycle equation. This representation is functionally equivalent to adding feedforward to the current feedback.

The feedforward technique provides better control of the operating conditions during an overload; consequently, it can reduce the amount of stress on the power circuitry in worst-case

$$I_{out\_LIM} = \frac{I_{A\_LIM} \times (1-D)}{n_2} = \frac{V_i}{n_2 \times V_i + V_o} \times \left(\frac{V_{C\_LIM}}{R_S} - \frac{V_o}{2L} \times \frac{V_i}{n_2 \times V_i + V_o} \times T_s \right) \quad (17)$$

situations. For example, reducing the maximum transformer leakage energy at the maximum input voltage results in a lower MOSFET peak-drain voltage in worst-case conditions.

Fig. 24 demonstrates that without any feedforward compensation, a higher input voltage will yield a higher output load current at the point where the current limit has just been reached. If a signal proportional to the input voltage is added to the current feedback, the output load-current limit becomes dramatically less dependent on the input DC voltage. With a relatively constant current limit, the controller's UVLO can also be used more effectively against short-circuits. In Fig. 24, the amount of feedforward is between 13% and 33% of peak current limit.

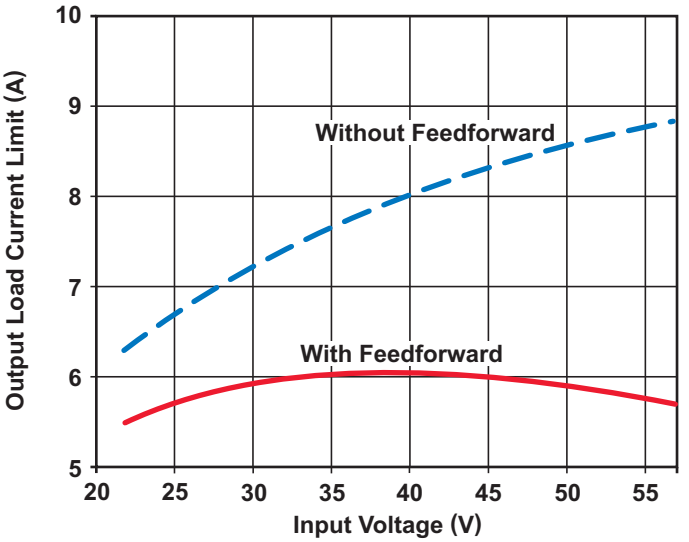


Fig. 24. Impact of feedforward on current limit.

Impact of Slope Compensation

Slope compensation is used to avoid subharmonic oscillation when the operating duty cycle exceeds or even approaches 50%. The effect of slope compensation is illustrated in Fig. 25.

The amount of slope compensation should be such that:

$$\left|\frac{R_S \times m_2}{2}\right| < |m_0| < |R_S \times m_2|, \qquad (18)$$

or between 50% and 100% of the secondary current downslope. The effect of slope compensation on peak current changes according to the duty cycle. Using slope compensation, the higher the duty cycle, the lower the primary peak current for a fixed V_C level. This has the effect of reducing the output load-current limit when at a minimum input voltage. Fig. 26, based on Fig. 20, shows that fact. In this particular case, the current limit is higher with slope compensation than without it at high voltage because the ramp signal is AC-coupled, resulting in a negative contribution at a lower duty cycle.

Impact of Parasitic Delays: Complete Model

Parasitic delays also have a strong effect on current limiting. Fig. 27 illustrates three types of delays. The first one, t_{del_off}, is the turn-off delay, including the controller's delay (mainly the current-sense comparator) and the gate-drive

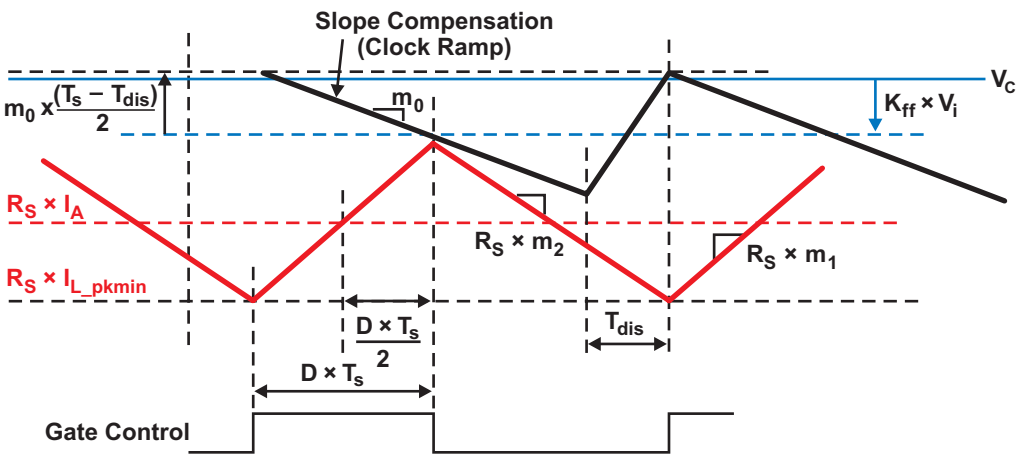


Fig. 25. Peak CMC law: Adding slope compensation to feedforward.

delay. The second one, t_{RC}, is created by the RC filter used at the current-sense input. It impacts both the current-feedback signal as well as the slope-compensation signal (the slope compensation is connected to the current-sense node). The third one, t_{d_CT}, is the primary FET turn-on delay from the clock-ramp signal, assuming that the clock ramp is used for slope compensation (see Fig. 20). The complete model is illustrated in Fig. 27.

Because of t_{del_off} and t_{RC} , the primary FET is turned off late, resulting in a higher current limit than expected. Conversely, a higher t_{d_CT} results in a higher contribution from the slope compensation signal at the same duty cycle, which means a lower current limit. The detailed output load current limit equation becomes as shown below in Equation (19).

Note that these equations are valid as long as there is a volt-second balance in the transformer when the output voltage approaches zero volts. If a short-circuit is applied, imbalance may occur due to parasitic turn-off delay (t_{del_OFF}), which means that the current steps up higher with each succeeding switch period until there is a volt-seconds balance again.

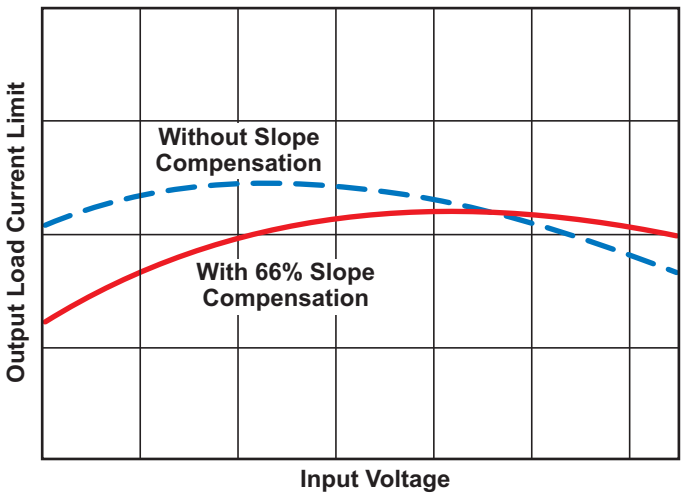


Fig. 26. An example of the influence of slope compensation on current limit.

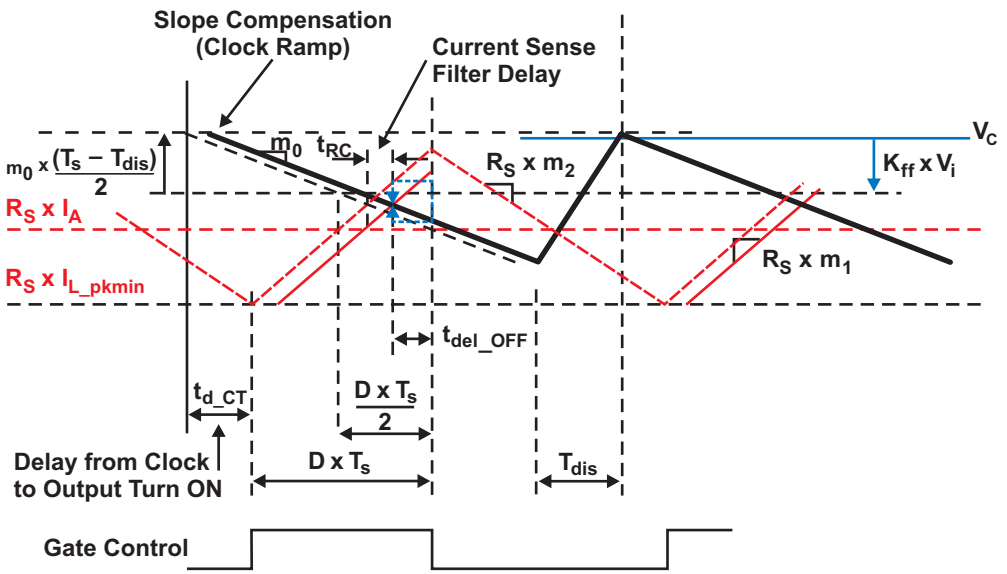


Fig. 27. Peak CMC law: With all delays, slope compensation, and feedforward effect.

$$I_{out\_LIM} = \frac{V_i}{n_2 \times V_i + V_o} \times \left[\frac{V_{C\_LIM}}{R_S} - \left(\frac{V_o}{2L} \times \frac{V_i}{n_2 \times V_i + V_o} \times T_S \right) + \frac{V_i}{L}(t_{del\_OFF} + t_{RC}) - \frac{K_{ff} \times V_i}{R_S} + \frac{m_0}{R_S} \left(\frac{T_s - T_{dis}}{2} - \frac{V_o \times T_S}{n_2 \times V_i + V_o} + t_{del\_OFF} + t_{RC} - t_{d\_CT} \right) \right] \quad (19)$$

Impact of Transformer Leakage on Current Limit

One impact of leakage inductance in a flyback transformer is a loss of volt-seconds during the commutation to secondary windings. As a result, both the duty cycle and the average magnetizing current become higher than expected (compensation coming from the voltage feedback loop), which means a lower efficiency due to higher conduction loss. While increasing the peak current limit could compensate to maintain the maximum available output power, the limit should not be raised to avoid transformer saturation. As a result, the output load-current limit becomes lower. In other words, with a fixed current limit on the primary side, the available current on the secondary is reduced.

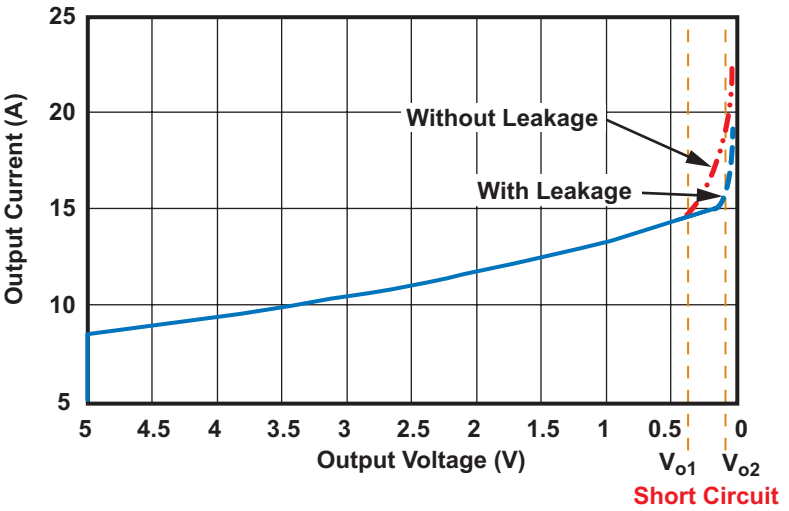


Fig. 28. An example of current-limiting behavior of a flyback power supply with peak CMC during overload.

Fig. 28 is a current-limiting example based on the TPS23754 application showing how high the output current can become when an overload becomes a short-circuit. This assumes that the controller's supply voltage does not go into a hiccup mode.

With a fixed current-limit setting, the output current can go from 8.8 A at 5 V up to 14.5 A at 0.5-V out, or much higher at a lower output voltage. The behavior in the zone between V_{o1} and V_{o2} depends on the transformer's leakage inductance as well as the clamp voltage.

B. Test Results Based on the TPS23754 Application

Using the TPS23754 to control the flyback power supply, tests were performed to show current-limit performance. For test setup details, refer to Section III, Part D, "Test Results: Cross-Regulation." Also, no current transformers were installed. As shown in Fig. 29, the basic characteristics of the TPS23754 circuit are:

- Slope-compensation current ramp (40 µA) provided inside the controller.
- Leading-edge blanking (≅ 1.5% of the switching cycle) so that no RC filtering is needed for current feedback.
- 250-kHz switching frequency.

Table 2 shows the dependency of output load-current limit on input bus voltage and the beneficial effect of feedforward. In each case, the current-limit point corresponds to the load current at which the output voltage starts to decrease. When the load current exceeded the load-current limit by approximately 10%, the power-supply controller went into hiccup mode, since the controller's supply rail was supplied by an auxiliary winding in the flyback transformer. In Table 2, the feedforward with a 120-kΩ resistor amounted to between 13% and 33% of the current-limit threshold.

TABLE 2. IMPROVED CURRENT LIMIT WITH FEEDFORWARD

Without Feedforward		With Feedforward (120-kΩ)	
V_i (V)	I_{out} (A)	V_i (V)	I_{out} (V)
56	8.21	56	5.71
48	7.81	48	5.808
36	6.91	36	5.71
24	5.61	24	5.109

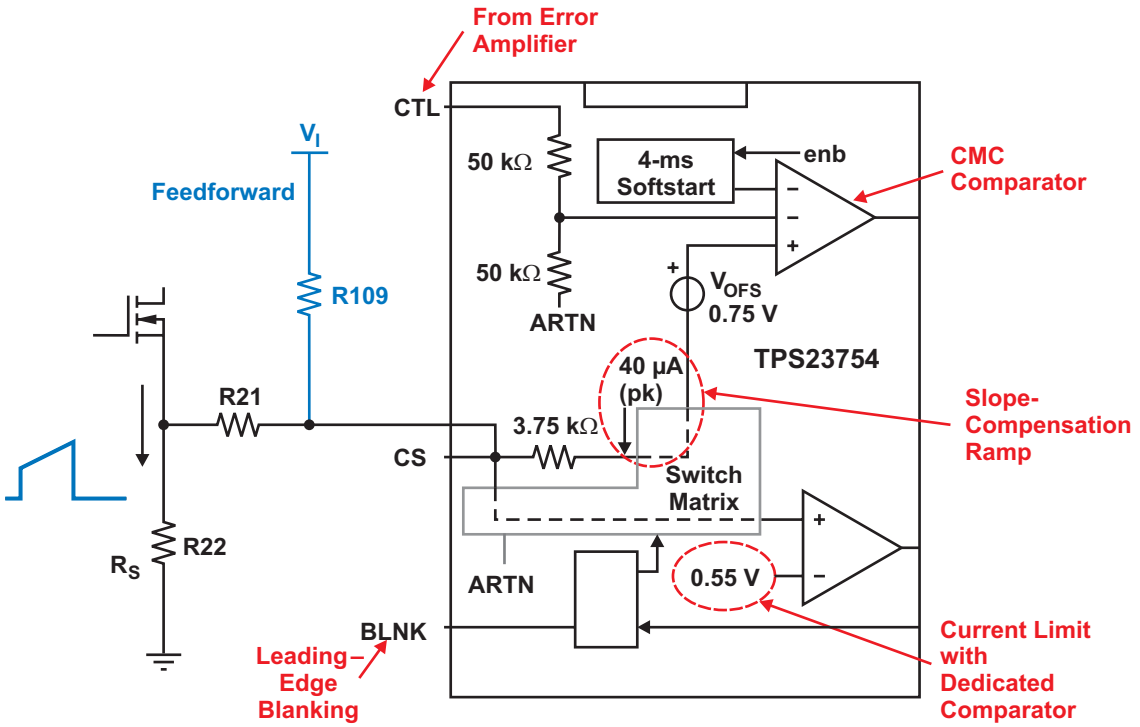


Fig. 29. Current-feedback network using TPS23754.

With a 48-V input and 5.8-A load, the duty cycle and the magnetizing current were 1.8% and 2.2% higher, respectively, than if there had been no effect introduced by the transformer's leakage inductance. The observed D_{tr} was 1.75%.

A similar test with a 24-V input produced an increase of 3.2% and 9.7%, respectively, which is significant.

V. EMI and Line Rejection

This section provides design tips helpful to minimize conducted and radiated EMI generation for a flyback power supply. For a more general discussion on EMI, please refer to Reference [7]. Line rejection, also known as audio susceptibility, will also be discussed.

A. Minimizing EMI in Flyback Applications

For many designers, the flyback converter remains synonymous with a poor EMI signature. EMI has many causes, although one major element is the flyback transformer. Its windings carry high-frequency switched current, making it an H-field (magnetic field) antenna. Some of its windings generate a ringing voltage at frequencies much higher than the switching frequency, making the

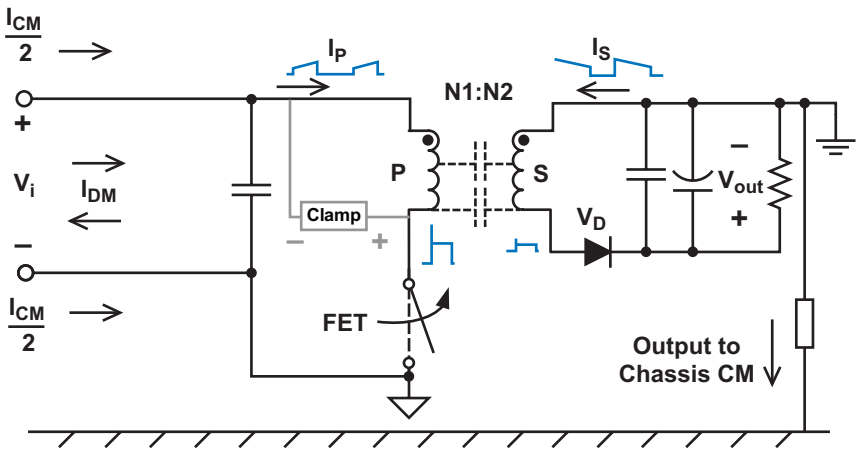


Fig. 30. Interwinding capacitance related to transformer construction.

transformer an E-field (electric field) antenna as well. Interwinding capacitance—specifically primary-to-secondary parasitic capacitance—can make the transformer a common-mode-conduction emission generator, as shown in Fig. 30. Other notable sources of EMI are MOSFET drain printed circuit board (PCB) traces, catch diodes (in series with secondary windings), PCB trace loops, and general PCB layout.

Transformer interwinding capacitance is influenced by how close two windings are to each other. The effective capacitance is usually somewhat less than the calculated physical capacitance because the voltage across the windings is not uniform. The voltage gradient effect must always be considered. The average of the AC voltages on facing portions of the capacitor "plates" determines the stored charge and hence the effective capacity (see Figs. 30 and 31).

An electrostatic shield referenced to the same ground potential as the primary MOSFET can neutralize this common-mode capacitance, forcing any common-mode current to return to the primary circuit through a local path.

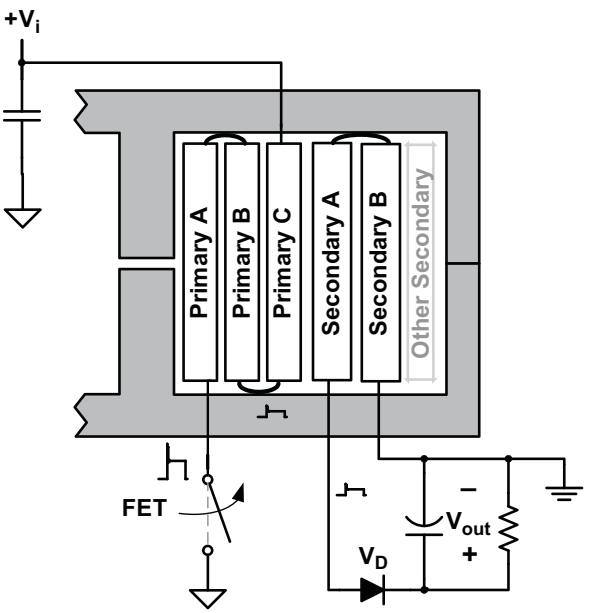


Fig. 31. Winding placement can reduce the effects of interwinding capacitance.

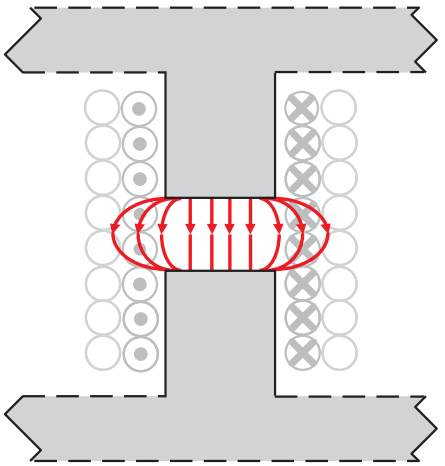


Fig. 32. Fringing flux in center gap of flyback transformer.

Here is a list of standard techniques that help minimize EMI when using a flyback topology:

- The transformer should be center-gapped because the fringing fields from the exposed air gap become a strong source of EMI. As explained previously, this means additional loss related to fringing-flux-induced currents in the winding turns closest to the center gap (see Fig. 32).
- If the primary winding is on multiple layers, it should be wound starting at the winding's end—connected to MOSFET's drain on the printed circuit—so that the outer layers shield the E-field emanating from the drain voltage excitation. This can also help reduce the effect of interwinding capacitance related to the voltage-gradient effect (see Fig. 31).
- A flyback converter is a strong source of ripple current at both its input and output. Use high-frequency, low-impedance capacitors at both the input and output of a flyback transformer, combined with other types of capacitors and filters. Minimize the loop area of fast dI/dt current paths. Use a torroidal-core inductor for output filters; and avoid rod inductors, which generate an H-field because of their open-core shape.
- Pay attention to the reverse-recovery characteristic of catch diodes, which can be source of H-field emissions. Forward recovery, if too slow, will delay the transition time and increase the E-field emission. Schottky diodes, although they don't have reverse-recovery issues, can introduce a resonance with parasitic inductances because of their parasitic parallel capacitance. When necessary, place an RC snubber across the catch diodes.
- The primary MOSFET turn on (but not the turn off) should be slower than the diode's reverse recovery time.
- The PCB layout should be done carefully to minimize EMI. There are many papers written on the subject, such as Reference [7].

B. Optimizing Line Rejection for a Flyback Converter

The line rejection of a power supply, or audio susceptibility, is the ability to reject noise applied to the voltage input.

A flyback converter operating in CMC inherently provides some (although imperfect) line rejection, however, accurately predicting the line rejection of a flyback converter is not straightforward; complex mathematical or simulation models are required. Also, line rejection is highly dependent on parasitics; prediction accuracy directly depends on accounting for the influence of each parasitic. For these reasons, lab tests are usually necessary in order to validate predictions. Fig. 33 on the next page shows a simplified flyback schematic, with a control-loop block diagram.

In the block diagram of Fig. 33, the K_{vi1} block shows the influence of input-voltage variations on the small-signal changes of the magnetizing current. The following simple equation, applicable during the ON time, can help clarify:

$$\Delta I_L = V_i \times \frac{D \times T_s}{L}. \qquad (20)$$

The gain from a variation in V_i to I_L is proportional to D. With peak CMC, there is inherent (K_{FF_in}) feedforward, because when V_i increases, so does the rise rate of the magnetizing current. The peak current threshold is reached earlier, which results in a reduced duty cycle.

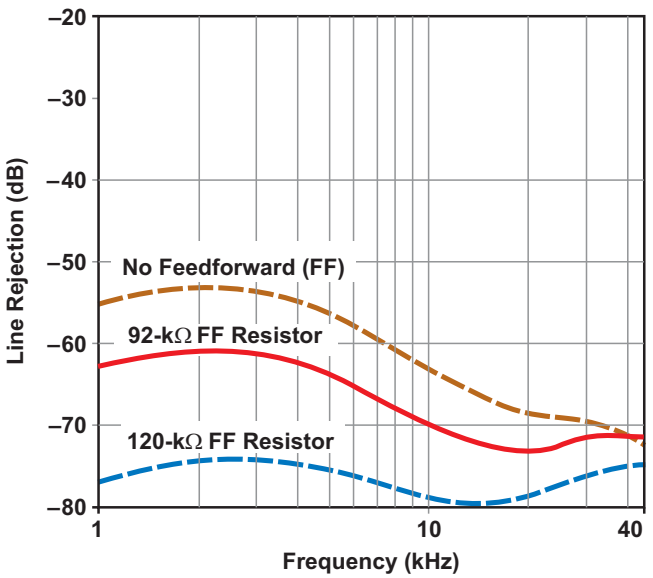
On the other hand, the K_{vi2} block shows that, when excluding the effect of the current loop, there is a natural direct impact from V_i to V_o. It is a nonlinear relationship.

Using the same K_{ff} external feedforward (introduced in the current-limit section) can help improve line rejection. It cannot provide a perfect cancellation in all operating conditions, however, because of the nonlinear nature of noise susceptibility in a flyback converter.

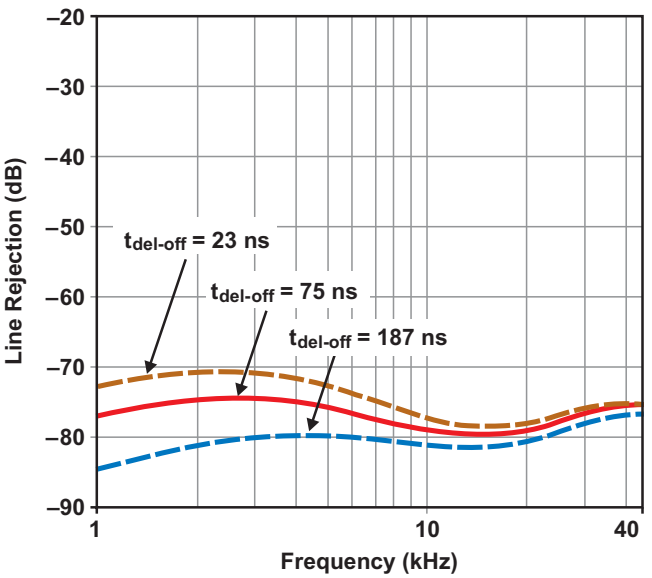
Still, the K_{ff} feedforward constitutes a very simple way, by using a resistor, to achieve very good line rejection for a specific input-voltage range, sometimes improving the rejection by more than 20 db and often removing the need for a second-stage (and inefficient) linear regulator.

As shown in the K_{FF_in} block (proportional to $a \times D \times T_s - t_{delays}$), the line-rejection performance of the flyback converter is dependent on turn-off delays, t_{delays} being in fact $t_{del\_OFF} + t_{RC}$ discussed previously in the current-limit section.

Fig. 34 illustrates the effects of feedforward and turn-off time delays in the TPS23754 application circuit.



a. Effects of feedforward resistor.



b. Effects of turn-off time delays with 120-kΩ feedforward resistor.

Fig. 34. Line rejection example at 48 V, $I_{5\ V}$ = 5 A, 1-Ω source impedance, 20-µH EMI inductance.

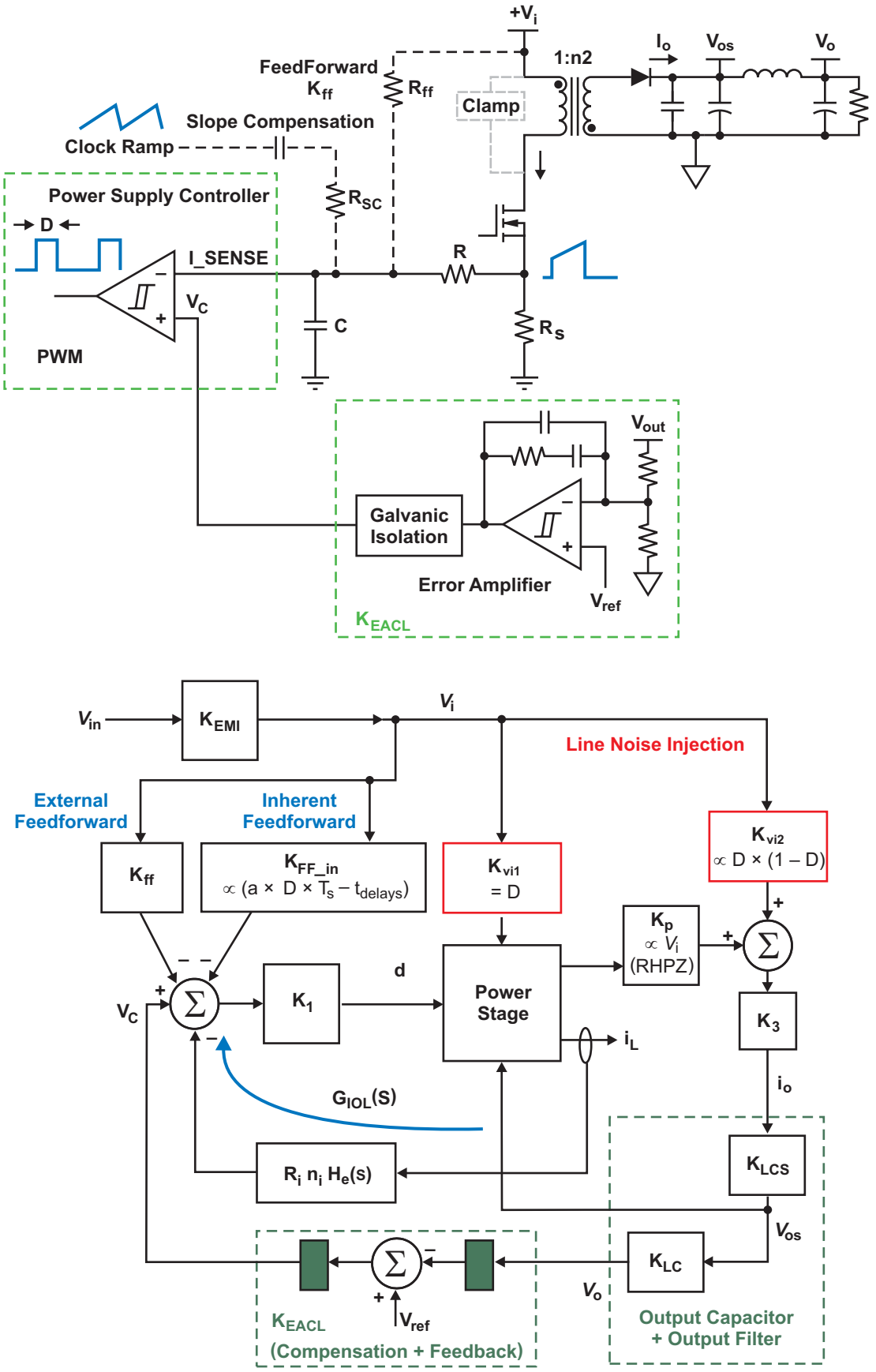


Fig. 33. Peak CMC flyback simplified schematic and block diagram.

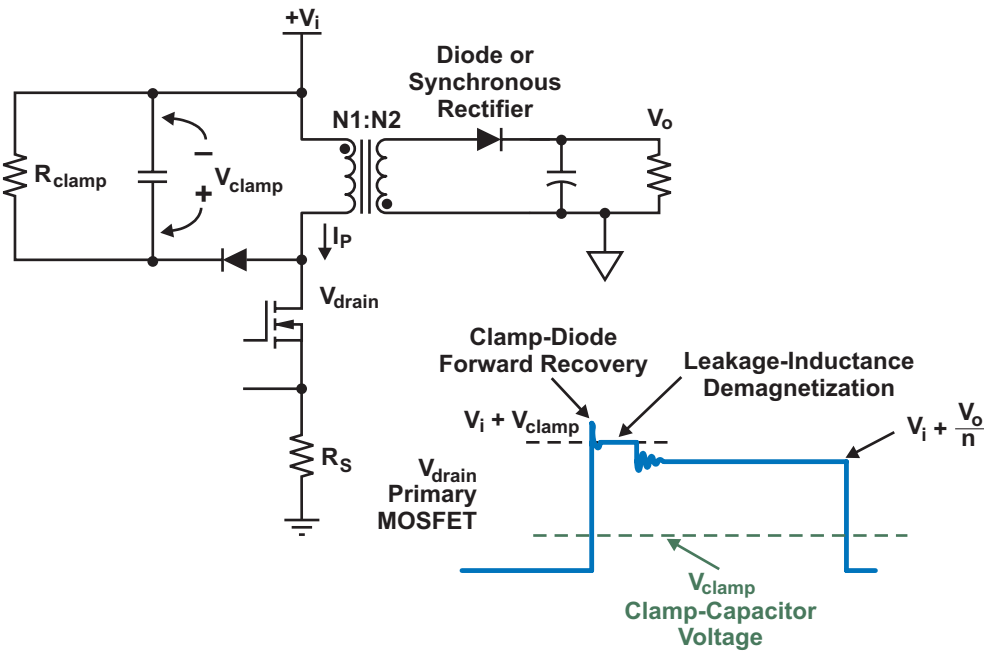


Fig. 35. Primary MOSFET drain voltage while using RCD clamp circuit.

VI. Snubbers and Clamp Circuits

Leakage energy in the flyback transformer requires the use of special clamp and/or snubber circuits in order to help protect the power switches and diodes against voltage breakdown failures.

There are many configurations for these circuits. The RCD clamp is a common approach for protecting the primary circuit. When efficiency is a concern, the nondissipative clamp circuit offers several good trade-offs. RC snubbers are the typical solutions for secondary protection.

A. RCD Clamp in Primary Circuit

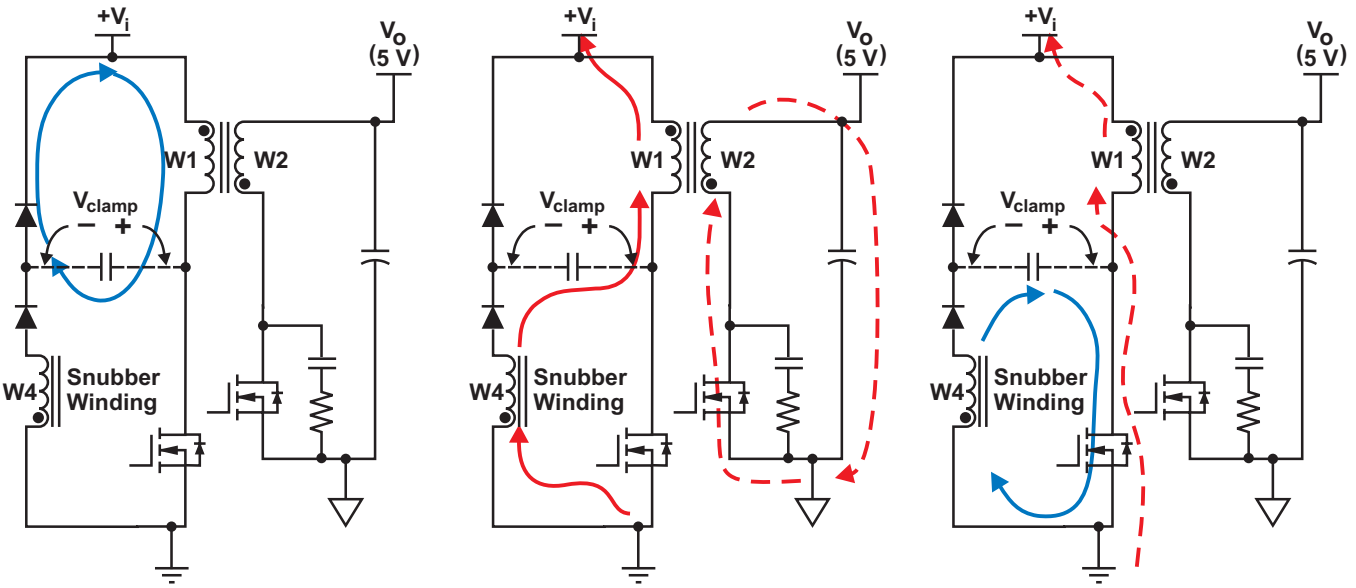
The RCD clamp works by creating a low-impedance voltage source connected to the input voltage. The resistor, R_{clamp}, dissipates power linked to the leakage energy, while the clamp capacitor ensures low voltage ripple (see Fig. 35). The clamp-capacitor voltage, which is constant during a switching cycle (with a large enough capacitance value), is maximum at full load and with minimum input voltage, which is the case where leakage energy is at a maximum.

It is important to select the resistance value to guarantee acceptable drain voltage in the worst case, which includes long-duration overload conditions. Also important is the type of diode, since a slow forward recovery will affect the maximum drain voltage at turn off. Of course, the power dissipation capability of the resistor needs to be adequate for the application.

Knowing the leakage inductance, the resistance value can be estimated as follows, assuming there are no stray capacitances to charge and that all of the leakage energy is conducted into the snubber capacitor:

$$R_{clamp} = \frac{2 \times \left(V_{clamp} - \frac{V_o}{n} \right) \times V_{clamp}}{Freq \times L_{leakP} \times I_{pkP}^2}, \quad (21)$$

where L_{leakP} is the total leakage inductance when moved to the primary side of transformer and I_{pkP} is the primary current at the moment turn off occurs. This circuit also needs to be tested in order to verify the potential impact of other parasitics, as well as the contribution from the parameters ignored in Equation (21), including diode forward voltage and recovery characteristics. Also, as mentioned earlier, the primary clamp-circuit design must be based on trade-offs between efficiency, peak drain voltage, output current limit, and cross-regulation.



a. Primary MOSFET turn off: Initial recharge of clamp capacitor.

b. Primary MOSFET turn off: If V_{clamp} is too high, there is partial discharge before reaching final voltage.

c. Primary MOSFET turn on.

Fig. 36. Nondissipative clamp circuit.

B. Nondissipative Clamp Circuit

Because the power lost in a clamp circuit can significantly affect overall power-supply efficiency, many circuits have been derived to minimize or eliminate this loss. Although successful in this effort, such solutions almost always add additional circuit complexity and thus demand a good engineering trade-off analysis. There is an innovative alternative based on the addition of a snubber winding incorporated within the flyback power transformer. This type of clamp circuit works very differently than the RCD clamp, as shown in Fig. 36.

The main characteristics of this clamp type are:

- Improved efficiency, combined with lower voltage stress on the primary MOSFET.
- Improved cross-regulation. The clamp voltage does not appear instantaneously. It increases gradually during the commutation period, which reduces the ringing effect. Also, its final voltage is significantly lower than with the RCD circuit, resulting in a smoother and longer commutation. As a result, the current shared between secondary windings during commutation is less dependent on the transformer parasitics and therefore better follows the load level of each output.
- Current limit is reached at lower load current, which is a disadvantage. The commutation from primary to secondary is more gradual (slower), which means that more volt-seconds are lost. Consequently, the power-supply current limit can be reached at a lower load current.

This clamp circuit works by first absorbing the leakage energy in the clamp capacitor and then recycling it, through an additional transformer winding called a snubber winding. In theory, no energy is lost.

At primary MOSFET turn off, the clamp capacitor is at first recharged until V_{clamp} reaches the secondary voltage reflected to the primary side. Then, V_{clamp} reaches a peak voltage that is influenced by the leakage energy and the other parasitic elements of the circuit, as shown on the left side of Fig. 36. If V_{clamp} has become too high, the excess energy is recycled to the output rail and the input bus. This first discharge is performed by the forward transformer effect. When the primary

MOSFET is turned back on, the clamp capacitor is then discharged, using forward coupling between W4 and W1. This discharge is performed with close to 100% overshoot.

This type of clamp can be very efficient when the input bus-voltage range is reasonable; from 36 to 56 V, for example. For a wider range, it still works, but may lose its efficiency advantage. In this 48-V, 25-W application, implementing this nondissipative clamp with a 10-nF NPO capacitor and a 14-turn snubber winding, it was possible to increase the efficiency to 93%, which is 1% more than that achieved with an RCD clamp.

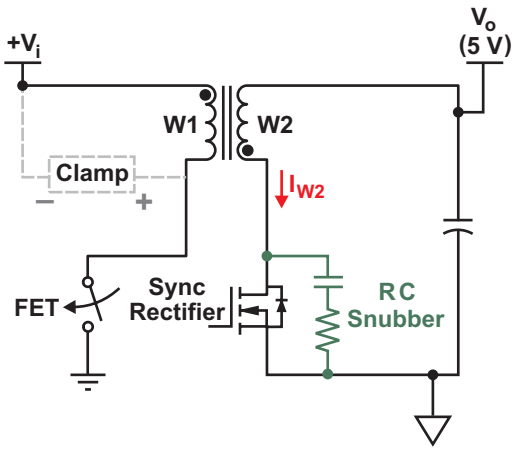


Fig. 37. RC snubber circuit for synchronous rectifier.

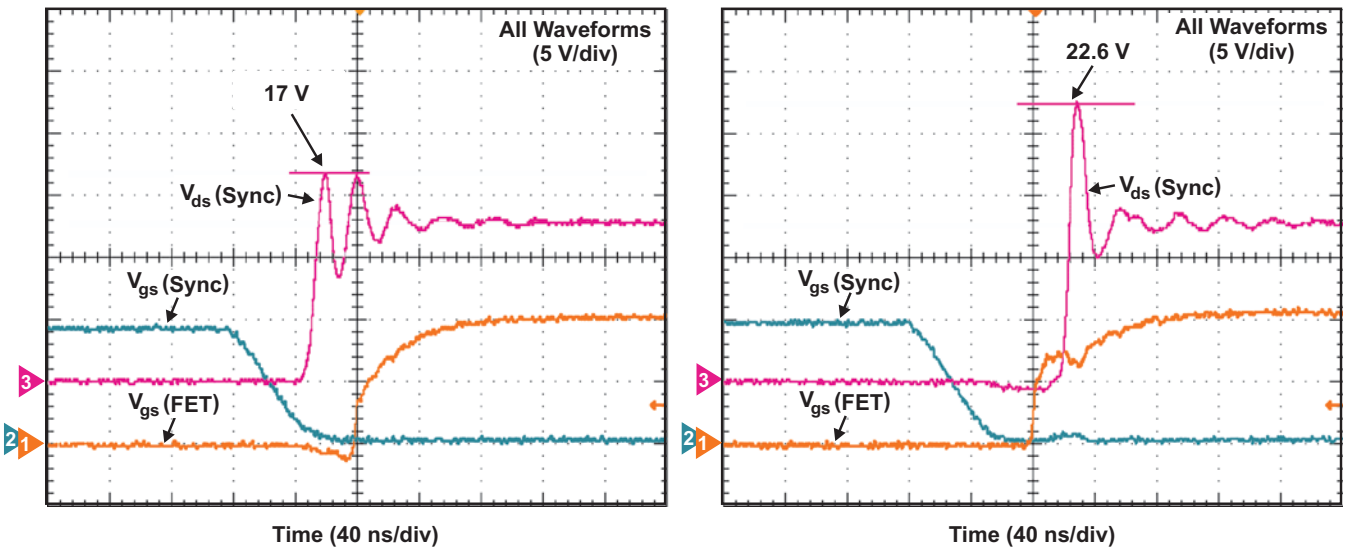
C. Voltage Stress at Secondary Windings, Snubbers

The semiconductors located on the secondary side of flyback transformers also are subject to voltage transients during commutations. In some cases, protection circuits such as RC snubbers can be useful (see Fig. 37).

When using a synchronous rectifier, voltage stress across the MOSFET may happen under two different circumstances when there is commutation from secondary to primary. First, at no load, the magnetizing current is changing polarity during a switching cycle, reaching a peak negative value until the synchronous rectifier is turned off, resulting in leakage energy. Also, if excessive cross-conduction exists with the primary MOSFET during the commutation, there is then a direct transformer coupling. This creates strong leakage energy in the secondary winding and increases the voltage stress on the synchronous rectifier.

Second, at full load, the dead time between both MOSFETs during commutation will result in conduction—and thus reverse recovery issues—of the synchronous rectifier's body diode, leading to transient stress in the synchronous rectifier.

Fig. 38 shows both situations. Notice that at full load, the voltage stress happens well after the sync rectifier was turned off but exactly when the primary MOSFET is turned on, thus confirming reverse recovery. At no load, the effect of the



a. No load. *b. Full load.*

Fig. 38. Voltage stress on the synchronous rectifier with a 10-Ω/1.2-nF snubber and a SIR414 MOSFET.

negative magnetizing current results in leakage energy at the time the synchronous rectifier is turned off. For that particular case, there is no overlapping of V_{gs}(Sync) and V_{gs}(FET), which limit the voltage stress at no load.

There is an optimum value for resistance and capacitance beyond which the voltage stress cannot be reduced further. It is important to optimize the snubber by testing, using the final transformer and MOSFETs.

Snubber turn-off loss can be estimated with this equation, excluding parasitic drain-to-source capacitance:

$$P_{sn} = \begin{bmatrix} C_{sn} \times \left(V_o + n \times V_i\right)^2 \\ + \frac{1}{2} \times L_{leakS} \times I_{pkS}^2 \end{bmatrix} \times Freq, \qquad (22)$$

where C_{sn} is the snubber capacitance, I_{pkS} is the peak negative secondary current, and L_{leakS} is the secondary-to-primary leakage inductance when moved to the secondary side. It is important to test and look for voltage overshoot across the output diodes to ensure that their voltage rating is adequate.

Other types of snubbers could also be considered. A saturable core in series with the synchronous rectifier at secondary winding can give good results, in addition to providing some immunity against excessive reverse recovery. The behavior of saturable cores is not covered in this topic.

VII. Conclusions

Many design factors and parasitic elements can strongly influence a flyback converter's behavior, particularly with respect to the behavior under overload or short-circuit conditions. The flyback transformer is a major component of the converter and needs to be carefully designed and tested for good cross-regulation, maximum efficiency, and low EMI.

The benefits of adding feedforward control do offer improved line rejection, as well as allowing the maximum power output to be held constant over a wider input voltage range. This reduces the cost of components that would otherwise be required to handle the excessive power or voltage stress at high-input voltages.

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APPENDIX A. DETAILED ANALYSIS OF FLYBACK POWER-SUPPLY CURRENT LIMITING WITH INFLUENCE FROM PARASITICS

A power-supply's current-limiting characteristic determines the maximum power available at its output, beyond which the output voltage falls out of regulation. It is also used to predict the output current in overload situations like a short-circuit, in which case the current may be significant. Appendix A presents an in-depth mathematical analysis for predicting the current-limiting behavior of a flyback power supply.

Fig. A-1 illustrates a basic current-feedback circuitry for a flyback power supply using slope compensation (through R_{sc}), with a single comparator used for both CMC and current limiting. The RC filter is used to eliminate nuisance noise from the current feedback signal. In such a configuration, the voltage (V_C) cannot exceed the maximum value set by the zener diode (V_{C_LIM}), which defines the peak current limit. The feedforward resistor (R_{ff}) provides a constant power limit.

It is assumed for this analysis that the converter operates with peak CMC in CCM. Its simplified CMC law is illustrated in Fig. A-2.

I. Impact of Feedforward

Combining the feedforward technique with peak CMC allows the maximum power output to be maintained fairly constant over a wide input-voltage range.

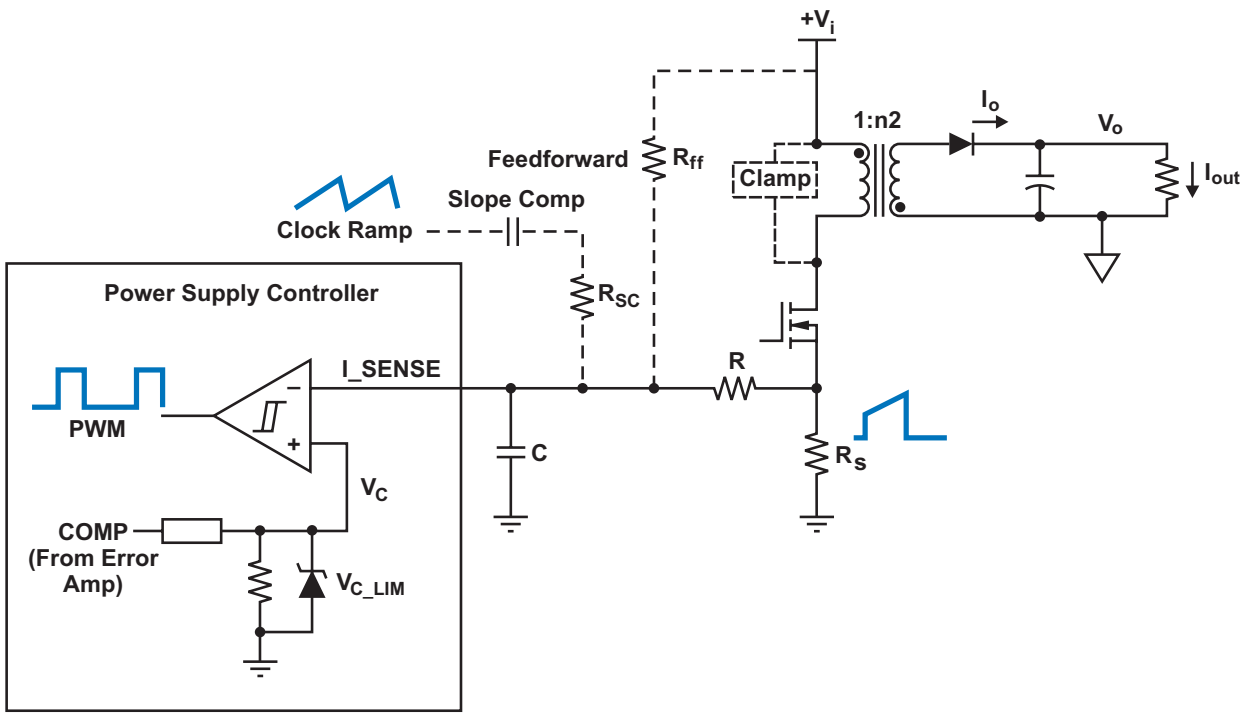

Fig. A-1. Current feedback network of flyback power supply.

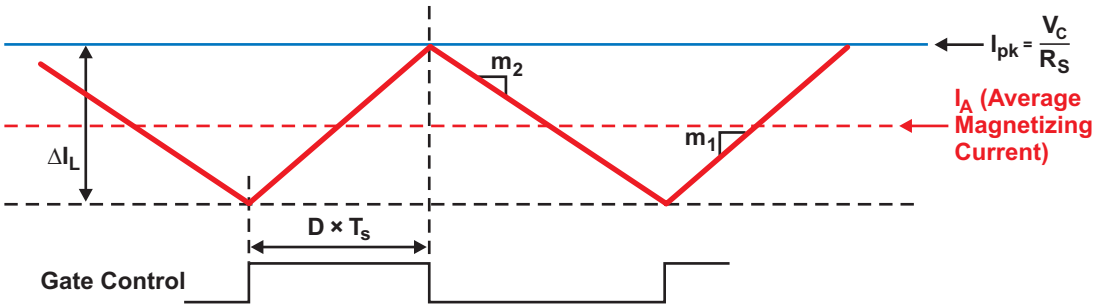

Fig. A-2. Peak CMC law: No parasitic or filter delays, no slope compensation, and no feedforward.

Fig. A-3 shows the impact of the feedforward resistor on the current limit. The feedforward contribution is subtracted from the error amplifier's output V_c so that it becomes easier to define the duty-cycle equation. This representation is functionally equivalent to adding the feedforward to the current feedback.

The equation of the output load-current limit becomes as shown below in Equation (A-1), where K_{ff} is the external feedforward gain. Referring to Fig. A-1, K_{ff} can be calculated as:

$$K_{ff} = \frac{\frac{R_{sc} \times (R + R_S)}{R_{sc} + R + R_S}}{\frac{R_{sc} \times (R + R_S)}{R_{sc} + R + R_S} + R_{ff}} = \frac{R_{sc} \times (R + R_S)}{R_{sc.} \times (R + R_S) + R_{ff} \times (R_{sc} + R + R_S)}. \quad \text{(A-2)}$$

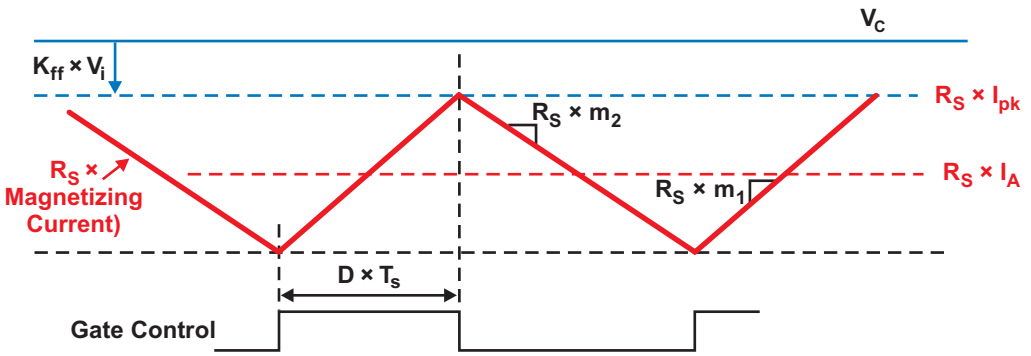

Fig. A-3. Peak CMC law: No parasitic or filter delays, no slope compensation, but with feedforward.

$$I_{out\_LIM} = \frac{I_{A\_LIM} \times (1 - D)}{n_2} = \frac{V_i}{n_2 \times V_i + V_o} \times \left(\frac{V_{C\_LIM}}{R_S} - \frac{V_o}{2L} \times \frac{V_i}{n_2 \times V_i + V_o} \times T_s - \frac{K_{ff} \times V_i}{R_S} \right) \quad \text{(A-1)}$$

II. Adding Slope Compensation

Slope compensation is used to avoid sub-harmonic oscillation when the operating duty cycle exceeds or even approaches 50%. The amount of slope compensation should be between 50% and 100% of the secondary current downslope, a typical ratio being around 65%.

The effect of slope compensation is illustrated in Fig. A-4. Its contribution is subtracted from the error amplifier's output V_c, so that it becomes easier to define the duty-cycle equation. This representation is functionally equivalent to adding the slope compensation to the current feedback.

As shown in Fig. A-4, the control MOSFET is turned off once the current feedback signal crosses over the reference signal. The basic equation for regular CMC or current-limit determination is shown below in Equation (A-3), where T_{dis} is the duration of the other slope of the ramp as shown in Fig. A-4. Also, m_1 is defined as:

$$m_1 = \frac{\Delta I_L}{D \times T_s} \approx \frac{V_i}{L}. \tag{A-4}$$

Still referring to Fig. A-4, the slope compensation voltage ramp is defined as:

$$\begin{aligned} m_o &= m_{ramp} \times \frac{\dfrac{R_{ff} \times (R + R_S)}{R_{ff} + R + R_S}}{\dfrac{R_{ff} \times (R + R_S)}{R_{ff} + R + R_S} + R_{sc}} \\ &= m_{ramp} \times \frac{R_{ff} \times (R + R_S)}{R_{ff} \times (R + R_S) + R_{sc} \times (R_{ff} + R + R_S)}, \end{aligned} \tag{A-5}$$

where m_{ramp} is the rising slope of the ramp signal shown in Fig. A-1.

The new output load current limit becomes as shown below in Equation (A-6).

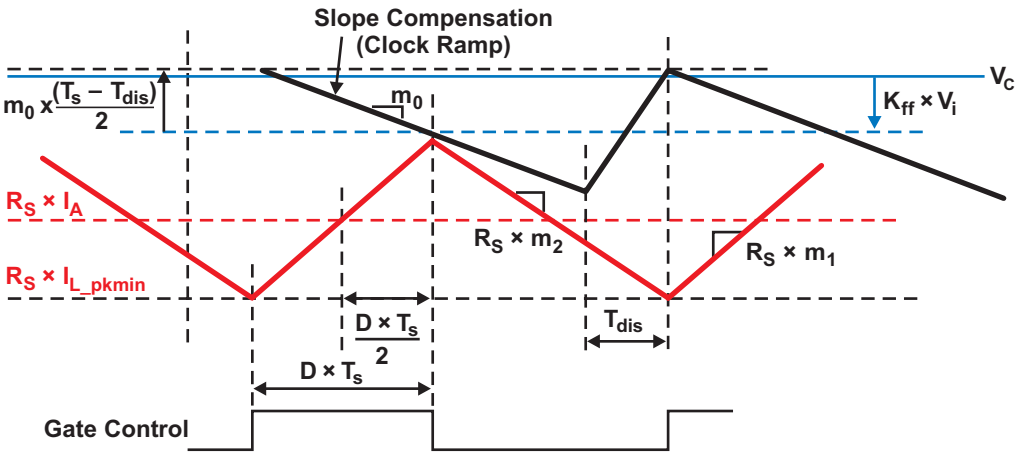

Fig. A-4. Peak CMC law: No parasitic or filter delays, but with slope compensation and feedforward.

$$R_S \times \left[I_A + m_1 \times \left(\frac{D \times T_s}{2} \right) \right] = V_c - K_{ff} \times V_i + m_o \times \left(\frac{T_s - T_{dis}}{2} - D \times T_s \right), \tag{A-3}$$

$$I_{out\_LIM} = \frac{I_{A\_LIM} \times (1 - D)}{n_2} = \frac{V_i}{n_2 \times V_i + V_o} \times \left[\frac{V_{C\_LIM}}{R_S} - \frac{V_o}{2L} \times \frac{V_i}{n_2 \times V_i + V_o} \times T_s - \frac{K_{ff} \times V_i}{R_S} + \frac{m_o}{R_S} \times \left(\frac{T_s - T_{dis}}{2} - \frac{V_o \times T_s}{n_2 \times V_i + V_o} \right) \right] \tag{A-6}$$

III. Including Delays

For a more accurate prediction, time delays including parasitics must be included in the analysis. The effect of parasitic turn-off delay is illustrated in Fig. A-5 .

As shown, the turn off of the control MOSFET is delayed by a time delay t_{del_OFF} . Note that V_c is lower than in previous figure in order to maintain regulation, assuming the same load current.

The equation for CMC or current limit is shown below in Equation (A-7). The output load-current limit becomes as shown in Equation (A-8). If then we add the current filter time delay t_{RC} and the time delay t_{d_CT} from the slope compensation ramp to the control MOSFET turn on, the CMC becomes as shown in Fig. A-6 on the next page.

The detailed equation for CMC or current limit becomes as shown below in Equation (A-9). The detailed output load-current limit equation becomes as shown in Equation (A-10). Note that these equations are valid as long as there is a volt-seconds balance at the transformer when the output voltage approaches zero volts. If a short-circuit is applied, imbalance may occur due to parasitic turn-off delay.

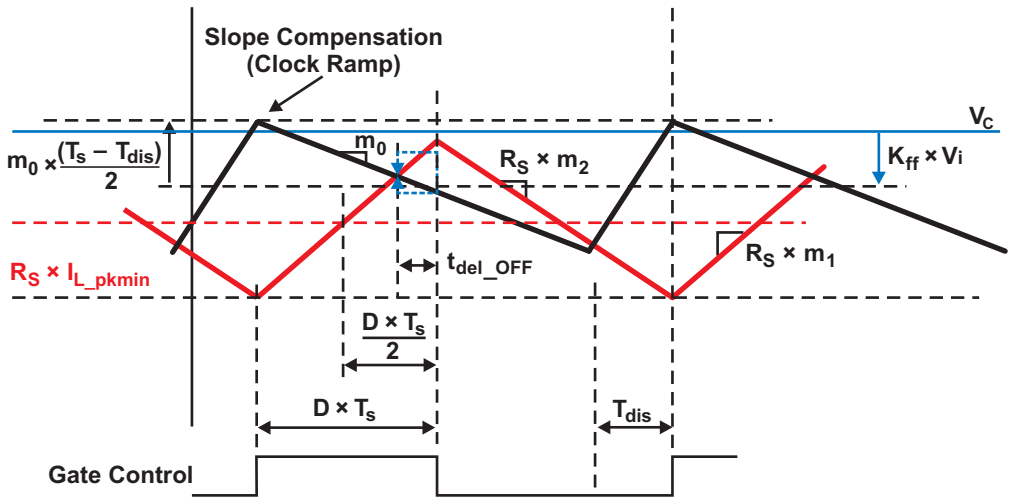

Fig. A-5. Peak CMC law: Parasitic turn-off delay added:

$$R_S \times \left[I_A + m_1 \times \left(\frac{D \times T_s}{2} - t_{del\_OFF} \right) \right] = V_C - K_{ff} \times V_i + m_o \times \left(\frac{T_s - T_{dis}}{2} - D \times T_s + t_{del\_OFF} \right). \quad \text{(A-7)}$$

$$I_{out\_LIM} = \frac{V_i}{n_2 \times V_i + V_o} \times \left[\begin{array}{l} \frac{V_{C\_LIM}}{R_S} - \frac{V_o}{2L} \times \frac{V_i}{n_2 \times V_i + V_o} \times T_s + \frac{V_i}{L} \times t_{del\_OFF} - \frac{K_{ff} \times V_i}{R_S} \\ + \frac{m_o}{R_S} \times \left(\frac{T_s - T_{dis}}{2} - \frac{V_o \times T_s}{n_2 \times V_i + V_o} + t_{del\_OFF} \right) \end{array} \right] \quad \text{(A-8)}$$

$$R_S \times \left[I_A + m_1 \times \left(\frac{D \times T_s}{2} - t_{RC} - t_{del\_OFF} \right) \right] = V_c - K_{ff} \times V_i + m_o \times \left(\frac{T_s - T_{dis}}{2} - t_{d\_CT} - D \times T_s + t_{del\_OFF} + t_{RC} \right). \quad \text{(A-9)}$$

$$I_{out\_LIM} = \frac{V_i}{n_2 \times V_i + V_o} \times \left[\begin{array}{l} \frac{V_{C\_LIM}}{R_S} - \frac{V_o}{2L} \times \frac{V_i}{n_2 \times V_i + V_o} \times T_s + \frac{V_i}{L} \times (t_{del\_OFF} + t_{RC}) - \frac{K_{ff} \times V_i}{R_S} \\ + \frac{m_o}{R_S} \times \left(\frac{T_s - T_{dis}}{2} - \frac{V_o T_s}{n_2 \times V_i + V_o} + t_{del\_OFF} + t_{RC} - t_{d\_CT} \right) \end{array} \right] \quad \text{(A-10)}$$

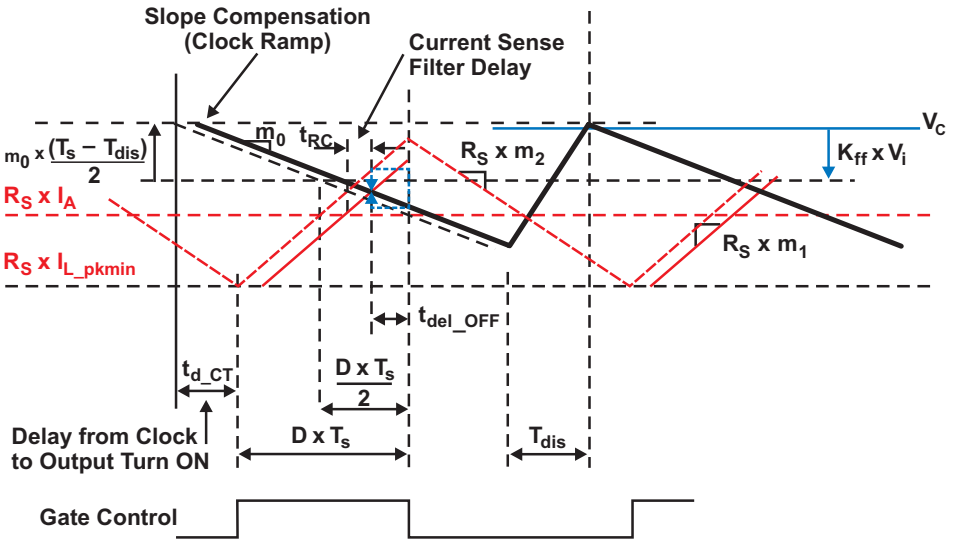

Fig. A-6. Peak CMC law: With all delays and feedforward effect.

IV. Including the Effect of Transformer Leakage

One impact of the leakage inductance of a flyback transformer is a loss of volt-seconds during the commutation to secondary windings. Referring to Fig. 5, during the primary-to-secondary commutation period (D_{tr}), the voltage applied to the magnetizing inductance on the primary side is approximately the clamp voltage itself, while the difference between the magnetizing inductance voltage and the output voltage (neglecting voltage across the rectifier) is across the leakage inductance.

The new duty-cycle equation becomes:

$$V_i \times D_{new} \approx \left[\begin{array}{l} V_{clamp} \times D_{tr} + \\ \frac{V_o}{n_2} \times (1 - D_{new} - D_{tr}) \end{array} \right], \qquad \text{(A-11)}$$

that is:

$$D_{new} \approx \frac{\frac{V_o}{n_2} + D_{tr} \times \left(V_{clamp} - \frac{V_o}{n_2} \right)}{V_i + \frac{V_o}{n_2}}. \qquad \text{(A-12)}$$

The duty-cycle increase is:

$$D_\Delta \approx \frac{D_{tr} \times \left(V_{clamp} - \frac{V_o}{n_2} \right)}{V_i + \frac{V_o}{n_2}}. \qquad \text{(A-13)}$$

D_Δ is usually higher at lower input-bus voltages.

D_{tr} can be estimated as follows:

$$D_{tr} \cong \frac{I_{pkS} \times L_{lkS}}{(n_2 \times V_{clamp} - V_o) \times T_s}, \qquad \text{(A-14)}$$

where L_{lkS} is the secondary-to-primary leakage inductance measured from the secondary. The secondary peak current (I_{pkS}) must be estimated starting from the projected load-current limit.

$$I_{pkS} \approx \frac{I_{out}}{1 - D} + \frac{V_o \times T_s \times (1 - D)}{2L \times n_2^2} \qquad \text{(A-15)}$$

The magnetizing current is also affected by the leakage inductance, since during D_{tr} part of the energy is not delivered to the output, but is instead delivered to the clamp. Assuming that no energy is delivered to the output during 50% of D_{tr}, the new

peak magnetizing current is estimated below by Equation (A-16)

The effects of leakage inductance must be considered when designing the flyback transformer in order to avoid risks of saturation. Adding the influence of leakage inductance, the output load current-limit equation then becomes as shown below in Equation (A-17).

The current-limit equations shown previously are valid as long as there is a volt-seconds balance at the transformer when the output voltage approaches zero. If a short circuit is applied, imbalance may occur due to parasitic turn-off delay, which means that the current steps up higher with each succeeding switch period until there is volt-seconds balance again. The volt-seconds balance equation is as shown below in Equation (A-18).

The transformer's leakage inductance helps maintain that balance as indicated by the last component of Equation (A-18). There is rarely a complete short-circuit situation given the effect of resistive series elements (including parasitics) and the catch diode's forward voltage drop. They should be included when defining the output voltage.

$$I_{pk\_new} \approx \frac{I_{out}}{\left(1 - D_{new} - 0.5 \times D_{tr}\right)} \times n_2 + \frac{V_i}{2L} \times T_s \times D_{new} \tag{A-16}$$

$$I_{out\_LIM} \cong \frac{\left(\dfrac{V_i}{V_i + \dfrac{V_o}{n_2}} - D_\Delta - 0.5 \times D_{tr} \right)}{n_2} \times \left[\begin{array}{l} \dfrac{V_{C\_LIM}}{R_S} - \dfrac{V_i \times D_{new} \times T_s}{2L} + \dfrac{V_i}{L} \times (t_{del\_OFF} + t_{RC}) - \dfrac{K_{ff} \times V_i}{R_S} \\ + \dfrac{m_o}{R_S} \times \left(\dfrac{T_s - T_{dis}}{2} - D_{new} \times T_s + t_{del\_OFF} + t_{RC} - t_{d\_CT} \right) \end{array} \right] \tag{A-17}$$

$$\frac{V_{o\_short}}{n_2} \times (T_s - t_{del\_OFF} - D_{tr} \times T_s) = V_i \times t_{del\_OFF} - V_{clamp} \times D_{tr} \times T_s \tag{A-18}$$